1.35V DDR3L SORDIMM

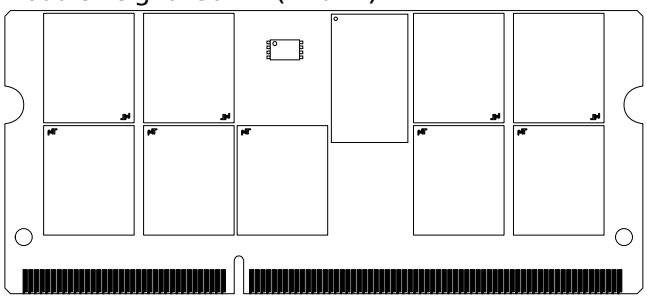
MT36KSS2G72RHZ – 16GB

Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small outline registered dual in-line memory module (SO-RDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 16GB (2 Gig x 72)
- V_{DD} = 1.35V (1.283–1.45V)
- V_{DD} = 1.5V (1.425–1.575V)
- Backward compatible to V_{DD} = 1.5V ±0.075V
- V_{DDSPD} = 3.0–3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Quad rank, using 4Gb TwinDie™ devices
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 204-Pin SODIMM (MO-268)

Module height: 30mm (1.181in)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 204-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)							^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G6	PC3-12800	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	16GB
Refresh count	8K
Row address	64K A[15:0]
Device bank address	8 BA[2:0]
Device configuration	8Gb (1 Gig x 8)
Column address	1K A[9:0]
Module rank address	4 S#[3:0]

Table 3: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT41K1G8,[1] 8Gb 1.35V TwinDie DDR3L SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT36KSS2G72RHZ-1G6__	16GB	2 Gig x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT36KSS2G72RHZ-1G4__	16GB	2 Gig x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT36KSS2G72RHZ-1G1__	16GB	2 Gig x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT36KSS2G72RHZ-1G6E1.

Pin Assignments

Table 4: Pin Assignments

204-Pin DDR3 SO-RDIMM Front								204-Pin DDR3 SO-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	V_{SS}	105	A1	157	DM5	2	V_{SS}	54	DQ28	106	A2	158	V_{SS}
3	V_{SS}	55	DQ24	107	A0	159	DQ42	4	DQ4	56	DQ29	108	BA1	160	DQ46
5	DQ0	57	DQ25	109	V_{DD}	161	DQ43	6	DQ5	58	V_{SS}	110	V_{DD}	162	DQ47
7	DQ1	59	DM3	111	CK0	163	V_{SS}	8	V_{SS}	60	DQS3#	112	PAR_IN	164	V_{SS}
9	V_{SS}	61	V_{SS}	113	CK0#	165	DQ48	10	DQS0#	62	DQS3	114	ERROUT#	166	DQ52
11	DM0	63	DQ26	115	V_{DD}	167	DQ49	12	DQS0	64	V_{SS}	116	V_{DD}	168	DQ53
13	DQ2	65	DQ27	117	A10/AP	169	V_{SS}	14	V_{SS}	66	DQ30	118	S3#	170	V_{SS}
15	DQ3	67	V_{SS}	119	BA0	171	DQS6#	16	DQ6	68	DQ31	120	S2#	172	DM6
17	V_{SS}	69	CB0	121	WE#	173	DQS6	18	DQ7	70	V_{SS}	122	RAS#	174	DQ54
19	DQ8	71	CB1	123	V_{DD}	175	V_{SS}	20	V_{SS}	72	CB4	124	V_{DD}	176	DQ55
21	DQ9	73	V_{SS}	125	CAS#	177	DQ50	22	DQ12	74	CB5	126	ODT0	178	V_{SS}
23	V_{SS}	75	DQS8#	127	S0#	179	DQ51	24	DQ13	76	DM8	128	ODT1	180	DQ60
25	DQS1#	77	DQS8	129	S1#	181	V_{SS}	26	V_{SS}	78	V_{SS}	130	A13	182	DQ61
27	DQS1	79	V_{SS}	131	V_{DD}	183	DQ56	28	DM1	80	CB6	132	V_{DD}	184	V_{SS}
29	V_{SS}	81	CB2	133	DQ32	185	DQ57	30	RESET#	82	CB7	134	DQ36	186	DQS7#
31	DQ10	83	CB3	135	DQ33	187	V_{SS}	32	V_{SS}	84	V_{REFCA}	136	DQ37	188	DQS7
33	DQ11	85	V_{DD}	137	V_{SS}	189	DM7	34	DQ14	86	V_{DD}	138	V_{SS}	190	V_{SS}
35	V_{SS}	87	CKE0	139	DQS4#	191	DQ58	36	DQ15	88	A15	140	DM4	192	DQ62
37	DQ16	89	CKE1	141	DQS4	193	DQ59	38	V_{SS}	90	A14	142	DQ38	194	DQ63
39	DQ17	91	BA2	143	V_{SS}	195	V_{SS}	40	DQ20	92	A9	144	DQ39	196	V_{SS}
41	V_{SS}	93	V_{DD}	145	DQ34	197	SA0	42	DQ21	94	V_{DD}	146	V_{SS}	198	EVENT#
43	DQS2#	95	A12	147	DQ35	199	V_{DDSPD}	44	DM2	96	A11	148	DQ44	200	SDA
45	DQS2	97	A8	149	V_{SS}	201	SA1	46	V_{SS}	98	A7	150	DQ45	202	SCL
47	V_{SS}	99	A5	151	DQ40	203	V_{TT}	48	DQ22	100	A6	152	V_{SS}	204	V_{TT}
49	DQ18	101	V_{DD}	153	DQ41	–	–	50	DQ23	102	V_{DD}	154	DQS5#	–	–
51	DQ19	103	A3	155	V_{SS}	–	–	52	V_{SS}	104	A4	156	DQS5	–	–

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

DQ Map

Table 6: Component-to-Module DQ Map, Front

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	13	U2	0	22	48
	1	1	7		1	21	42
	2	3	15		2	23	50
	3	0	5		3	20	40
	4	6	16		4	18	49
	5	4	4		5	16	37
	6	7	18		6	19	51
	7	5	6		7	17	39
U5	0	38	142	U6	0	54	174
	1	37	136		1	53	168
	2	39	144		2	50	177
	3	33	135		3	49	167
	4	34	145		4	55	176
	5	32	133		5	48	165
	6	35	147		6	51	179
	7	36	134		7	52	166
U7	0	13	24	U8	0	25	57
	1	11	33		1	27	65
	2	12	22		2	29	56
	3	15	36		3	31	68
	4	8	19		4	28	54
	5	14	34		5	30	66
	6	9	21		6	24	55
	7	10	31		7	26	63
U9	0	CB1	71	U10	0	41	153
	1	CB6	80		1	46	160
	2	CB5	74		2	45	150
	3	CB2	81		3	47	162
	4	CB0	69		4	44	148
	5	CB3	83		5	43	161
	6	CB4	72		6	40	151
	7	CB7	82		7	42	159

Table 6: Component-to-Module DQ Map, Front (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	57	185				
	1	62	192				
	2	61	182				
	3	63	194				
	4	60	180				
	5	59	193				
	6	56	183				
	7	58	191				

Table 7: Component-to-Module DQ Map, Back

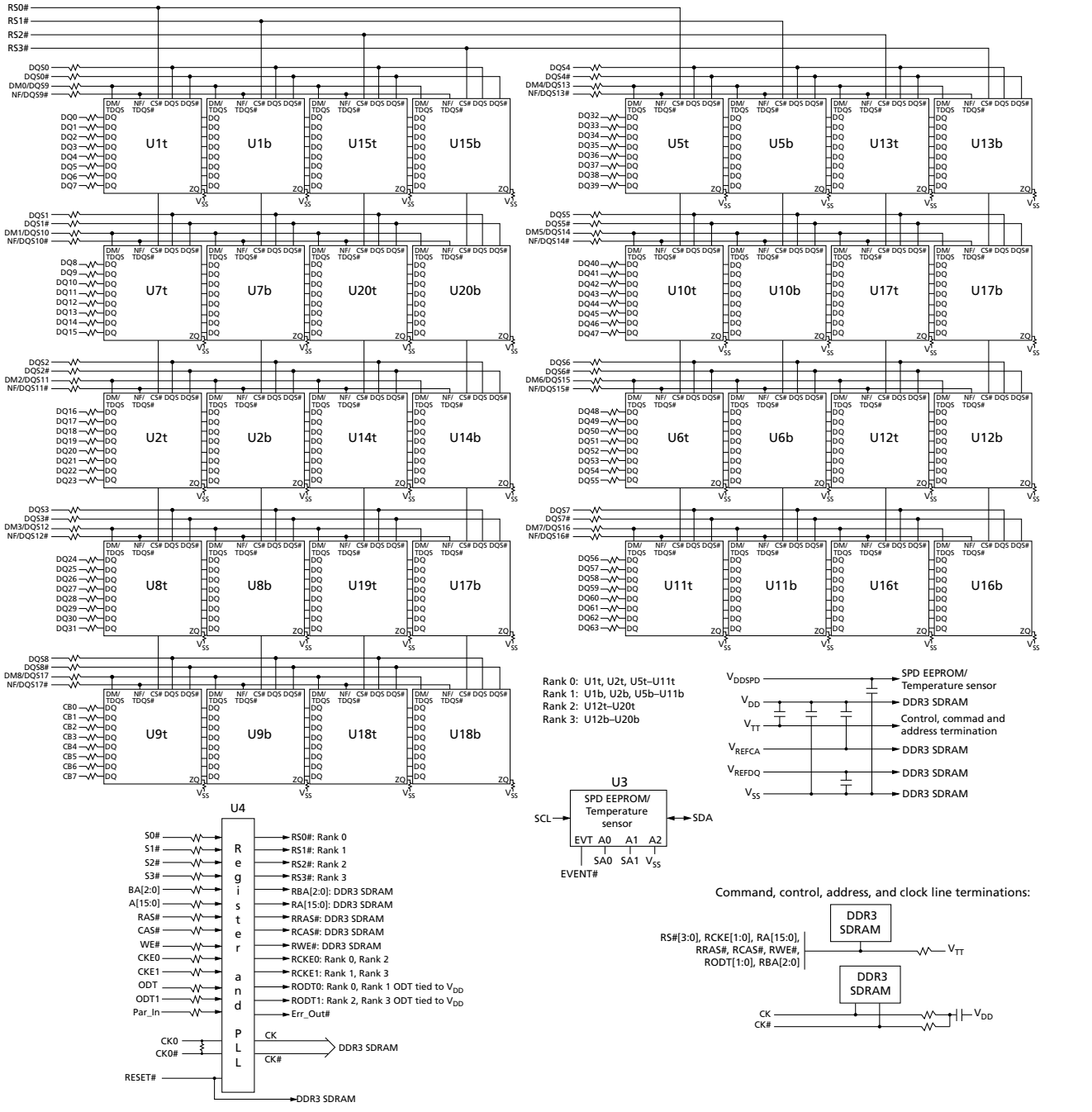
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U12	0	53	168	U13	0	37	136
	1	54	174		1	38	142
	2	49	167		2	33	135
	3	50	177		3	39	144
	4	52	166		4	36	134
	5	51	179		5	35	147
	6	48	165		6	32	133
	7	55	176		7	34	145
U14	0	21	42	U15	0	1	7
	1	22	48		1	2	13
	2	20	40		2	0	5
	3	23	50		3	3	15
	4	17	39		4	5	6
	5	19	51		5	7	18
	6	16	37		6	4	4
	7	18	49		7	6	16

Table 7: Component-to-Module DQ Map, Back (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U16	0	62	192	U17	0	46	160
	1	57	185		1	41	153
	2	63	194		2	47	162
	3	61	182		3	45	150
	4	58	191		4	42	159
	5	56	183		5	40	151
	6	59	193		6	43	161
	7	60	180		7	44	148
U18	0	CB6	80	U19	0	27	65
	1	CB1	71		1	25	57
	2	CB2	81		2	31	68
	3	CB5	74		3	29	56
	4	CB7	82		4	26	63
	5	CB4	72		5	24	55
	6	CB3	83		6	30	66
	7	CB0	69		7	28	54
U20	0	11	33				
	1	13	24				
	2	15	36				
	3	12	22				
	4	10	31				
	5	9	21				
	6	14	34				
	7	8	19				

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC standard "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver includes an even parity function for checking parity. The memory controller accepts a parity bit at the Par_In input and compares it with the data received on A[15:0], BA[2:0], RAS#, CAS#, and WE#. Valid parity is defined as an even number of ones (1s) across the address and command inputs (A[15:0], BA[2:0], RAS#, CAS#, and WE#) combined with Par_In. Parity errors are flagged on Err_Out#.

Address and command parity is checked during all DRAM operations and during control word WRITE operations to the registering clock driver. For SDRAM operations, the address is still propagated to the SDRAM even when there is a parity error. When writing to the internal control words of the registering clock driver, the write will be ignored if parity is not valid. For this reason, systems must connect the Par_In pins on the DIMM and provide correct parity when writing to the registering clock driver control word configuration registers.

Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I^2C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.283	1.35	1.45	V	
			1.425	1.5	1.575	V	1
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{VTT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	2
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	–	–	–	µA	3
		DM	–8	0	8		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–20	0	20	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V)		–36	0	36	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	4, 5
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	4, 5, 6

Notes:
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
2. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
3. Inputs are terminated to V_{DD}/2. Input current is dependent on terminating resistance selected in register.
4. T_A and T_C are simultaneous requirements.
5. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

6. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

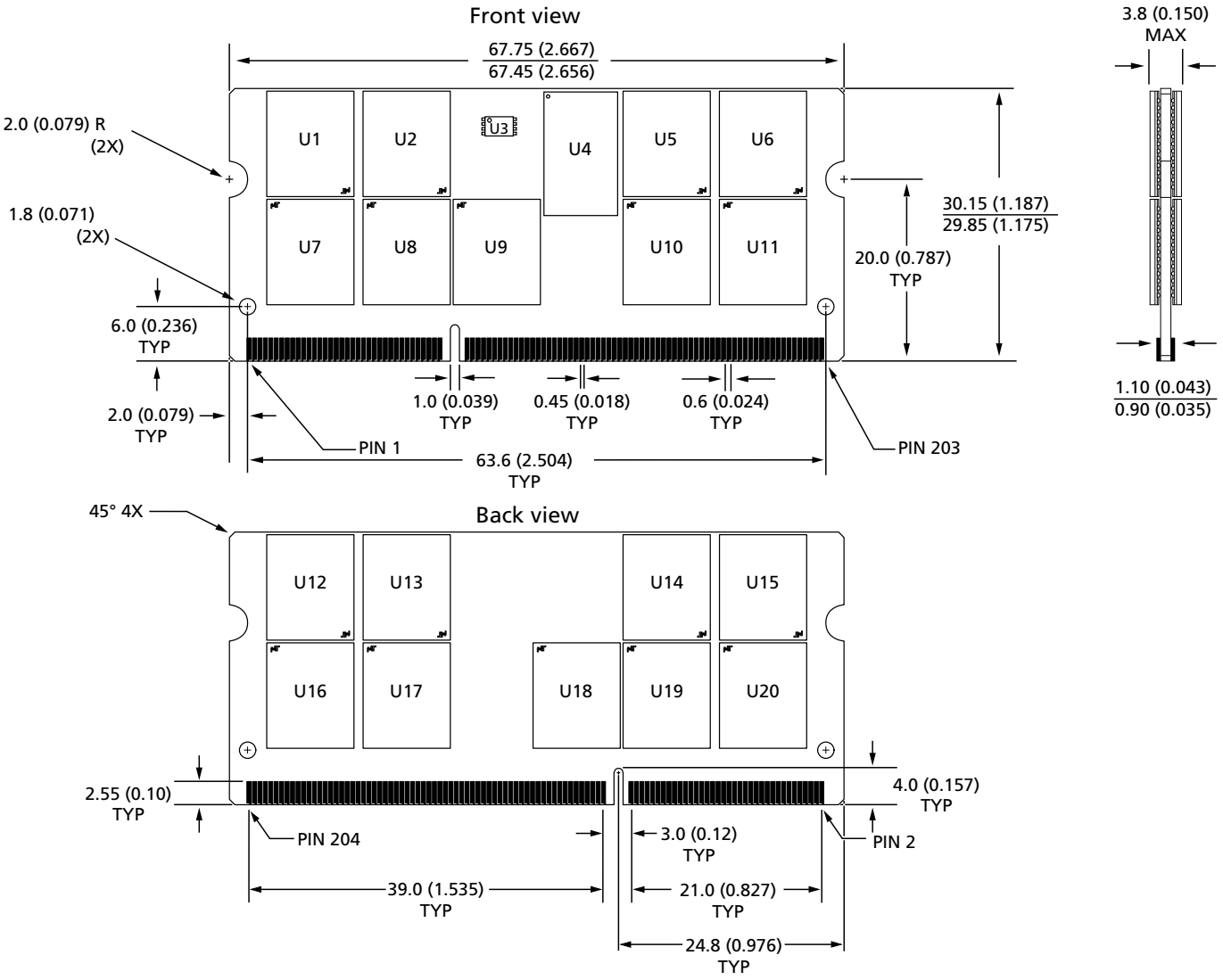
Table 11: DDR3 I_{DD} Specifications and Conditions – 16GB (Die Revision E)

Values are for the MT41K1G8 DDR3L SDRAM only and are computed from values specified in the 1.35V TwinDie 8Gb component data sheet

Parameter	Combined Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{CDD0}	1152	1053	1017	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{CDD1}	1251	1188	1152	mA
Precharge power-down current: Slow exit	I_{CDD2P0}	648	648	648	mA
Precharge power-down current: Fast exit	I_{CDD2P1}	774	738	720	mA
Precharge quiet standby current	I_{CDD2Q}	900	828	810	mA
Precharge standby current	I_{CDD2N}	900	846	828	mA
Precharge standby ODT current	I_{CDD2NT}	1026	954	900	mA
Active power-down current	I_{CDD3P}	1395	1260	1152	mA
Active standby current	I_{CDD3N}	1008	954	900	mA
Burst read operating current	I_{CDD4R}	2070	1890	1728	mA
Burst write operating current	I_{CDD4W}	1782	1620	1476	mA
Refresh current	I_{CDD5B}	2727	2637	2592	mA
Self refresh temperature current: MAX T_C = 85°C	I_{CDD6}	720	720	720	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{CDD6ET}	900	900	900	mA
All banks interleaved read current	I_{CDD7}	2637	2340	2061	mA
Reset current	I_{CDD8}	720	720	720	mA

Module Dimensions

Figure 3: 204-Pin DDR3 SODIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.