August 16, 2010

CP2501-B01 Errata

Errata Status Summary

Errata #	Title	Impact	Status	
			Affected Revisions	Fixed Revision
1	Configuring 48 MHz Operation	Minor	CP2501-B01-GM	

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description**: When configuring the device for 48 MHz operation using the System Firmware API, the System Firmware does not set the Flash timing correctly to account for the higher system clock speed.

   Impact: The device can behave unpredictably if the Flash timing is incorrect. The problem is more likely to occur at higher temperatures.

   Workaround: Set the Flash timing manually before calling CP250x_System_Init() to configure the system clock to 48 MHz:

```
// Add the following to CP250x.h
SFR (FLSCL, 0xB6);                          // Flash Timing Register

// Add the following to CP250x_Main.c
FLSCL |= 0x10;                              // Set Flash Timing
CP250x_System_Init (BUS_POW, OSC_48);       // Configure System Clock
```

   Resolution: The CP2501-B02-GM System Firmware will set the Flash timing correctly for 48 MHz operation.