

## PIC18FXX39 Rev. B5 Silicon Errata Sheet

The PIC18FXX39 Rev. B5 parts you have received conform functionally to the Device Data Sheet (DS30485A), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18FXX39 silicon.

### 1. Module: Program Memory

Data corruption may occur during a Table Write operation if a peripheral interrupt also occurs. This happens only when the interrupt enable bit (PIE or INTCON register) for the corresponding interrupt has also been set.

#### Work around

Before executing any Table Write instructions, disable ALL peripheral interrupts. This is best done by clearing all Interrupt Enable bits in the three Interrupt Control registers (INTCON, INTCON2 and INTCON3) and both Peripheral Interrupt Enable registers (PIE1 and PIE2). After the Table Write is complete, restore all INTCON and PIE registers to their pre-instruction state.

#### Date Codes that pertain to this issue:

All engineering and production devices.

### 2. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may become corrupted in the second instruction cycle after the RD bit (EECON1<0>) is set. The actual contents of the EEPROM remains unaffected.

#### Work around

To ensure the integrity of the contents of EEDATA, the register must be read in the instruction immediately following the setting of the RD bit. Use the `movf` or `movff` instructions to do this (see Example 1).

Additionally, all interrupts must be disabled prior to the read instruction sequence. Interruptions of the sequence may have the same result of altering the contents of EEDATA.

#### EXAMPLE 1: SUGGESTED SEQUENCE FOR READING EEDATA

```

:
:
bcf    INTCON,GIEH ;disable interrupts
                ;if using interrupts
bsf    EECON1,RD  ;start the read operation
movf   EEDATA,W   ;move the data out of
                ;EEDATA
bsf    INTCON,GIEH ;enable interrupts
                ;if using interrupts
:
:

```

#### Date Codes that pertain to this issue:

All engineering and production devices.

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## 3. Module: Core (Program Memory Space)

Performing Table Read operations above the user Program Memory space (addresses over 1FFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFh, including the User ID locations (200000h - 200007h), the configuration bytes (300000h - 30000Dh), and the Device ID locations (3FFFFEh and 3FFFFFFh). User program memory is unaffected.

### **Work around**

Three possible work arounds are presented. Other solutions may exist.

1. Do not perform Table Read operations on areas above the User Memory Space at -40°C.
2. Insert NOP instructions (specifically, literal FFFFh) around any Table Read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each Table Read. This may vary, depending upon the particular application, and should be optimized by the user.

Date Codes that pertain to this issue:

All engineering and production devices.

## 4. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the RD bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

### **Work around**

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the RD bit. The instruction between the write to EEADR and the read can be any valid instruction, including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30485A), the following clarifications and corrections should be noted.

None.

## REVISION HISTORY

Rev A Document (12/2002)

First revision of this document. Silicon issues 1 through 4 (Program Memory, Data EEPROM and Core - Program Memory Space).

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NOTES:

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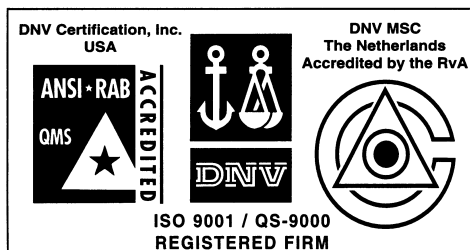
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