General description

DA7202 is a powerful, high efficiency, low EMI Class-D speaker driver that can drive 10 W into 4 Ω loads directly from a 2S lithium ion battery pack.

DA7202 is a standalone high performance mono Class-D audio amplifier targeted at powering a variety of two cell portable applications such as Ultrabooks™ and tablets.

It uses a fully-differential switched mode amplifier architecture with a fixed +18 dB gain, with differential analogue inputs. It also has a PWM modulator and an H-bridged switched power output stage that delivers 8 W into an 8 Ω load, making a speaker sound louder on portable devices.

The DA7202 can be directly connected between the two-cell battery and the speaker. Noise suppression circuitry to reduce audible pops and clicks at the speaker output is also included.

Available as a 9-bump WL-CSP package with 0.5 mm pitch that is suited to low cost PCB technology, it is ideal for portable applications that require small footprints.

Key features

- PRMS: 3.8 W into 8 Ω load at 8.2 V, 1% THD+N
- Efficiency: 90% @ P_{OUT} = 3.5 W at 8.2 V, 8 Ω and 85%@P_{OUT} = 7.0 W at 8.2 V, 4 Ω
- Supports 4 Ω and 8 Ω loads
- SNR (A-weighted) 104 dB
- THD+N: 90 dB @ 3.0 W, 8.2 V, 8 Ω
- PSRR: 78 dB
- Auto-Shutdown/Start-up: <3.5 ms
- Ultra low standby current: 7 µA
- Short-Circuit & Thermal-Overload Protection with auto recovery
- Wide supply voltage range 4.5 to 9.0 V
- 9-bump WL-CSP with 0.5 mm pitch
- 2S battery pack

Applications

- Tablets
- Personal navigation devices
- Ultrabooks™
- Speaker accessories
- Handheld gaming devices

Contents

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Tables

1 Terms and definitions

EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FCC	Federal Communications Commission
LDO	Low Dropout regulator
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion plus Noise
WL-CSP	Wafer Level-Chip Scale Packaging

2 Block diagram

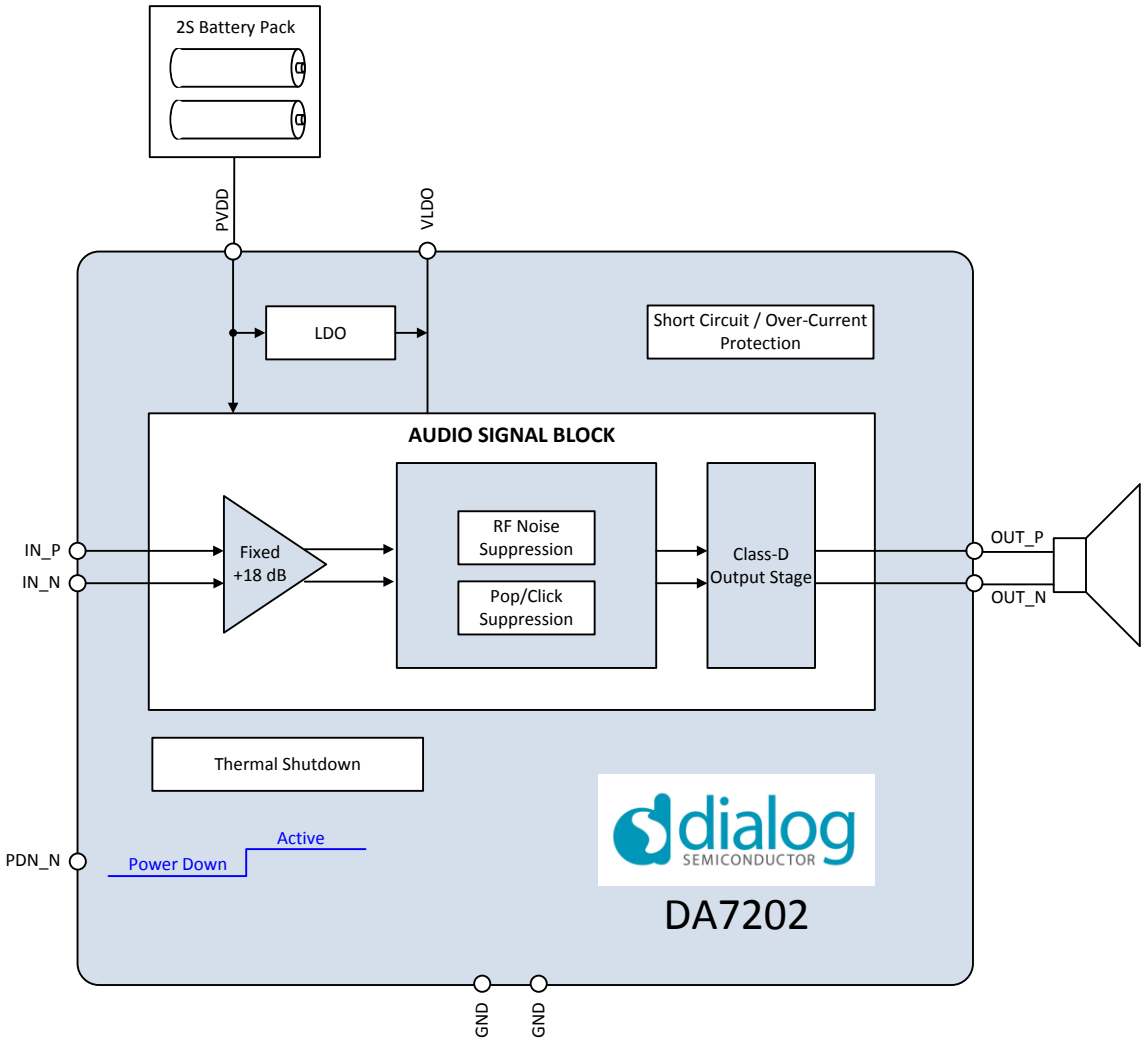

Figure 1: DA7202 block diagram

3 Pinout

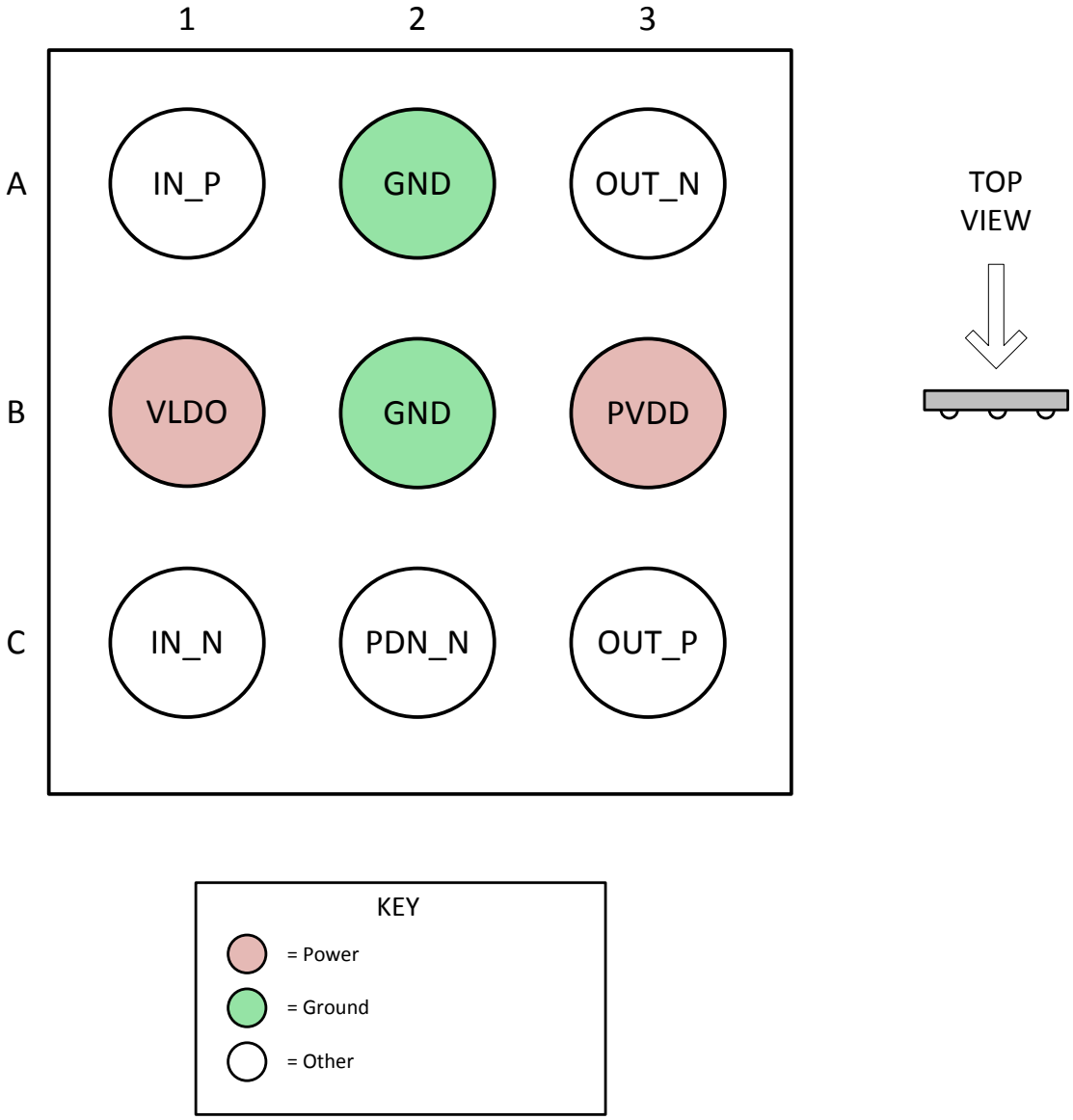

Figure 2: Connection diagram

Table 1: Pin description

Pin no.	Pin name	Description
A1	IN_P	Positive Analogue Input
A2	GND	Ground
A3	OUT_N	Negative Output
B1	VLDO	Output voltage from LDO
B2	GND	Ground
B3	PVDD	Power Supply
C1	IN_N	Negative Analogue Input
C2	PDN_N	Power Down Control (0 = Power Down / 1 = Active)
C3	OUT_P	Positive Output

4 Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
	Storage temperature		-65		+85	°C
	Operating temperature		-45		+85	°C
	Junction temperature (T_J)				+150	°C
PVDD	Supply voltage		+4.5	+8.2	+10.0	V
VLDO				+5.0		V
PDN_N	Power down control		-0.3		+5.0 (VLDO)	V
	ESD susceptibility	Human body model			2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended operating conditions

Table 3: Recommended operating conditions

V_{DD} = 8.2 V, T_A = 25°C, R_L = 8 Ω +33 µH, unless otherwise noted.

Parameter	Description	Conditions	Min	Typ	Max	Unit
PVDD	Supply voltage		4.5		9.0	V
VLDO		Output		5.0		V
				30		kΩ
			18			µH
P_{RMS}	Output power	R_{LOAD} = 8 Ω V_{PWR} = 8.2 V THD+N = 1%		3.8		W
$P_{MPO\ (RMS)}$		R_{LOAD} = 8 Ω V_{PWR} = 8.2 V THD+N = 1%			7.6	W
P_{RMS}		R_{LOAD} = 4 Ω V_{PWR} = 8.2 V THD+N = 1%		8.0		W
$P_{MPO\ (RMS)}$		R_{LOAD} = 4 Ω V_{PWR} = 8.2 V THD+N = 1%			10.0	W
	Efficiency	P_{OUT} = 3.5 W R_{LOAD} = 8 Ω + 18 µH audio = 1 kHz			90	%
	THD+N	P_{OUT} = 3.0 W, 8 Ω, 8.2 V		90		dB
	SNR			104		dB
	PSRR (AC grounded)	Frequency = 217 Hz		78		dB
	Gain	Fixed		18		dB
	Output switching frequency	Fixed		1		MHz
	Output Noise (RMS)	Integrated over bandwidth SNR = 99 dB, Gain = 18 dB			60	µV
	Standby current consumption at Shutdown			7		µA

6 Electrical characteristics

Table 4: Digital inputs (PDN_N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input-Voltage High		1.3		+5 (VLDO)	V
V_{IL}	Input-Voltage Low		0		0.7	V
	Input Hysteresis			0.4		V
I_{IH}	Input High Leakage current	V_{IN}=5 V, T_A=25°C			25	µA
I_{IL}	Input Low Leakage current	V_{IN}=GND, T_A=25°C			0.1	µA

Note 2 V_{IH} and V_{IL} define logic levels to enable or disable the DA7202.

Table 5: Analog inputs (IN_P, IN_N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Audio input signal				+5.0	V

7 Thermal protection

Monitoring of the ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

The junction temperature of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). An estimation of the junction temperature (T_J) can be calculated using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

- T_J = junction temperature
- T_A = ambient temperature of the package (°C)
- P_D = power dissipation of the package (W)
- θ_{JA} = junction to ambient thermal resistance (°C / W) = 72°C/W

The value of θ_{JA} can vary, depending on PCB material, the layout, and the environmental conditions. The specified value of θ_{JA} (72°C/W) is based on a 4-layer, 101.5 mm x 114.5 mm circuit board as specified in the JEDEC standard JESD51-9.

Table 6: Thermal protection

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Thermal Shutdown Threshold			150		°C
	Thermal Shutdown Restart Threshold			100		°C
	Thermal Shutdown Hysteresis			50		°C
θ_{JA}	Junction to ambient thermal resistance			72		°C/W

8 Functional description

The DA7202 is a powerful, high efficiency, low EMI Class-D speaker driver that can drive a maximum of 10 W into 4 Ω loads directly from a 2S lithium ion battery pack.

The device provides audio noise and RF noise suppression. It also has short circuit protection, as well as protection against over-heating.

The DA7202 is available in a 9-bump WL-CSP package with 0.5 mm pitch that enables low cost PCB technology which is ideal for portable applications that require small footprints.

8.1 Pop and click suppression

DA7202 includes noise suppression circuitry that reduces audible pops and clicks at the speaker output when enabling or disabling the device.

8.2 Short circuit/over-current protection

The DA7202 is protected by a short circuit/over current detector. If a short circuit is detected, regardless of the frequency of the signal, the device is disabled immediately. After 8 ms, the short-circuit status is checked. If the short condition has been resolved, the chip will be re-enabled. If the short condition still persists, the DA7202 remains disabled. The short-circuit status is checked every 8 ms until the short condition has been resolved. The chip will then be re-enabled.

Note that the disabling of the chip, and its later re-enabling, are both performed without using the noise suppression circuitry. Audible artefacts may be present in the output signal.

Note also that whenever the DA7202 has been powered down, the power stage is placed in a high impedance (high-Z) state to minimise power consumption.

8.3 Thermal performance and thermal protection

8.3.1 Thermal shutdown

DA7202 is provided with a thermal protection feature that automatically disables the power stage and the LDO if the junction temperature reaches 150°C.

When a thermal shutdown is performed, the chip is disabled, leaving only the temperature sensor block active. The process of disabling the chip is performed using the noise suppression circuitry, so no audible artefacts will be present on the output signal during the disabling process. The time taken for a noise free shutdown is illustrated in Figure 16.

If thermal shutdown is activated, the chip is not re-enabled until the temperature has dropped to 100°C. Once the temperature has reached 100°C, the DA7202 restarts with an automatic soft start. The process of re enabling the chip is performed using the noise suppression circuitry, so no audible artefacts will be present on the output signal during start-up process. The time taken for a noise free start-up is illustrated in Figure 15.

Note that whenever the DA7202 has been powered down, the power stage is placed in a high impedance (high-Z) state to minimise power consumption.

8.3.2 Maximum power dissipation

Given the Junction-to-Ambient thermal impedance (72°C/W), the Power Dissipation versus Output Power (from Figure 17 and Figure 18), and the maximum junction temperature ($T_{J(MAX)}$ specified in Table 6), it is possible to calculate the maximum ambient temperature ($T_{A(MAX)}$) using the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - \theta_{JA} \times P_{D(MAX)}$$

Up to an ambient temperature of 85°C, DA7202 can dissipate 0.56 W of heat before reaching 125°C.

Note that if the DA7202 is operated continuously at, or close to, its maximum output power, there is a risk of overheating and thermal shutdown unless steps are taken to dissipate this excess heat.

8.4 Gain

The DA7202 has a fixed gain of +18 dB.

Output volume is directly proportional to the input signal strength. It is assumed that any required variation in output volume will be controlled by varying the DA7202 input signal. The input signal amplitude can be reduced by the use of resistor dividers in conjunction with the known input impedance.

8.5 Class D output stage

The class D output stage is connected directly to the PVDD (two cell battery pack) power supply. High-efficiency operation is achieved by operating the output transistors as switches. The output power transistors are either fully On or fully Off, providing a minimum resistance path for current from the power supply to the load. The block's outputs are connected directly to the speaker at OUT_P and OUT_N.

Filterless operation is achieved by connecting a load (a speaker) between the output terminals of the Class D ouput block. As a result, the voltage across the load represents a PWM (Pulse Width Modulated) audio signal, while the output current in the load is a filtered, demodulated representation of the input audio signal.

For filterless operation, the speaker load can be considered as a first order output filter with a cut-off frequency well below the PWM carrier signal (the current in the load is a filtered version of the output PWM voltage signal). See section 10.2 for further detail on speaker selection.

8.6 Power down (PDN_N)

The DA7202 is powered down by pulling the PDN_N pin low. When the device is powered down, a controlled shutdown process is performed, thus ensuring that there are no audible artefacts (pops and clicks) on the output path.

The time to disable the device is illustrated in Figure 16.

Table 7: Actions of the PDN_N pin

PDN_N Value	Description
0	Power Down
1	Active

9 Typical performance plots

9.1 THD versus output power (8 Ω + 33 µH)

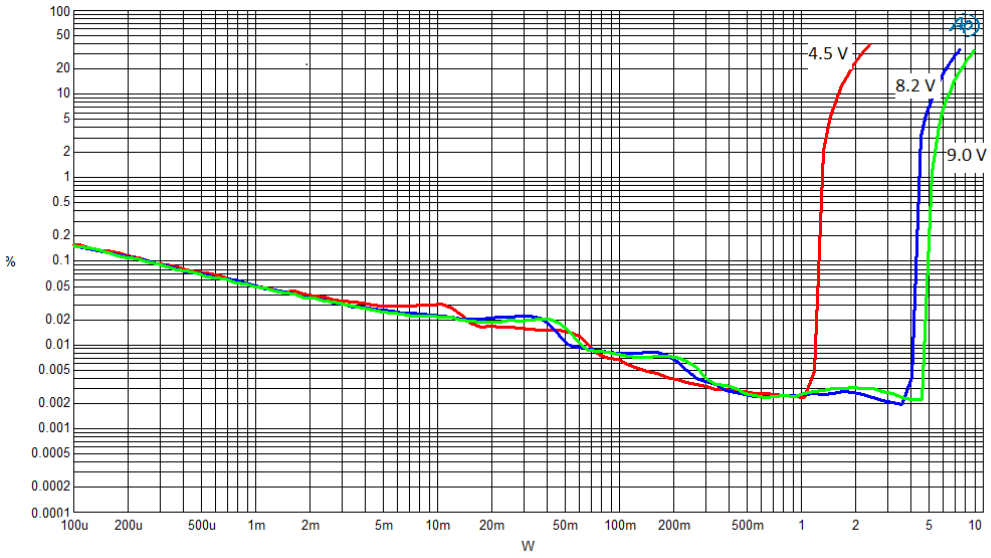

Figure 3: THD versus output power (8 Ω + 33 µH)

9.2 THD versus output power (4 Ω + 33 µH)

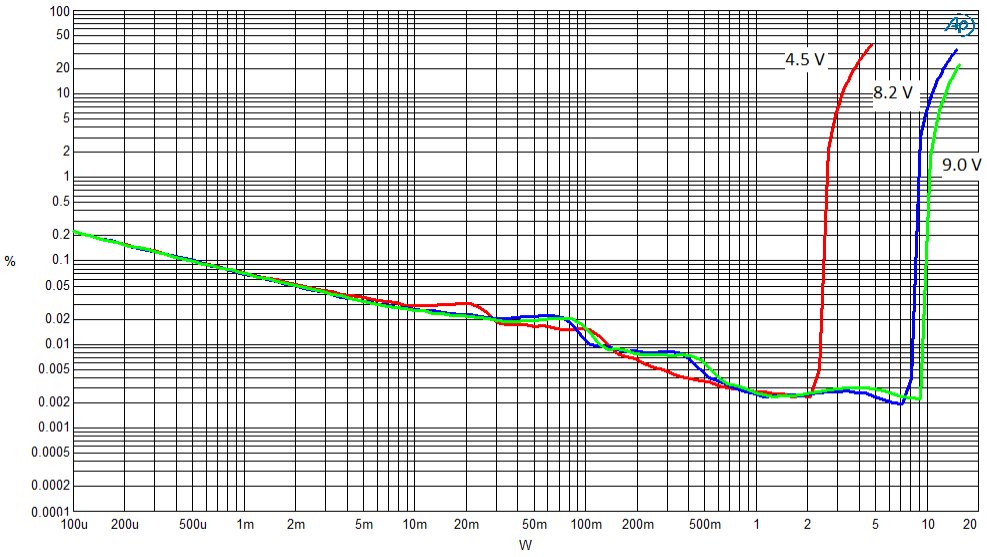

Figure 4: THD versus output power (4 Ω + 33 µH)

9.3 THD versus frequency (8 Ω + 33 µH) 4.5 V

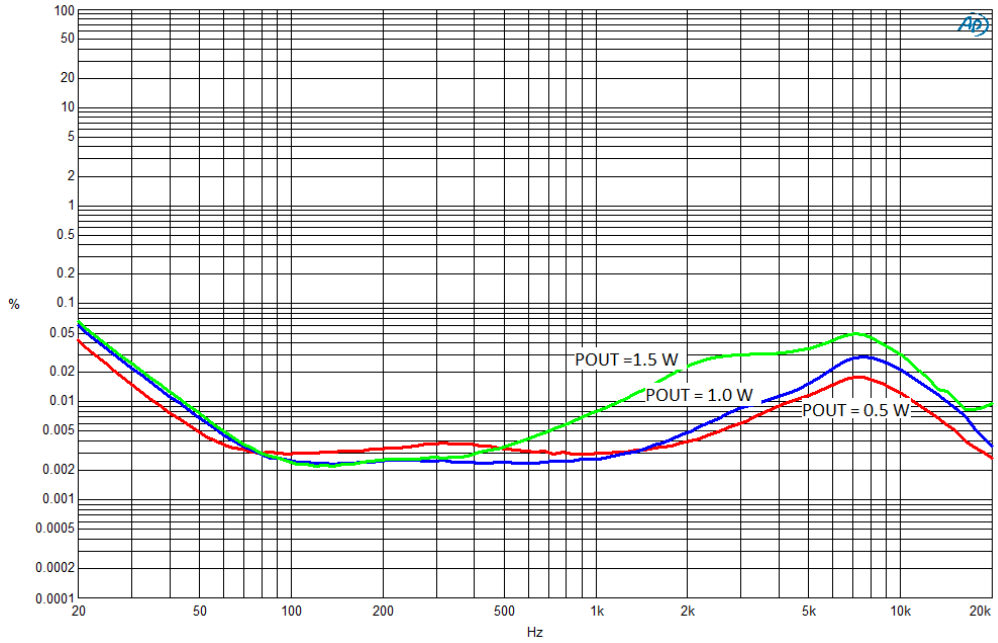

Figure 5: THD versus frequency (8 Ω + 33 µH) 4.5 V

9.4 THD versus frequency (4 Ω + 33 µH) 4.5 V

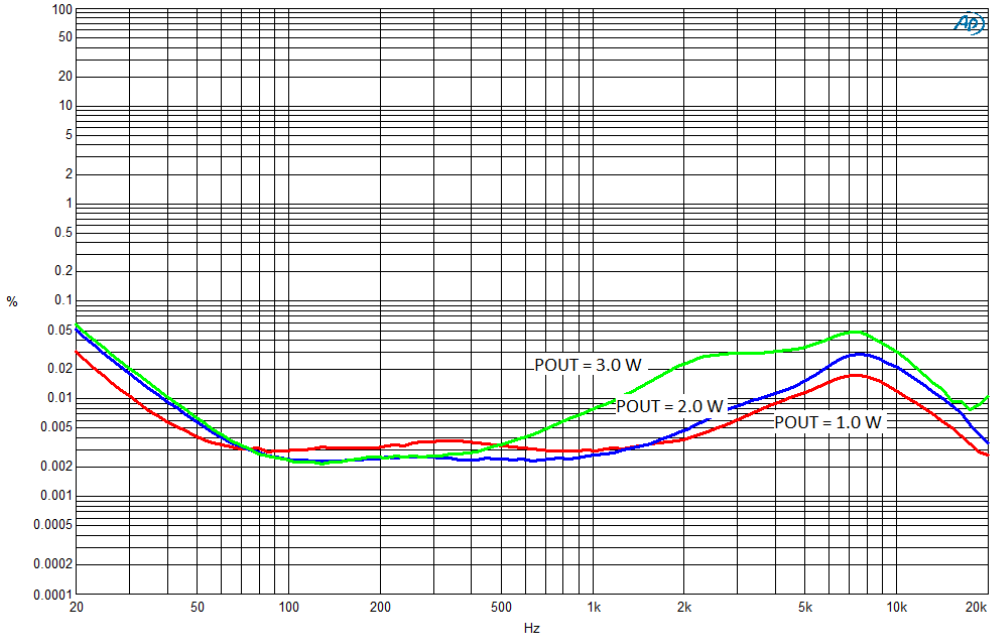

Figure 6: THD versus frequency (4 Ω + 33 µH) 4.5 V

9.5 THD versus frequency (8 Ω + 33 µH) 8.2 V

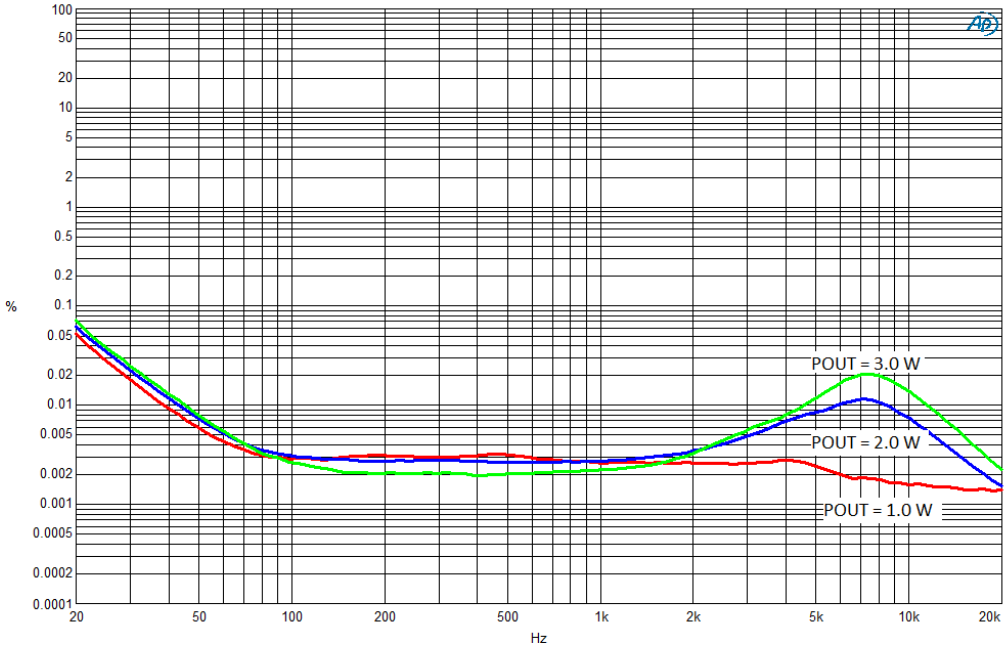

Figure 7: THD versus frequency (8 Ω + 33 µH) 8.2 V

9.6 THD versus frequency (4 Ω + 33 µH) 8.2 V

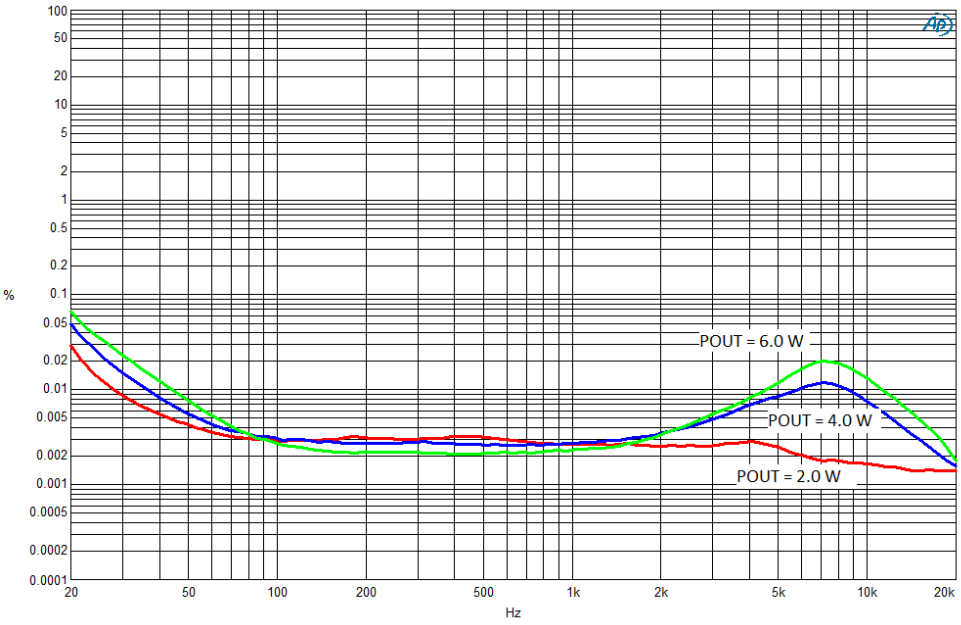

Figure 8: THD versus frequency (4 Ω + 33 µH) 8.2 V

9.7 THD versus frequency (8 Ω + 33 µH) 9.0 V

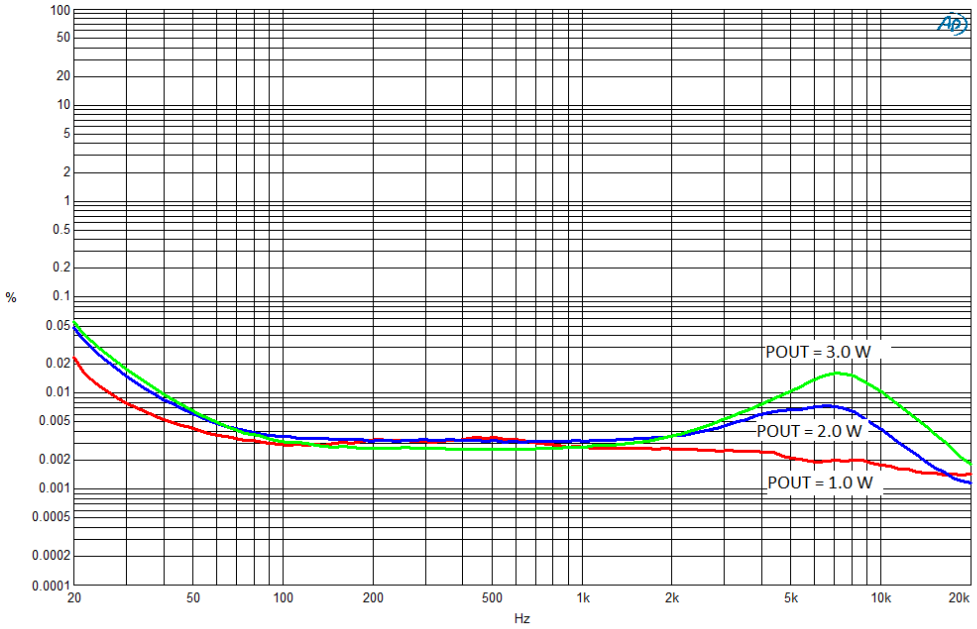

Figure 9: THD versus frequency (8 Ω + 33 µH) 9.0 V

9.8 THD versus frequency (4 Ω + 33 µH) 9.0 V

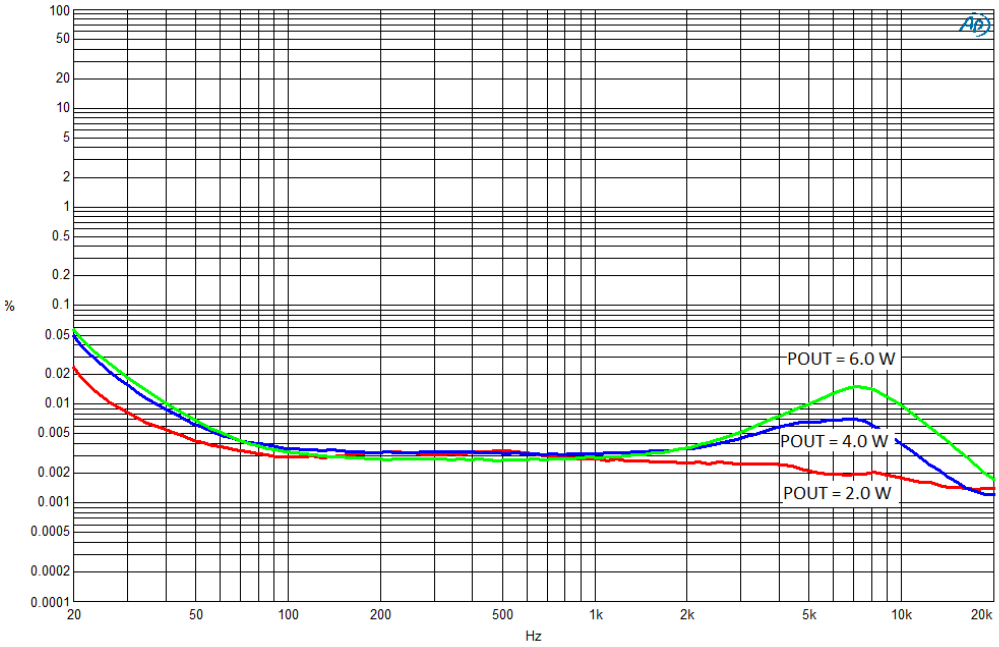

Figure 10: THD versus frequency (4 Ω + 33 µH) 9.0 V

9.9 Max P_{out} versus supply voltage (8 Ω + 33 µH)

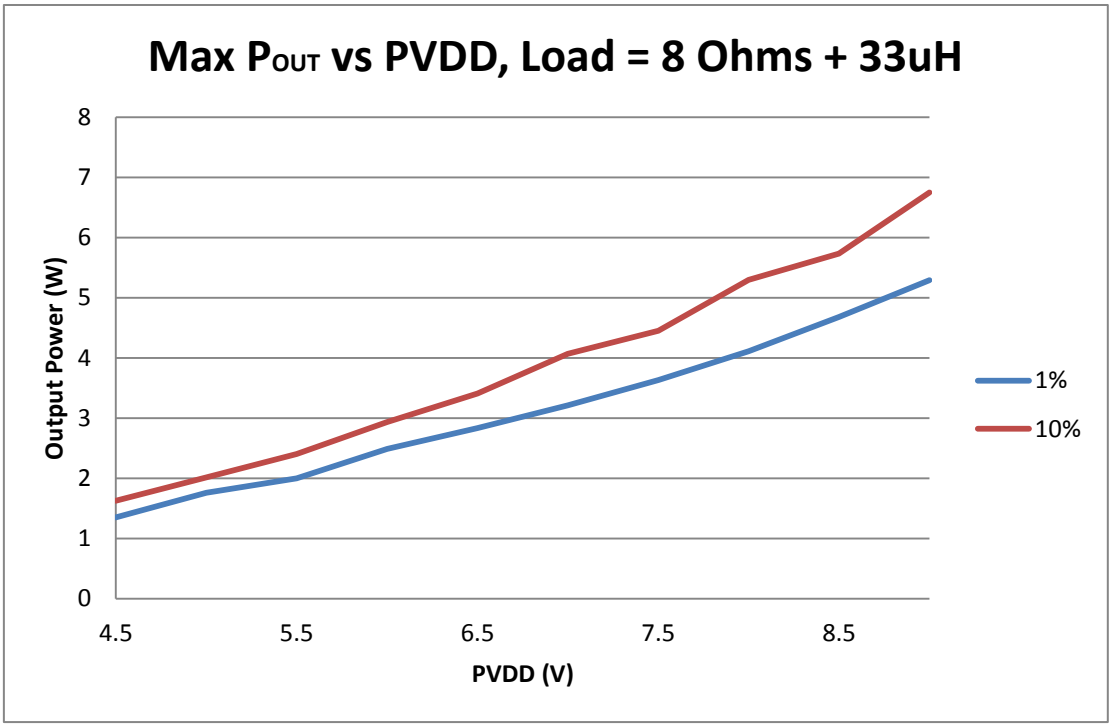

Figure 11: Maximum output power (P_{out}) versus supply voltage (8 Ω + 33 µH)

9.10 Max P_{out} versus supply voltage (4 Ω + 33 µH)

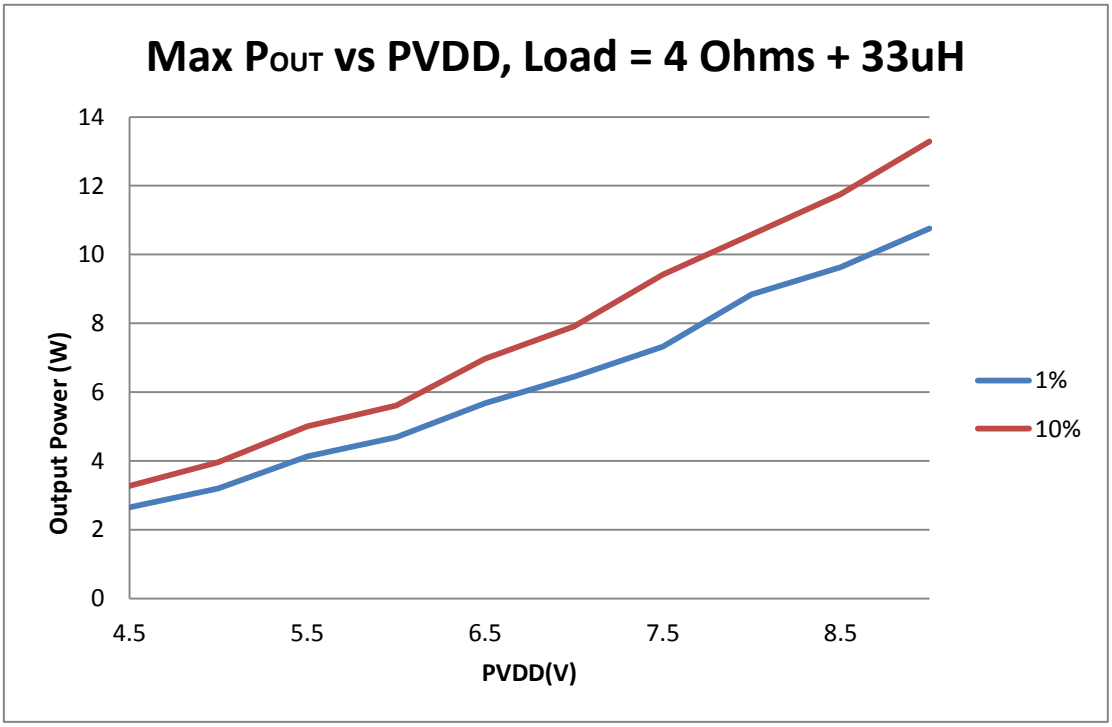

Figure 12: Maximum output power (P_{out}) versus supply voltage (4 Ω + 33 µH)

9.11 Efficiency versus output power (8 Ω + 33 µH)

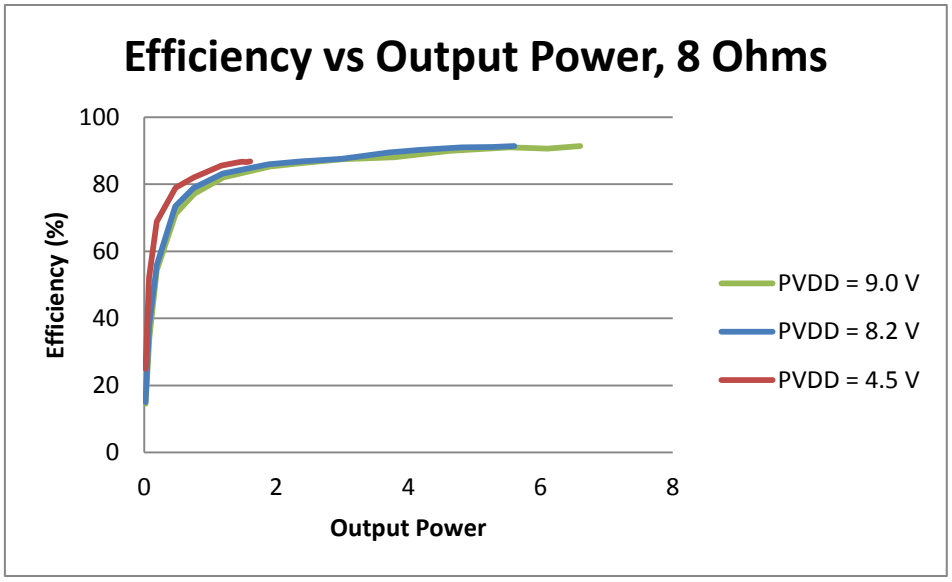

Figure 13: Efficiency versus output power (8 Ω + 33 µH)

9.12 Efficiency versus output power (4 Ω + 33 µH)

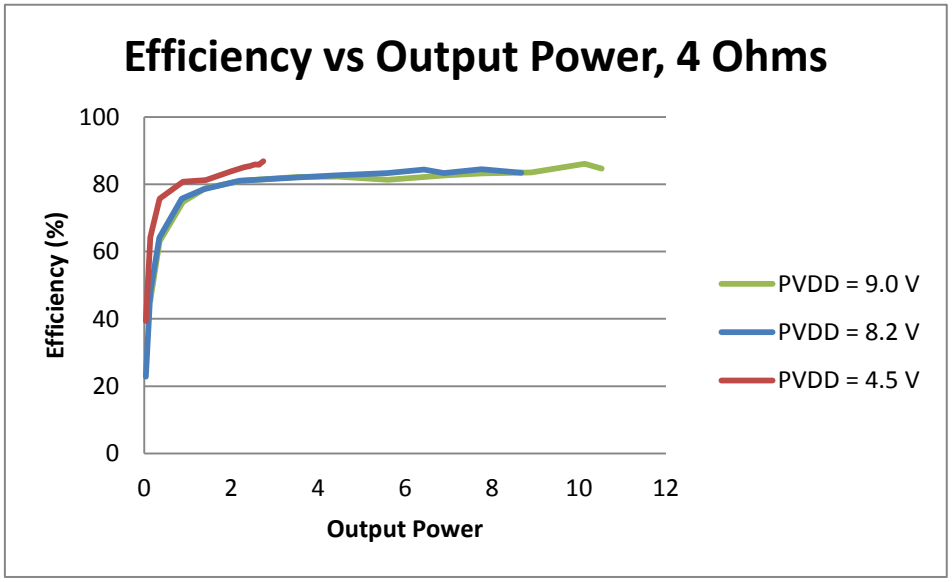

Figure 14: Efficiency versus output power (4 Ω + 33 µH)

9.13 Start-up timing

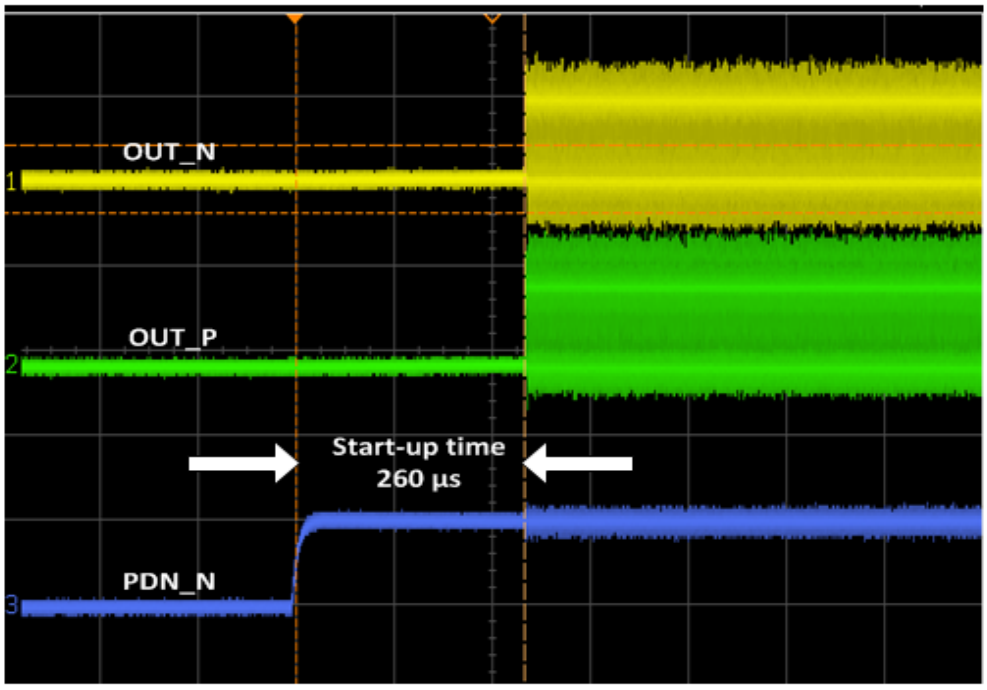

Figure 15: Start-up timing (260 µs from asserting PDN_N to valid output)

9.14 Shutdown timing

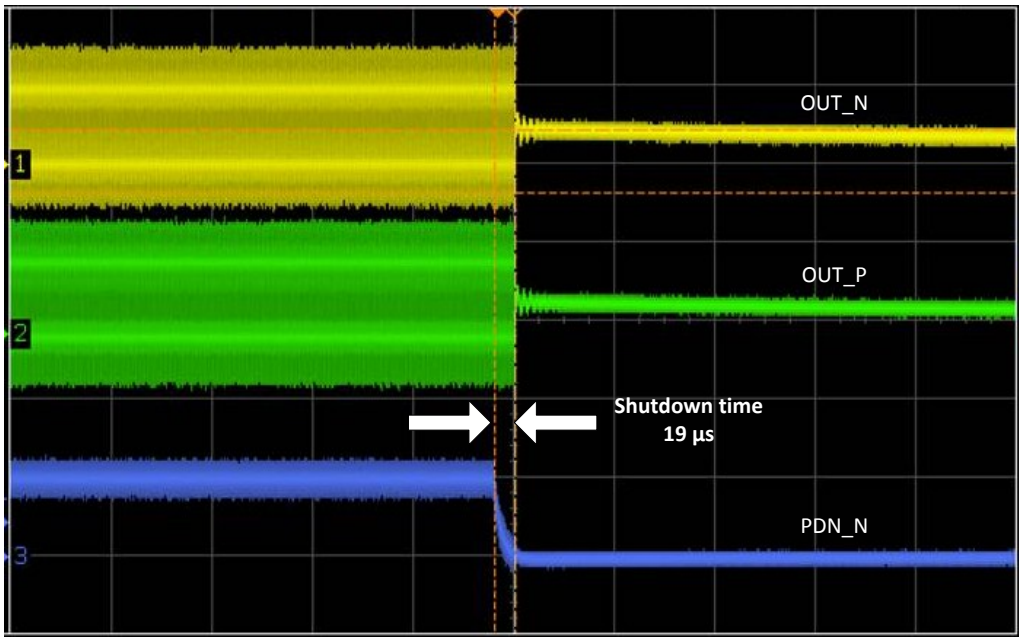

Figure 16: Shutdown timing (19 µs from de-asserting PDN_N to zero output)

9.15 Power dissipation versus output power (8 Ω + 33 µH)

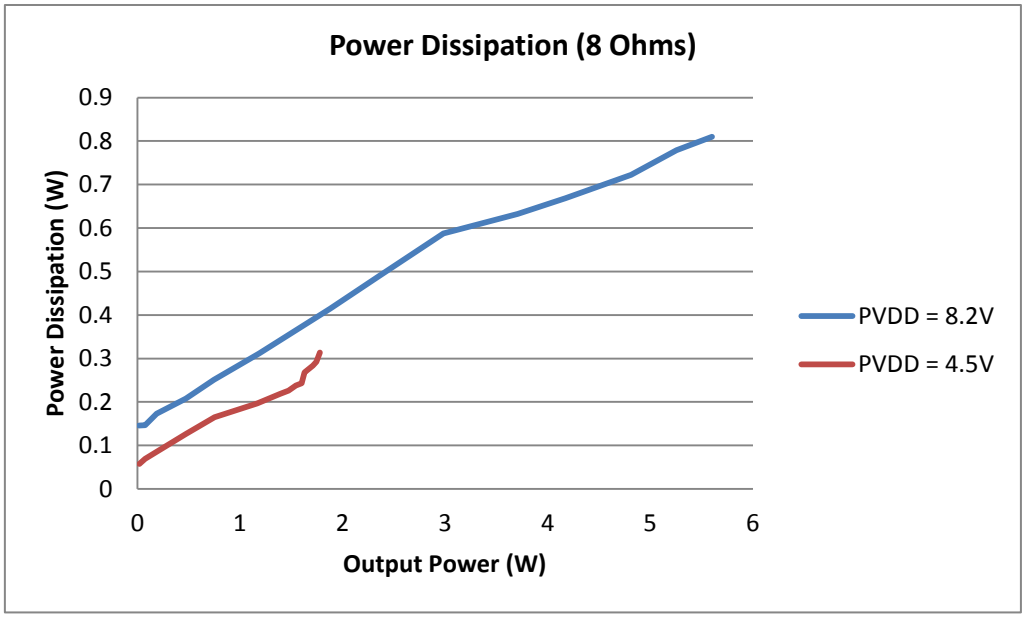

Figure 17: Power dissipation versus output power (8 Ω + 33 µH)

9.16 Power dissipation versus output power (4 Ω + 33 µH)

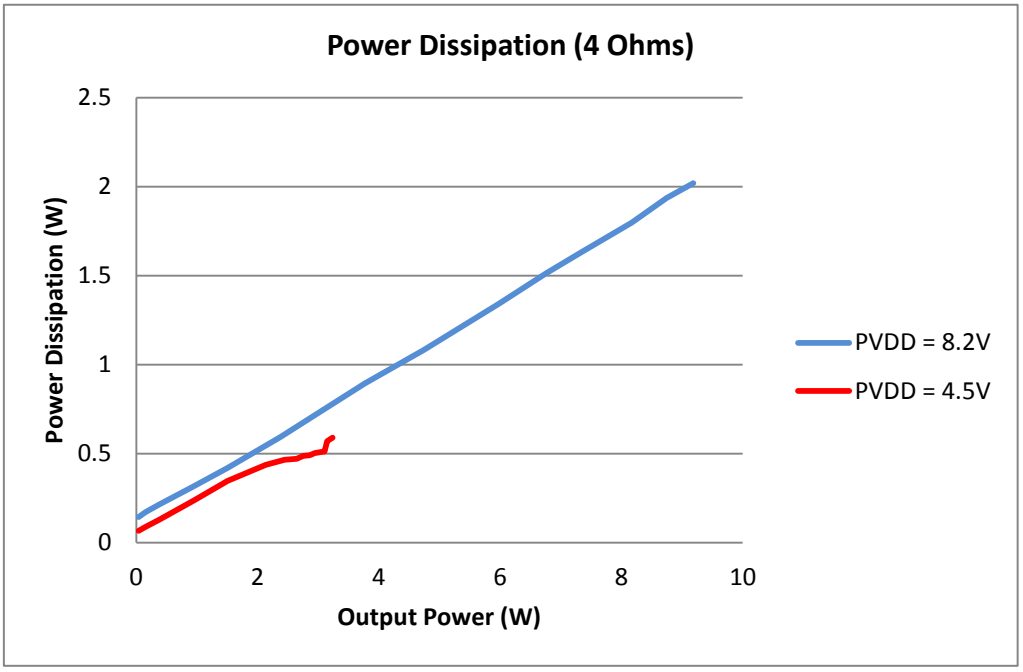

Figure 18: Power dissipation versus output power (4 Ω + 33 µH)

9.17 Electromagnetic interference (EMI) performance

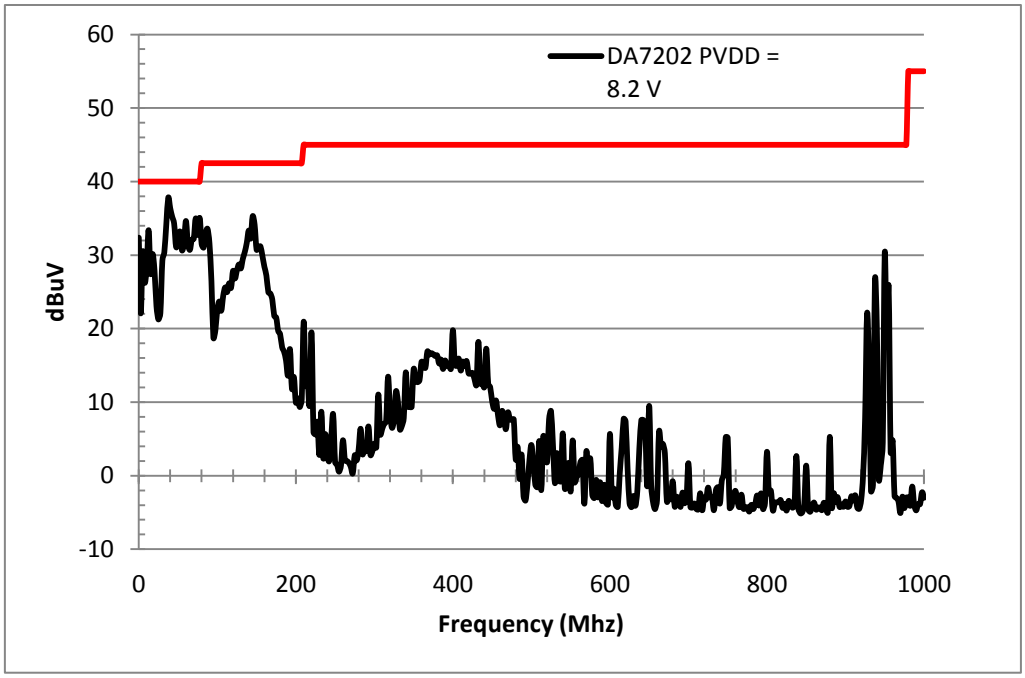

Figure 19: EMI performance with FCC Class-D limit also shown

Note 3 Measurements taken using a typical layout as illustrated in Figure 20 (speaker cable length = 12 cm).

10 Application information

10.1 PCB layout

The performance of the DA7202 relies on good PCB layout. Failure to follow best practice can have undesired side effects that include, but are not limited to, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. Dialog Semiconductor recommend that the following guidelines are followed:

- Place any input capacitors and output capacitors close to the device using short tracks. These components carry high switching frequencies, and long tracks can act as an antenna.
- Maximise the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- If external resistors are to be used to change the gain, these should be placed close to the device.
- It is recommended that ferrite beads are included on the output paths to reduce EMI interference and noise.

10.2 Speaker selection

The output from the DA7202 Class-D amplifier contains high frequency signals that are a result of its switched PWM operation. These high frequency harmonics are at a much higher frequency than is recommended for most speakers, so they must be filtered out to protect the speaker.

The correct choice of speaker is therefore important since the speaker itself can act as a low-pass filter, attenuating the undesirable high frequency harmonics while still passing the desired audio frequencies.

The 3 dB cut-off frequency for speaker inductance and resistance can be calculated using the following formula:

$$f_c = R_{LOAD} / 2\pi L$$

Therefore to achieve a 3 dB cut-off frequency of 20 kHz with an 8 Ω speaker, a speaker should be selected with an inductance of:

$$L = R_{LOAD} / 2\pi fc = 8\ \Omega / 2\pi * 20\ kHz = 64\ \mu H$$

8 Ω speakers for portable applications typically have an inductance in the range of 20 µH to 100 µH. Speakers with a higher inductance than the 64 µH calculated above will have a 3 dB cut-off frequency below 20 kHz, resulting in a reduced audio bandwidth. Conversely, speakers with an inductance lower than 64 µH will have a higher cut-off frequency.

10.3 Recommended external component layout

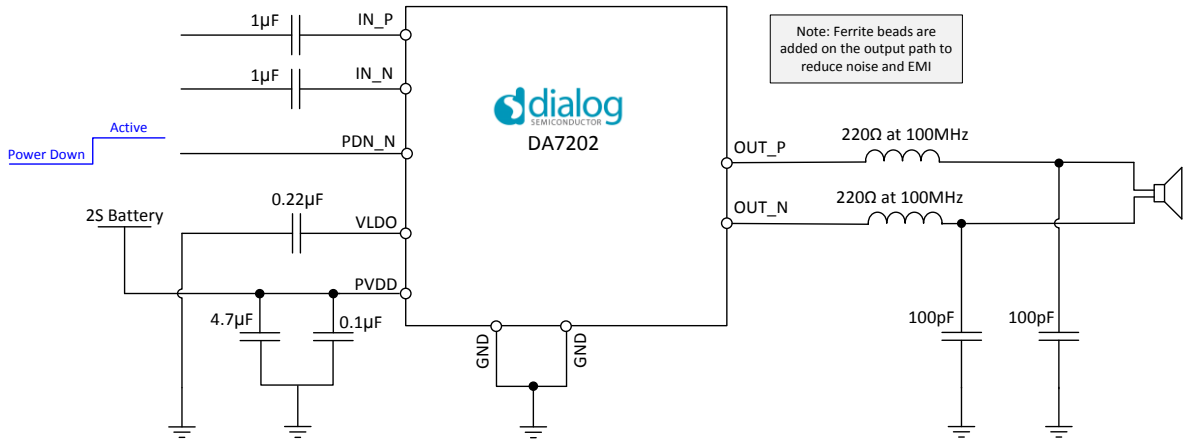

Figure 20: Layout of recommended external components and their values

10.4 Recommended external components

Table 8: Recommended external components

Pin Name	Capacitance	Tolerance	Voltage	Dielectric	Manufacturer	Part number
PVDD	4.7 µF	±10%	35 V	X5R	Muruta	GRM188R6YA475KE15
PVDD OUT_P OUT_N	100 pF	±5%	50 V	COG/NPO	Muruta	GRM1555C1H101JD01D
VLDO	4.7 µF	±10%	16 V	X7R	Muruta	GRM155R71C224KA12D
IN_P IN_N	1 µF	±10%	10 V	X5R	Muruta	GRM155R61A105KE15D
Ferrite bead	220 Ω at 100 MHz	±25%	2 A		TDK	MPZ1608S221A

10.5 Capacitor selection

10.5.1 Input and output capacitors

The DA7202 is designed for operation with small, space-saving ceramic capacitors, but function with most commonly used capacitors as long as attention is paid to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 3.0 µF capacitance with an ESR of 1 Ω or less is recommended for the input capacitor on PVDD to ensure the stability of the DA7202.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the DA7202's transient response to large changes in load current.

10.5.2 Input and output capacitor properties

Use any good quality ceramic capacitors with the DA7202 that meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behaviour over temperature and applied voltage. Capacitors must have a dielectric sufficient to ensure that the minimum capacitance over the required temperature range and the DC

bias conditions. X5R or X7R dielectrics with a voltage rating of greater than 16 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended.

The voltage stability of a capacitor is strongly influenced by the capacitor size and its voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about 15% over the −40°C to +85°C operating temperature range of the DA7202, and is not a function of package or voltage rating.

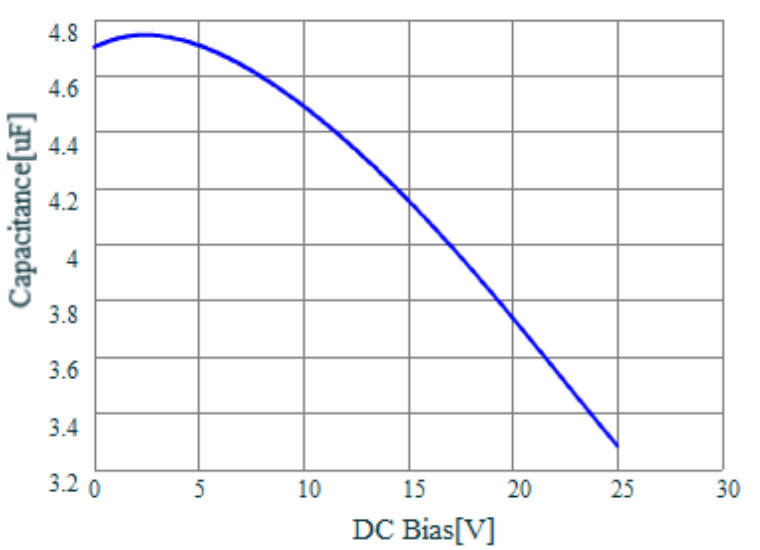

Figure 21: Performance plot of the sample capacitor used in the example (below)

Use the following equation to determine the worst case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{OUT} = C_{EFF} \times (1 - TEMPCO) \times (1 - TOL)$$

Where:

- C_{EFF} is the effective capacitance at the operating voltage
- **TEMPCO** is the worst-case capacitor temperature coefficient, specified as a value between 0 and 1.
- **TOL** is the worst-case component tolerance, specified as a value between 0 and 1.

In this example, the worst case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and CEFF is 4.620 µF at 7.2 V, as shown in Figure 21. Substituting these values into the equation yields

$$C_{OUT} = 4.620\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.53\ \mu F$$

The capacitor chosen in this example therefore meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the DA7202, it is imperative that the effects of DC bias and temperature on the behaviour of the capacitors are evaluated for each application.

11 Package information

11.1 Package outlines

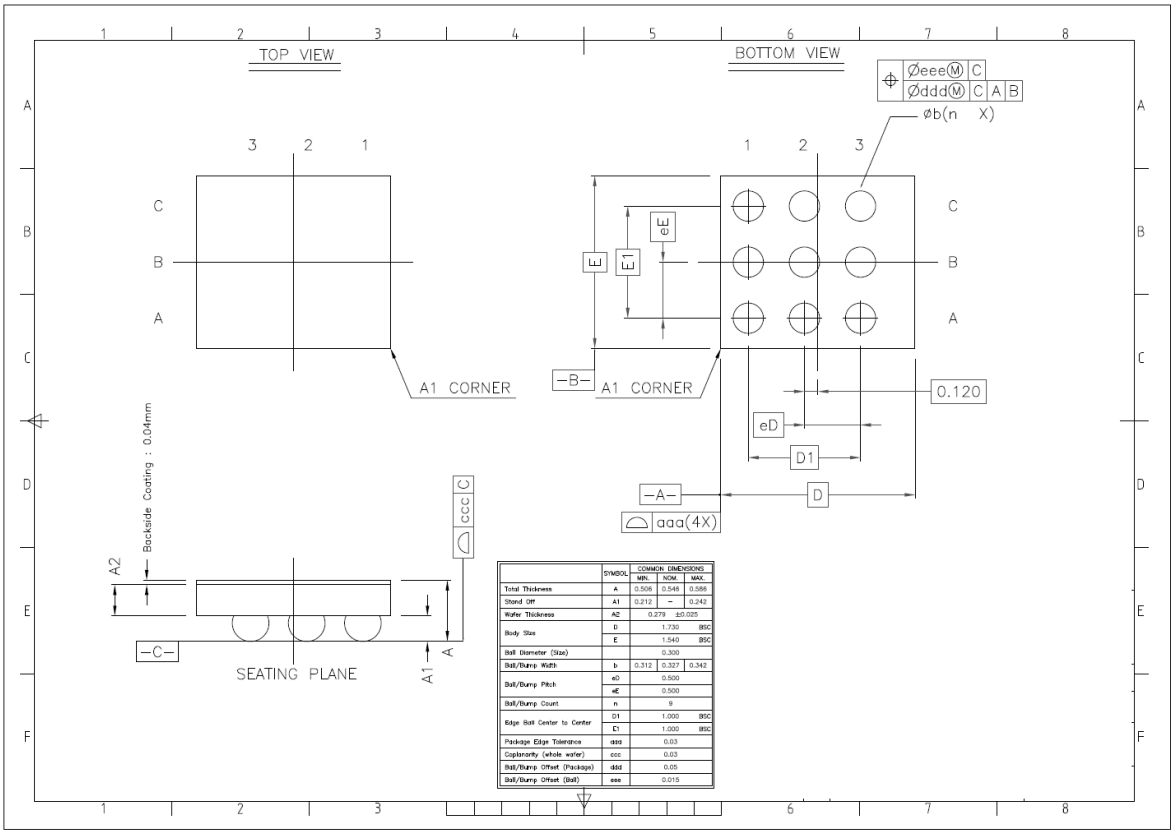

Figure 22: DA7202 package outline drawing (9-bump WL-CSP 0.5 mm pitch)

11.2 Soldering information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12 Ordering information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 9: Ordering information

Part number	Package	Shipment form	Pack quantity
DA7202-00UH2	9-bump CSP Pb free/green	T & R	4000

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS compliance

Dialog Semiconductor complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.

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