LCMXO3LF-9400C Hitless I/O Demo

User Guide

FPGA-UG-02022 Version 1.0

June 2017

Contents

Figures

Tables

1. Introduction

In mission critical systems such as data centers, storage and networking, feature improvements and bug fixes are performed through background updates. Designers, however, avoid updating the control programmable logic device (PLD) because it forces a power cycle or reset of the entire system to enable the new algorithm to take effect. The PLD typically performs power management, reset management, glue logic and other housekeeping functions on the board that should not be interrupted.

The Lattice Semiconductor MachXO3™ control PLD offers designers the option of performing updates in the background and enabling new algorithms to take effect without interrupting board-level operations by eliminating the need to power-cycle or reset the device. The LCMXO3LF-9400C Hitless I/O Demo showcases this feature known as hitless or zero-downtime system update. The Lattice Diamond® software is used in this demo, enabling key features such as TransFR and Leave Alone.

This demo user guide describes the MachXO3 hitless I/O technology and provides the details of the design.

1.1. Demo Design Overview

System-critical functions are controlled and supervised by CPLD or FPGA logic. It can be time consuming, inconvenient and costly to remove these systems from service to perform updates to the reprogrammable logic. It is advantageous to update system control logic and state machines in the background without impacting dependent downstream circuits such as power supplies or alarms. The MachXO3 hitless I/O feature is specifically designed to hold critical signal output states stable while the underlying logic is updated. The output states that are put on hold do not glitch during the update process. These can optionally be used to preset the logic state machines to resume control at any desired operating point upon resumption of normal operation.

The hitless I/O design uses silicon features built into the MachXO3 FPGA in concert with minimal additions to the user design logic. MachXO3 supports background reprogramming and TransFR mode reconfiguration. A simple multiplexer latch circuit is added to the critical user outputs and a simple common Message Control block (MCB) is used for interfacing with the System Update Controller. The System Update Controller communicates with the Message Control block over a suitable channel, for example signal wire or I^{2}C, to coordinate the update event.

The hitless I/O demo consists of five parts:

- Normal operation – Loading the ‘original’ design. The output LEDs are under the ‘original’ design control.
- Updating the Flash image – Programming the ‘new’ design into Configuration Flash in the background.
- Preparing for update – Communicating to the device regarding a design update using an external switch. The binary counter value is frozen.
- Updating the design – Reconfiguring the configuration SRAM with the new bitstream image contained in the configuration Flash array using the TransFR and Leave Alone features. LED outputs are held stable without glitching.
- Resuming normal operation – The updated ‘new’ design is active with the outputs driven by the updated design.

1.2. MachXO3-9400 Development Board and Resources

The onboard buttons, DIP Switches and LEDs of the MachXO3LF-9400 Development Board are used to demonstrate the hitless I/O feature of the MachXO3 device. Figure 1.1 shows the top side of the MachXO3-9400 Development Board and resources used for the demo.

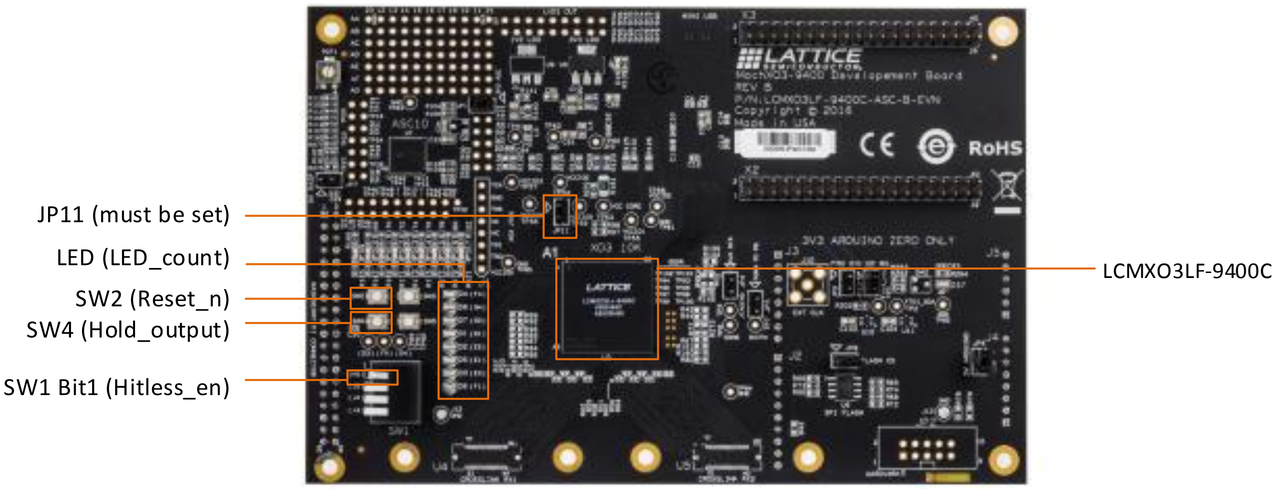


Figure 1.1 Demo Resources

2. Functional Description

2.1. General

The following is a general description of the hitless I/O feature operation. Figure 2.1 shows the demo design block diagram and Figure 2.2 shows the timing diagram.

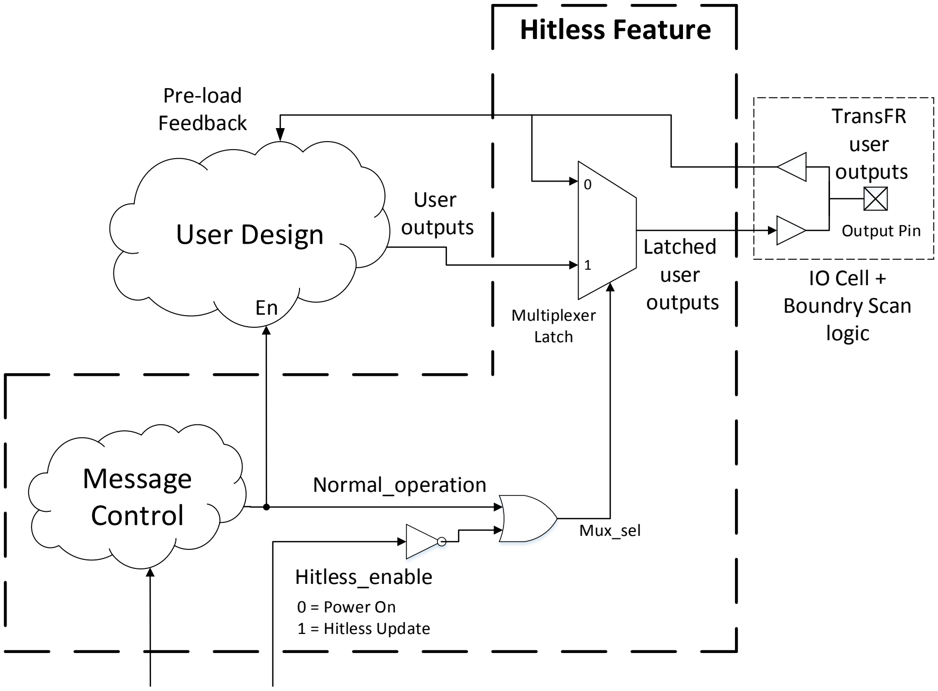


Figure 2.1. Hitless I/O Demo Design Block Diagram

A Normal_operation signal is used to support the hitless I/O circuit. Normal_operation must have a default global reset signal GSR value of False. Following the release of the GSR, Normal_operation is typically asserted by the user logic to indicate that the User Design circuit is free to operate. Normal_operation typically remains asserted until the start of the hitless I/O operation. A message from an external controller is used to deassert Normal_operation, typically after the new bitstream is programmed into Flash memory and just prior to a sysConfig REFRESH command or PROGRAMN pin toggle.

The User Design outputs are captured and held with the soft 2:1 multiplexer latch. Normal_operation then remains deasserted until the MachXO3 device begins reconfiguration. As reconfiguration begins, the TransFR circuit in the Boundary Scan logic in the I/O cell latches the output value (Phase 2 of the Non-JTAG mode TransFR Sequence. Refer to TN1087 – Minimizing System Interruption During Configuration Using TransFR Technology). The TransFR Boundary Scan logic holds the output states through Phases 3 and 4 until the device wake-up is complete and the device re-enters User Mode. The re-established soft 2:1 multiplexer re-acquires the TransFR cell value during the device wake-up sequence (Phase 4) and holds it until the assertion of Normal_operation.

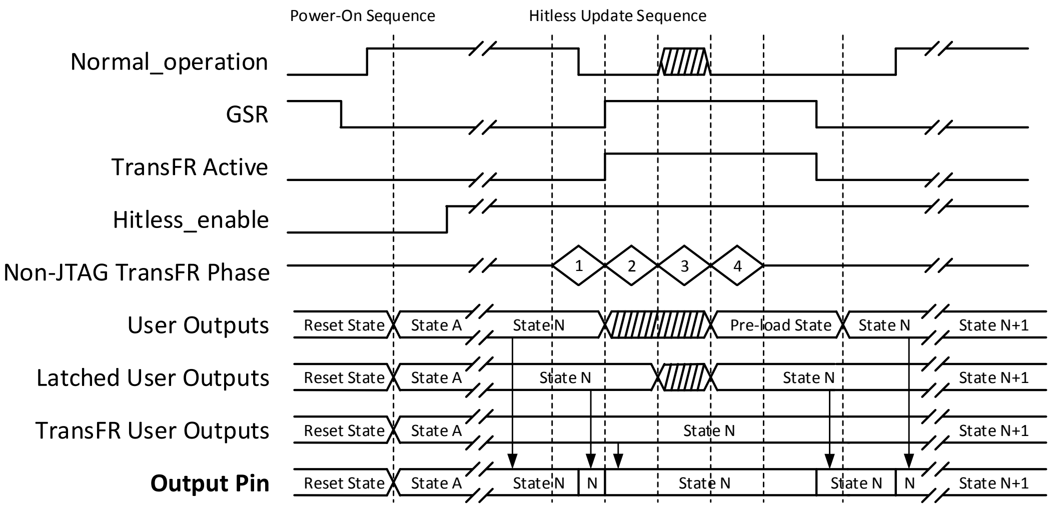


Figure 2.2. Hitless I/O Demo Timing Diagram

The hitless I/O logic must cover two primary scenarios when the FPGA enters User Mode: Power-up and Hitless Reconfiguration. The control input Hitless_en is driven by an external controller to determine which scenario is active. If Hitless_en is false, the user logic starts from a power-up reset state. If true, the user logic can utilize the values held in the TransFR Boundary Scan I/O cells to initialize the control logic to resume from the pre-update state. See Table 2.1 for the truth table showing both the general behavior of the feature and the specific behavior of the demonstration design.

Table 2.1. Truth Table for Normal_Operation, Hitless_Enable

Hitless_enable	Normal_operation	User Design Output	Demo Design Output
X	1	Normal Operation	Normal Counter Operation
0	0	User Defined Power-up State	‘0’ (LED’s ON)*
1	0	User Defined Hold/Preload State	Feedback Value

***Note**: All LED cathodes are driven by the design output. As such, LED ON represents ‘0’ and LED OFF represents ‘1’.

As shown in Figure 2.3, the hitless top level design is divided into three major blocks:

- User design block
- Multiplexer latch to hold outputs
- Message control block

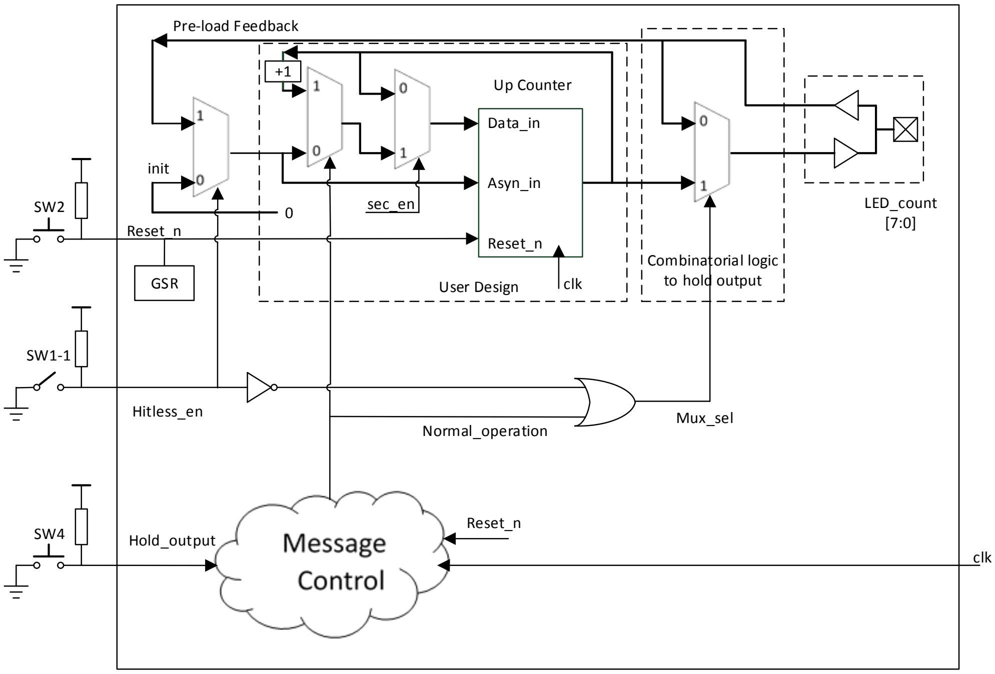


Figure 2.3. TransFR I/O Cell Simplified Block Diagram

For detailed pin/port descriptions, see the Port Assignments and Descriptions section.

2.2. User Design Block

The User Design block contains the original user logic, in this case a simple 8-bit up-counter design. The original user logic is updated to include two accommodations which support the hitless I/O process:

- Enable input
- Addition of a multiplexer latch to select the asynchronous reset Preset/Restore value.

In the demonstration, this block is updated to become a down-counter. The reset_n logic is placed on the GSR net by the software.

2.3. Multiplexer Latch to Hold Outputs

The hitless I/O design also features multiplexer latch(es) and a few basic logic cells added to the top level to hold the outputs stable. A 2:1 multiplexer latch is instantiated for each original output signal which is to become hitless, and the output is changed into a bidirectional I/O. A common combinatorial logic path is instantiated for the Hitless_en control signal. The path must be 100% combinatorial so that the 2:1 muxes are controlled by the state of Hitless_en prior to the release of GSR.

2.4. Message Control Block

This hitless I/O design addition is used to communicate messages to the hitless top level design that the transFR operation is about to occur. SW4 represents the ‘external controller’ as described in the General section. The message is conveyed by closing SW4, a momentary switch on the MachXO3-9400 Development Board. The closing edge (falling edge) of Hold_output is detected and used to negate Normal_operation until the device is refreshed.

Following the FPGA image update, Normal_operation is re-asserted after a small delay, providing time for the circuit to synchronize to the previous counter state as preserved in the LED_count I/O cells.

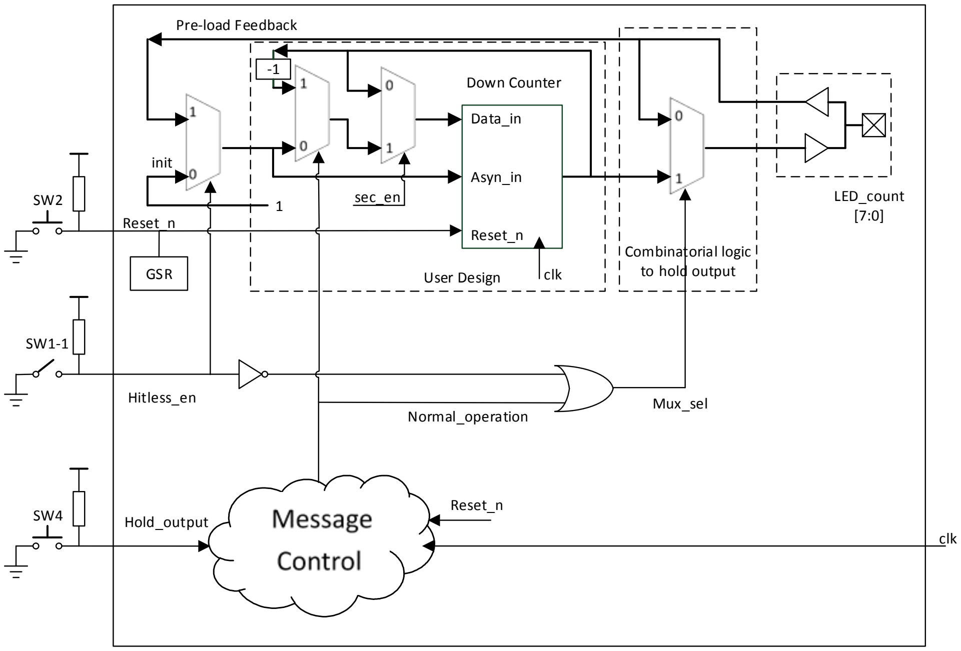


Figure 2.4. Hitless I/O New Top Level Block Diagram

A second, nearly identical design project is included as part of the hitless I/O demonstration. As shown in Figure 2.4, only the user design block is changed to include a Down Counter block in place of the prior Up Counter. All the other blocks remain untouched.

The user will be able to switch between the designs without causing glitches or state changes to the LED outputs.

3. Demo Package

The demo package includes the following:

- Lattice Diamond project and preference files
- JED file for programming the MachXO3 internal configuration flash

3.1. Hardware Requirements

To run the demo, the following hardware are required:

- PC running Windows 7 Operating System
- MachXO3-9400 Development Board
- Mini USB cable for programming the MachXO3 device

3.2. Software Requirements

To run the demo, the following software are required:

- Lattice Diamond version 3.9 or later
- Lattice Diamond Programmer software for bitstream downloading

Note: These software programs are available at www.latticesemi.com/en/Products/DesignSoftwareAndIP.

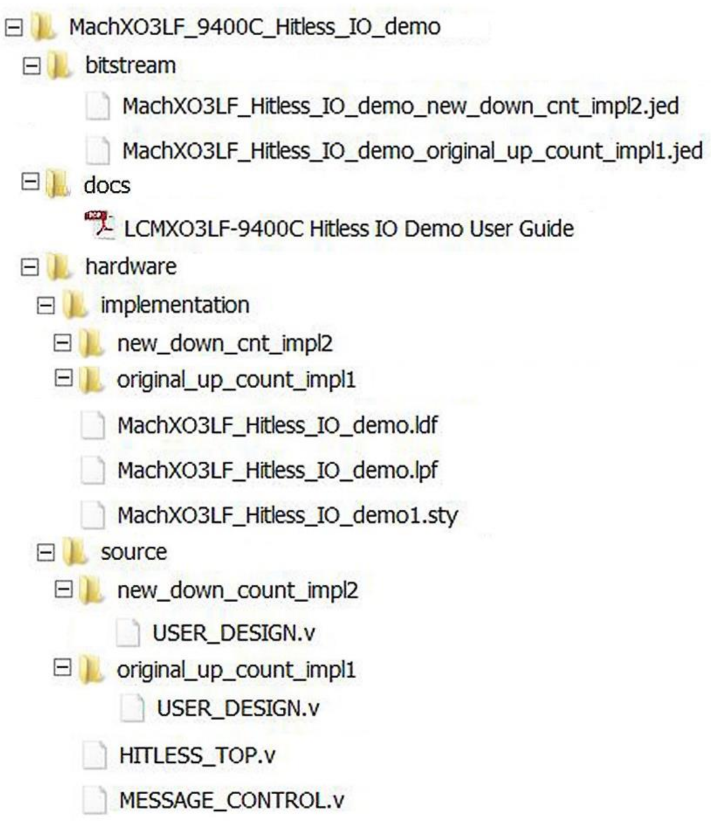
4. Port Assignments and Descriptions

Table 4.1. FPGA Demo Design Ports

Port Name	I/O Type	Width	Description
Reset_n	Input	1	Asynchronous reset, active low (Button SW2)
Clk	Input	1	Input clock from crystal
Hitless_en	Input	1	Toggle switch (SW1 BIT1) to differentiate between the power on and hitless I/O operation. Down (0) – Power on Up (1) – Hitless I/O
hold_output	Input	1	Push-button switch (SW4) to hold the output state
LED_count	Output	8	LEDs indicating the output values

5. Demo Package Directory Structure

Figure 5.1 shows the demo package directory structure.



```
MachXO3LF_9400C_Hitless_IO_demo
  bitstream
      MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed
      MachXO3LF_Hitless_IO_demo_original_up_count_impl1.jed
  docs
      LCMXO3LF-9400C Hitless IO Demo User Guide
  hardware
    implementation
      new_down_cnt_impl2
      original_up_count_impl1
      MachXO3LF_Hitless_IO_demo.ldf
      MachXO3LF_Hitless_IO_demo.lpf
      MachXO3LF_Hitless_IO_demo1.sty
    source
      new_down_count_impl2
        USER_DESIGN.v
      original_up_count_impl1
        USER_DESIGN.v
      HITLESS_TOP.v
      MESSAGE_CONTROL.v
```

Figure 5.1. Demo Package Directory Structure

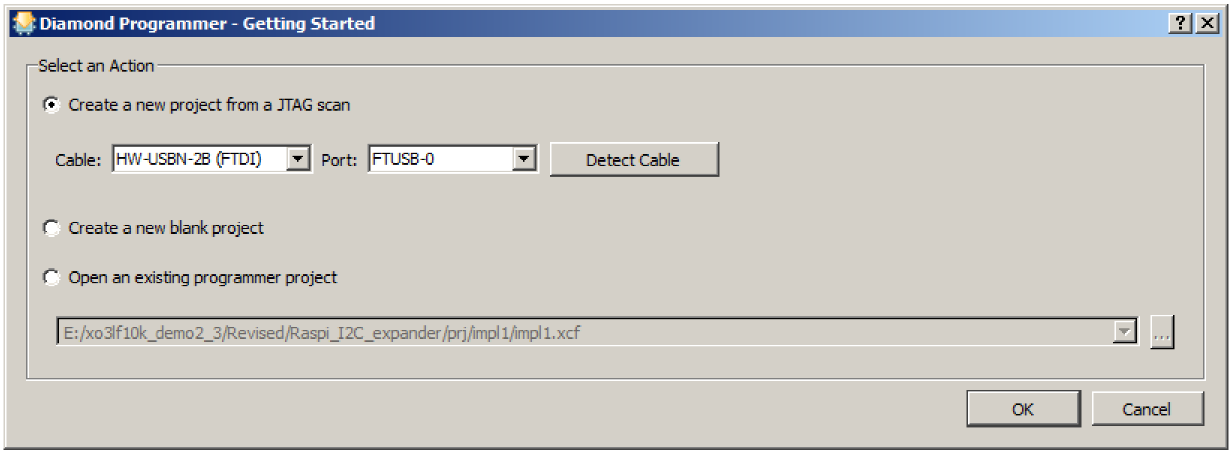
6. Running the Demo

6.1. Programming the Device

To program the device:

Loading the initial design. The onboard output LEDs start counting upwards.

1. Launch the Diamond Programmer Software (version 3.9 or above). In the Getting Started dialog box as shown in Figure 6.1, select **Create a new project file from JTAG scan** and click **OK**.



Diamond Programmer - Getting Started

Select an Action

● Create a new project from a JTAG scan

Cable: HW-USBN-2B (FTDI) Port: FTUSB-0

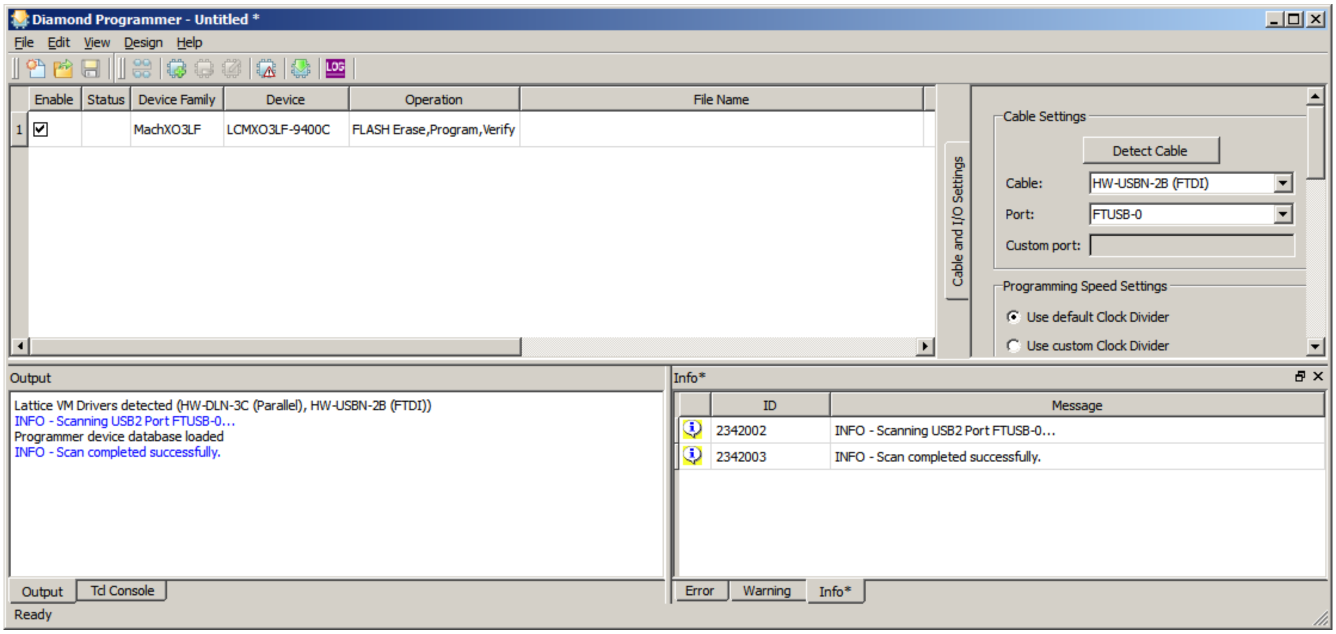
○ Create a new blank project

○ Open an existing programmer project

E:/xo3lf10k_demo2_3/Revised/Raspi_I2C_expander/prj/impl1/impl1.xcf

Figure 6.1. Diamond Programmer Getting Started Page

2. The Diamond Programmer starts scanning the board attached to the USB cable.



Diamond Programmer - Untitled *

	Enable	Status	Device Family	Device	Operation	File Name
1	☑		MachXO3LF	LCMXO3LF-9400C	FLASH Erase,Program,Verify	

Cable Settings

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

Output

```
Lattice VM Drivers detected (HW-DLN-3C (Parallel), HW-USBN-2B (FTDI))
INFO - Scanning USB2 Port FTUSB-0...
Programmer device database loaded
INFO - Scan completed successfully.
```

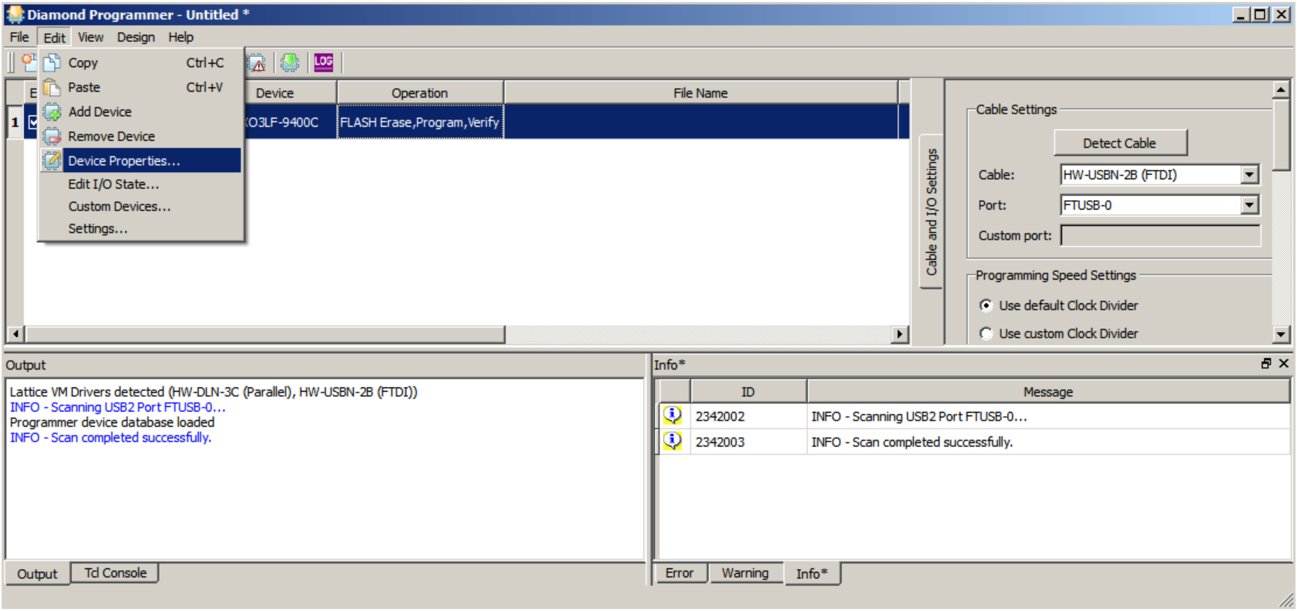
Info*

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.

Ready

Figure 6.2. Diamond Programmer Main Interface

3. Click the device row to highlight it and select **Edit > Device Properties** from the menu bar. This allows you to edit the access mode, operation mode and select the programming file.



	Device	Operation	File Name
1	O3LF-9400C	FLASH Erase,Program,Verify	

Cable Settings
Cable: HW-USBN-2B (FTDI)
Port: FTUSB-0
Custom port:

Programming Speed Settings
● Use default Clock Divider
○ Use custom Clock Divider

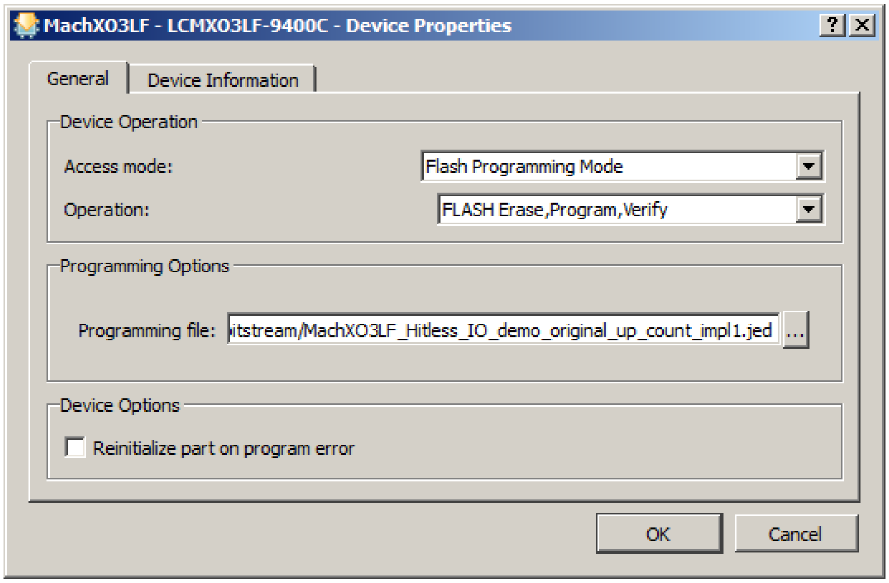
Output

```
Lattice VM Drivers detected (HW-DLN-3C (Parallel), HW-USBN-2B (FTDI))
INFO - Scanning USB2 Port FTUSB-0...
Programmer device database loaded
INFO - Scan completed successfully.
```

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.

Figure 6.3. Device Properties Option

4. Set device properties as shown in Figure 6.4.
In the Device Properties dialog box, select **Flash Programming Mode** in Access mode and **Flash Erase, Program, Verify** in Operation. Select the bitstream file **\bitstream\MachXO3LF_Hitless_IO_demo_original_up_count_impl1.jed** in Programming file. Click **OK**.



Device Operation
Access mode: Flash Programming Mode
Operation: FLASH Erase,Program,Verify

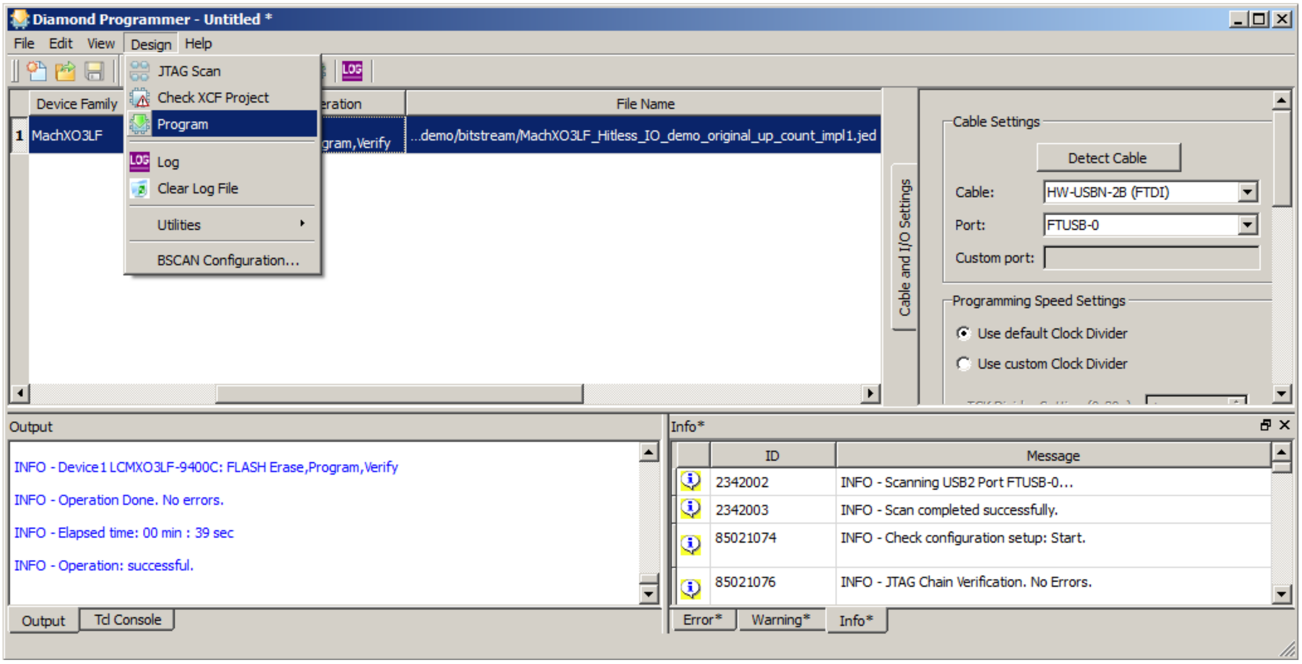
Programming Options
Programming file: itstream/MachXO3LF_Hitless_IO_demo_original_up_count_impl1.jed

Device Options
□ Reinitialize part on program error

Figure 6.4. Browse Programming File

The next step is to program the device.

5. From the menu bar, select **Design > Program**.



	Device Family	eration	File Name
1	MachXO3LF	gram,Verify	...demo/bitstream/MachXO3LF_Hitless_IO_demo_original_up_count_impl1.jed

Cable Settings

Detect Cable

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

```
INFO - Device1 LCMXO3LF-9400C: FLASH Erase,Program,Verify
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 39 sec
INFO - Operation: successful.
```

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.

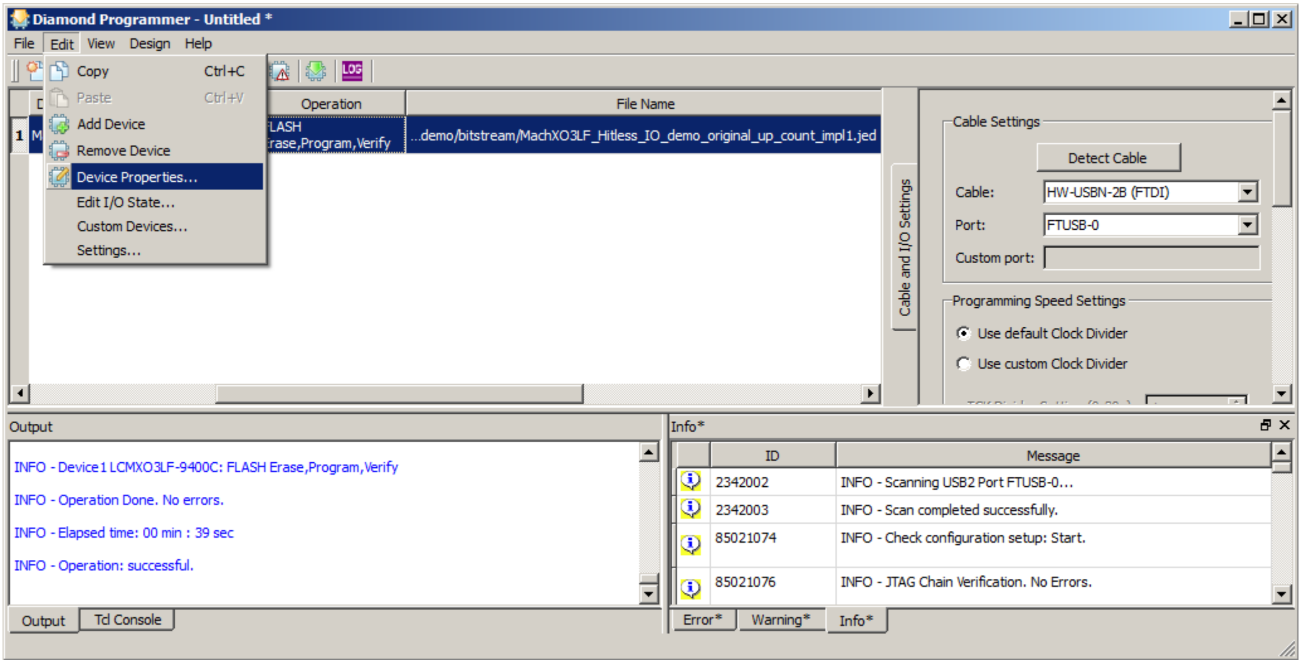
Figure 6.5. Programming the Device

When the programming of the device is completed, the LEDs on the MachXO3LF 9400 Development Board start counting up from zero (LED OFF represents 1; LED ON represents 0).

6.2. Updating the Flash Image

To update the flash image:

1. Click the device row to highlight it and from the menu bar, select **Edit > Device Properties**. This allows you to edit the access mode as well as operation.



	Operation	File Name
1	FLASH Erase,Program,Verify	...demo/bitstream/MachXO3LF_Hitless_IO_demo_original_up_count_impl1.jed

Cable Settings

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

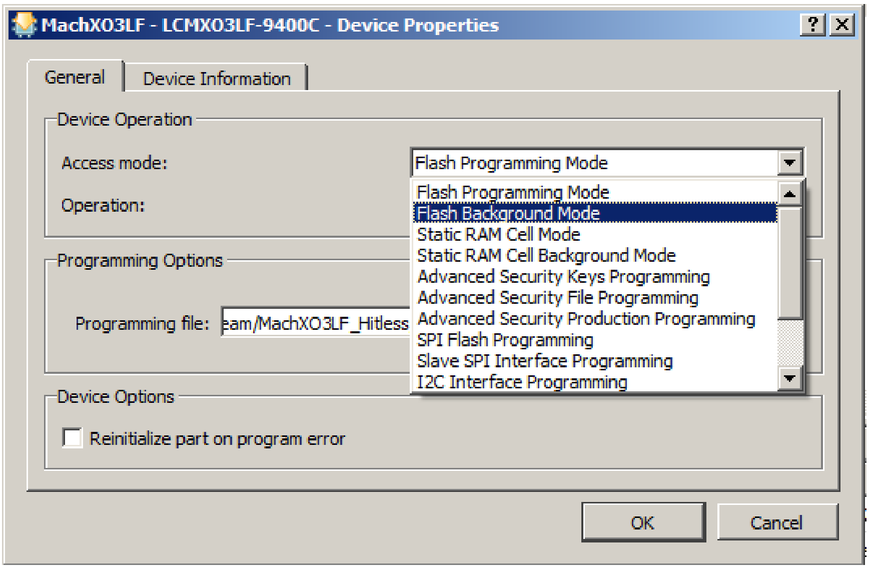
Output

```
INFO - Device1 LCMXO3LF-9400C: FLASH Erase,Program,Verify
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 39 sec
INFO - Operation: successful.
```

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.

Figure 6.6. Device Properties Option

2. From the **Access Mode** drop-down list select **Flash Background Mode** as shown in Figure 6.7.


MachXO3LF - LCMXO3LF-9400C - Device Properties
General
Device Information
Flash Programming Mode
Flash Background Mode
Static RAM Cell Mode
Static RAM Cell Background Mode
Advanced Security Keys Programming
Advanced Security File Programming
Advanced Security Production Programming
SPI Flash Programming
Slave SPI Interface Programming
I2C Interface Programming
OK
Cancel

Device Operation

Access mode: Flash Programming Mode

Operation:

Programming Options

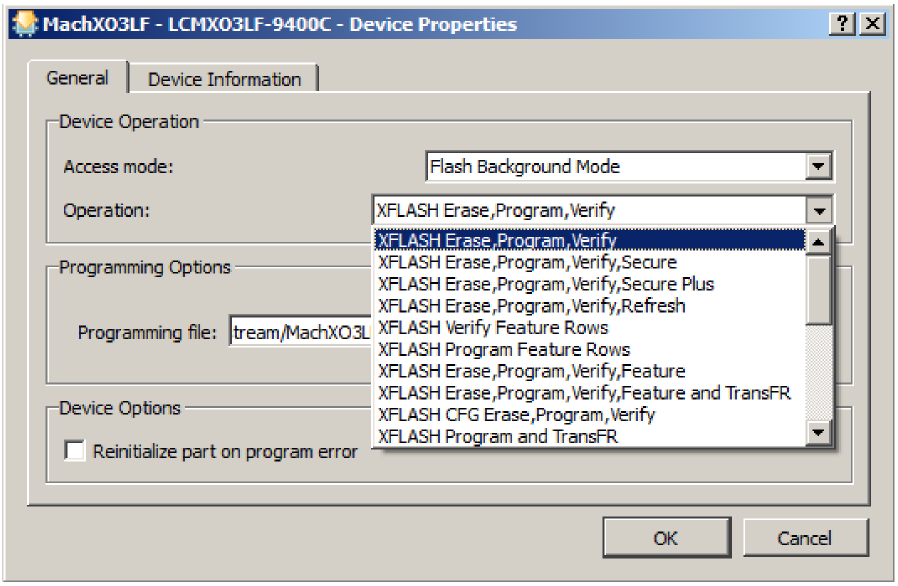
Programming file: eam/MachXO3LF_Hitless

Device Options

□ Reinitialize part on program error

Figure 6.7. Access Mode Options

3. From the Operation drop-down list select **XFLASH Erase, Program, Verify**.


MachXO3LF - LCMXO3LF-9400C - Device Properties
General
Device Information
Device Operation
Programming Options
Device Options
XFLASH Erase,Program,Verify
XFLASH Erase,Program,Verify,Secure
XFLASH Erase,Program,Verify,Secure Plus
XFLASH Erase,Program,Verify,Refresh
XFLASH Verify Feature Rows
XFLASH Program Feature Rows
XFLASH Erase,Program,Verify,Feature
XFLASH Erase,Program,Verify,Feature and TransFR
XFLASH CFG Erase,Program,Verify
XFLASH Program and TransFR
OK
Cancel

Access mode: Flash Background Mode

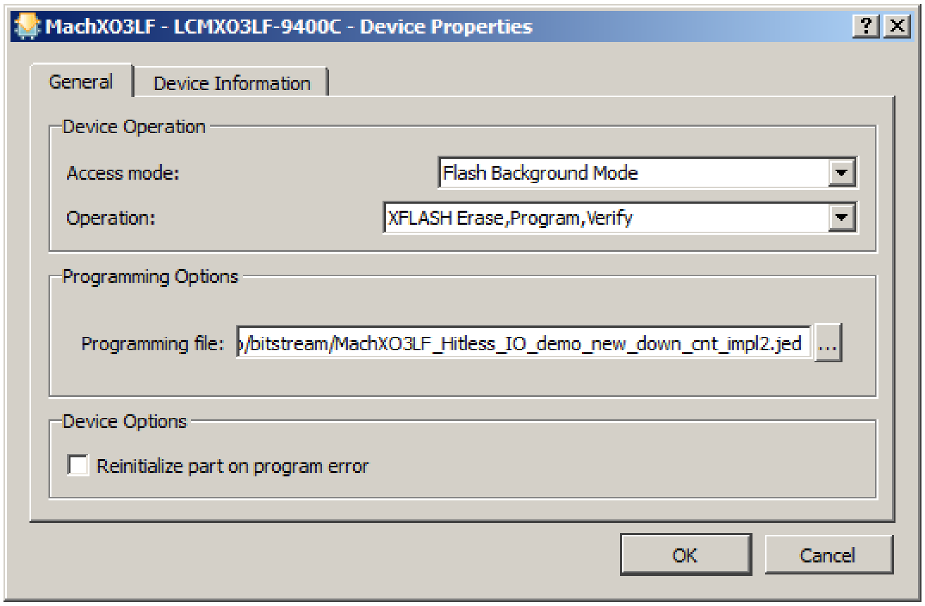
Operation: XFLASH Erase,Program,Verify

Programming file: tream/MachXO3L

□ Reinitialize part on program error

Figure 6.8. Operation Options

4. Select the bitstream file **\bitstream\MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed** in Programming file. Click **OK**.



Access mode: Flash Background Mode

Operation: XFLASH Erase,Program,Verify

Programming file: :/bitstream/MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed

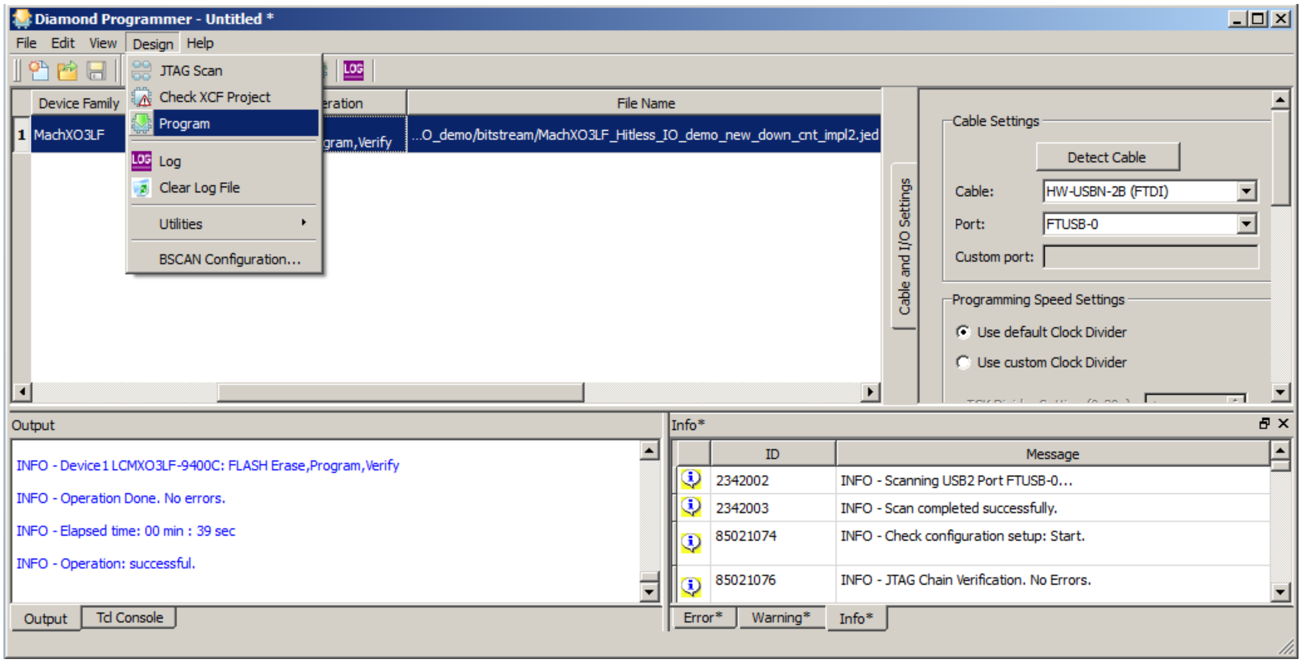
□ Reinitialize part on program error

Figure 6.9. Browse Programming File

The next step is to program this bitstream into the device.

5. From the menu bar, select **Design > Program**.

During the Program operation, the LEDs do not change counting state nor glitch. This can be confirmed using an oscilloscope.



	Device Family	eration	File Name
1	MachXO3LF	...gram,Verify	...O_demo/bitstream/MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed

Cable Settings

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

```
INFO - Device1 LCMXO3LF-9400C: FLASH Erase,Program,Verify
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 39 sec
INFO - Operation: successful.
```

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.

Figure 6.10. Programming the Device

6.3. Preparing for Update

Before the new design is transferred to active SRAM, it is necessary to communicate with the device regarding the imminent update.

In this demo, an external switch is used to communicate with the device regarding the design update. Check that all bits of SW1 are 'Up', then press the button SW4 momentarily to freeze the LED binary count output on LED7~0. Refer to Figure 6.11.

Note that if SW1 BIT1 is down, the counter resets to the power up state when button SW4 is pressed (LED OFF represents 1; LED ON represents 0).When SW1 BIT1 is up If SW4 is not pressed to freeze the outputs, the outputs may glitch during the update step.

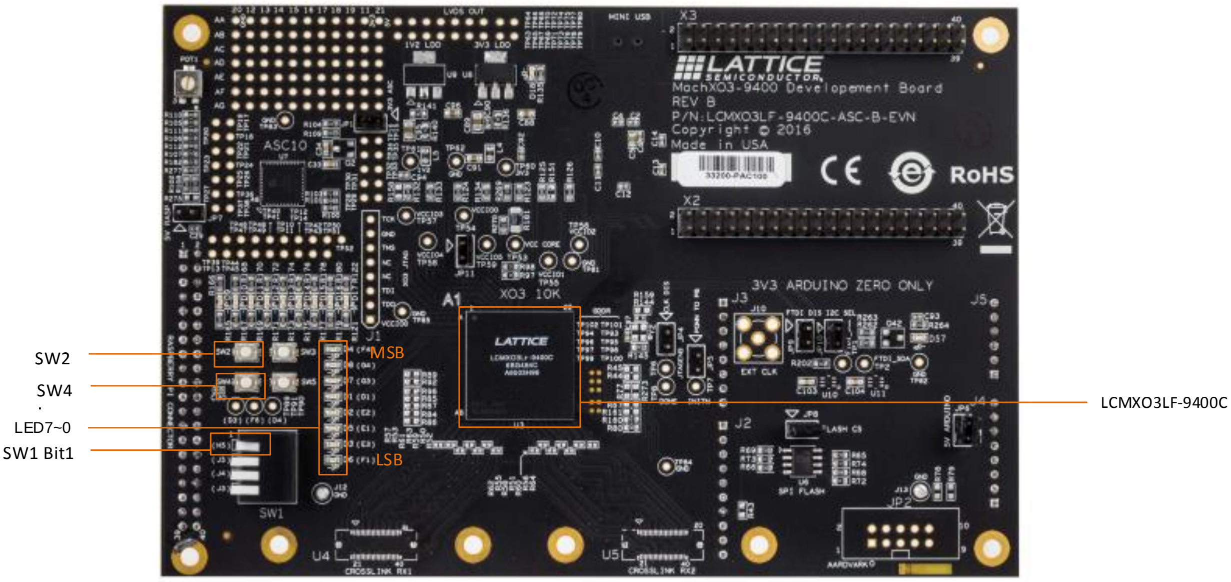
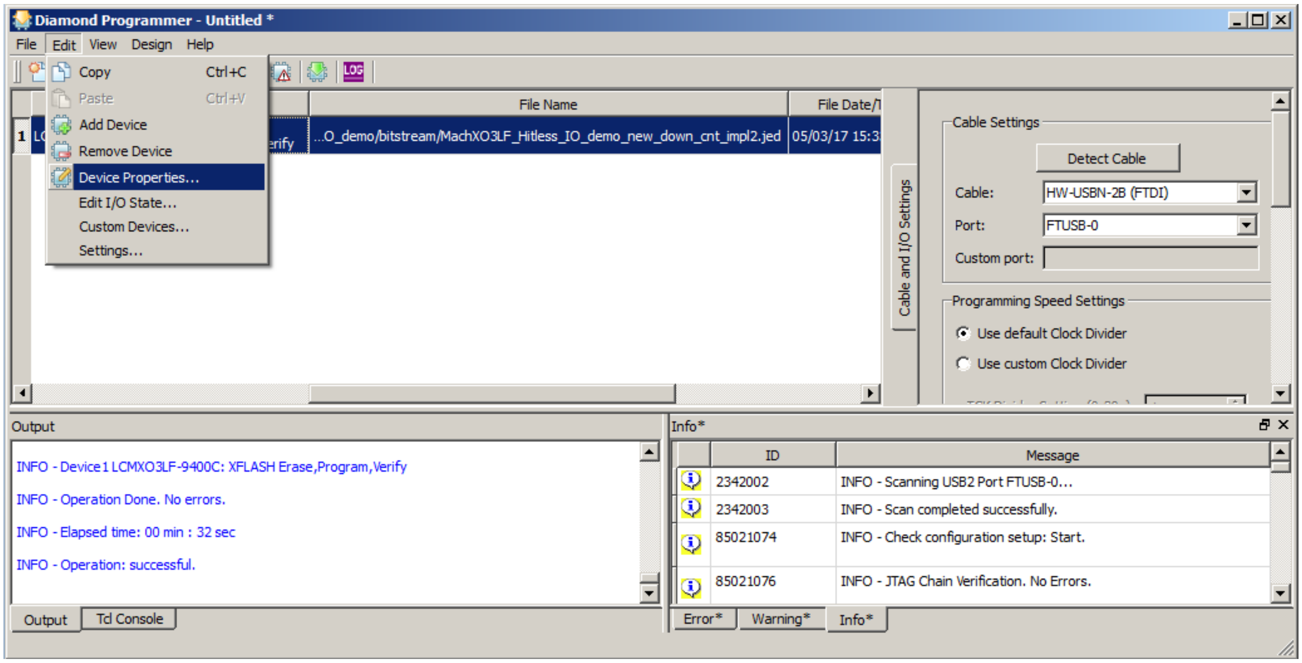


Figure 6.11. Preparations for the Demonstration

6.4. Updating the Design

To update the design:

1. Highlight the device row by clicking anywhere on the row. From the menu bar select **Edit** > **Edit I/O State**.



1 LC ... erify ...O_demo/bitstream/MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed 05/03/17 15:3

Cable Settings

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

Programming Speed Settings

● Use default Clock Divider

○ Use custom Clock Divider

Output

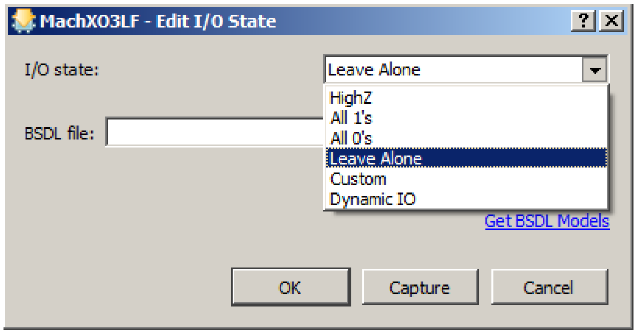
```
INFO - Device1 LCMXO3LF-9400C: XFLASH Erase,Program,Verify
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 32 sec
INFO - Operation: successful.
```

Info*

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.

Figure 6.12. Edit I/O State Option

2. In the Edit I/O State dialog box, from the I/O state drop-down list select **Leave Alone** as shown in Figure 6.13. Click **OK** to confirm this selection.

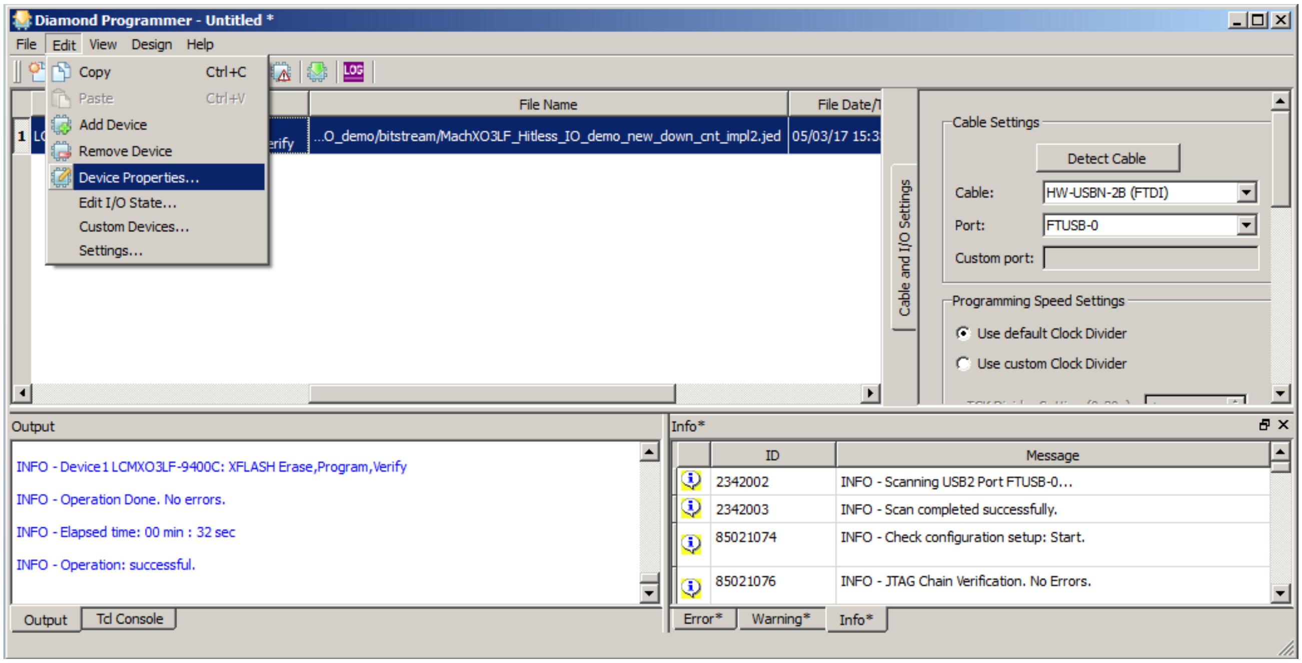


I/O state: Leave Alone

BSDL file:

Figure 6.13. Edit I/O State Dialog Box

3. Click the device row to highlight it and from the menu bar, select **Edit > Device Properties**. This allows you to edit the access mode as well as operation.



1	LC...	...erify	...O_demo/bitstream/MachXO3LF_Hitless_IO_demo_new_down_cnt_impl2.jed	05/03/17 15:3

Cable: HW-USBN-2B (FTDI)

Port: FTUSB-0

Custom port:

● Use default Clock Divider

○ Use custom Clock Divider

Output

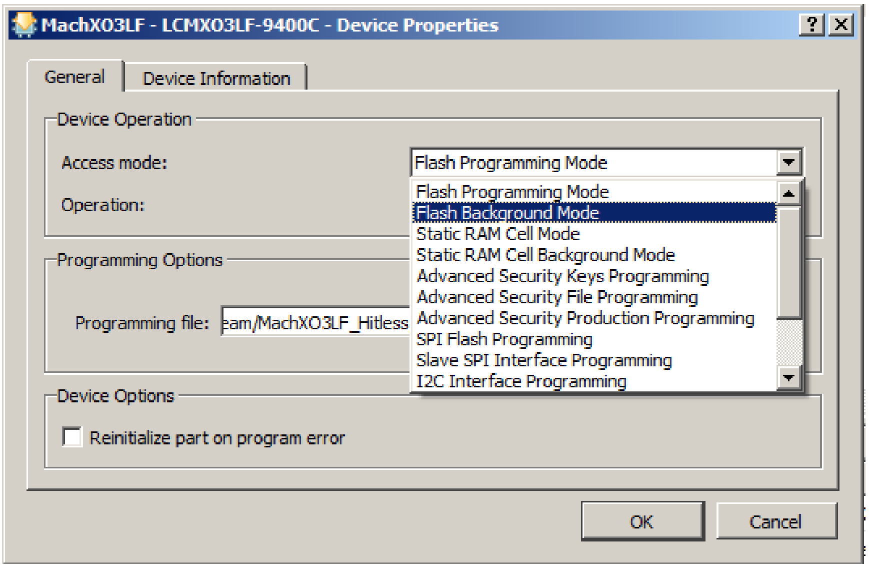
```
INFO - Device1 LCMXO3LF-9400C: XFLASH Erase,Program,Verify
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 32 sec
INFO - Operation: successful.
```

Info*

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.

Figure 6.14. Device Properties Option

4. From the Access Mode drop- down list select **Flash Background Mode** as shown in Figure 6.15.



MachXO3LF - LCMXO3LF-9400C - Device Properties

Device Operation

Access mode: Flash Programming Mode

Operation:

Programming Options

Programming file: eam/MachXO3LF_Hitless

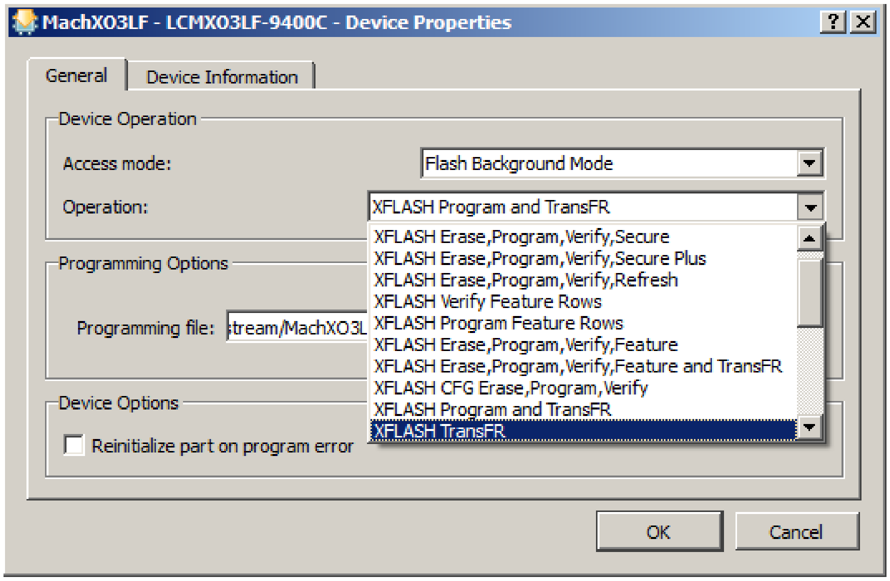
Device Options

☐ Reinitialize part on program error

General
Device Information
Flash Programming Mode
Flash Background Mode
Static RAM Cell Mode
Static RAM Cell Background Mode
Advanced Security Keys Programming
Advanced Security File Programming
Advanced Security Production Programming
SPI Flash Programming
Slave SPI Interface Programming
I2C Interface Programming
OK
Cancel

Figure 6.15. Access Mode Options

5. Under Operation, select **XFLASH TransFR** to transfer the ‘new’ bitstream from Configuration Flash to SRAM using the TransFR feature.



MachXO3LF - LCMXO3LF-9400C - Device Properties

Device Operation

Access mode: Flash Background Mode

Operation: XFLASH Program and TransFR

Programming Options

Programming file: tream/MachXO3L

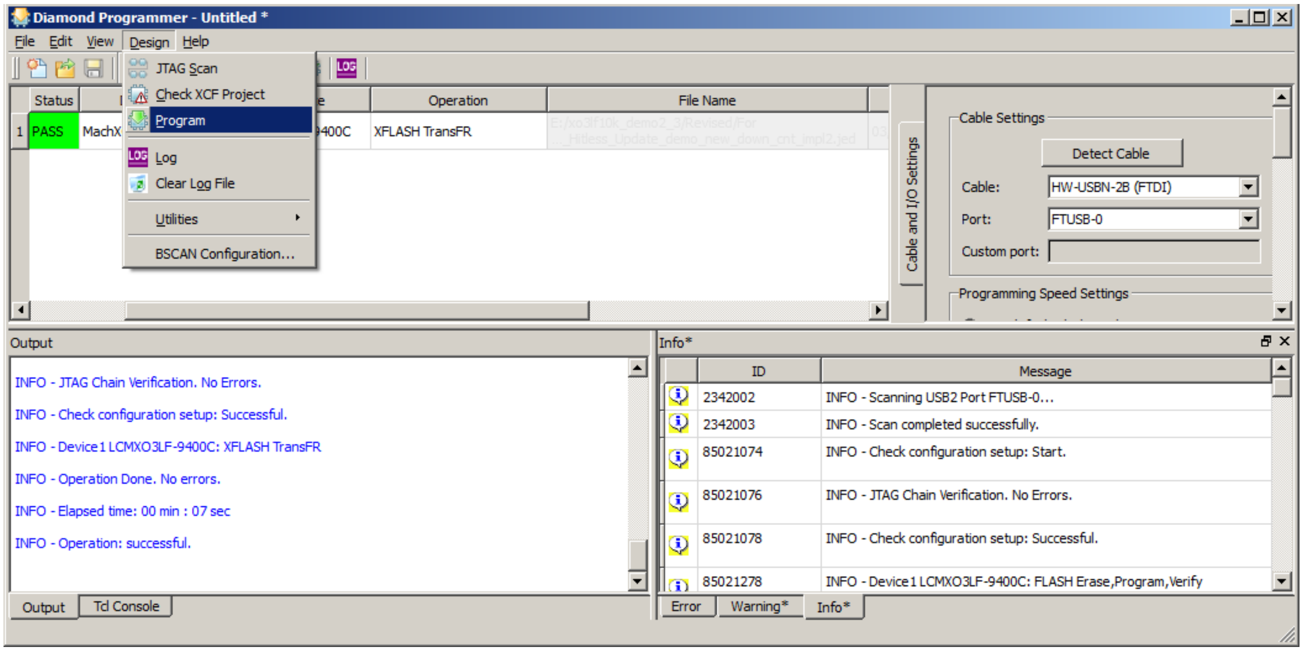
Device Options

☐ Reinitialize part on program error

General
Device Information
XFLASH Erase,Program,Verify,Secure
XFLASH Erase,Program,Verify,Secure Plus
XFLASH Erase,Program,Verify,Refresh
XFLASH Verify Feature Rows
XFLASH Program Feature Rows
XFLASH Erase,Program,Verify,Feature
XFLASH Erase,Program,Verify,Feature and TransFR
XFLASH CFG Erase,Program,Verify
XFLASH Program and TransFR
XFLASH TransFR
OK
Cancel

Figure 6.16. Operation Options

6. From the menu bar, select **Design > Program** to execute the Flash-to-SRAM transfer.



	Status			Operation	File Name
1	PASS	MachX	9400C	XFLASH TransFR	E:/xo3lf10k_demo2_3/Revised/For ..._Hitless_Update_demo_new_down_cnt_impl2.jed

Cable: HW-USBN-2B (FTDI)
Port: FTUSB-0
Custom port:

```
INFO - JTAG Chain Verification. No Errors.
INFO - Check configuration setup: Successful.
INFO - Device1 LCMXO3LF-9400C: XFLASH TransFR
INFO - Operation Done. No errors.
INFO - Elapsed time: 00 min : 07 sec
INFO - Operation: successful.
```

ID	Message
2342002	INFO - Scanning USB2 Port FTUSB-0...
2342003	INFO - Scan completed successfully.
85021074	INFO - Check configuration setup: Start.
85021076	INFO - JTAG Chain Verification. No Errors.
85021078	INFO - Check configuration setup: Successful.
85021278	INFO - Device1 LCMXO3LF-9400C: FLASH Erase,Program,Verify

Figure 6.17. Programming the Device

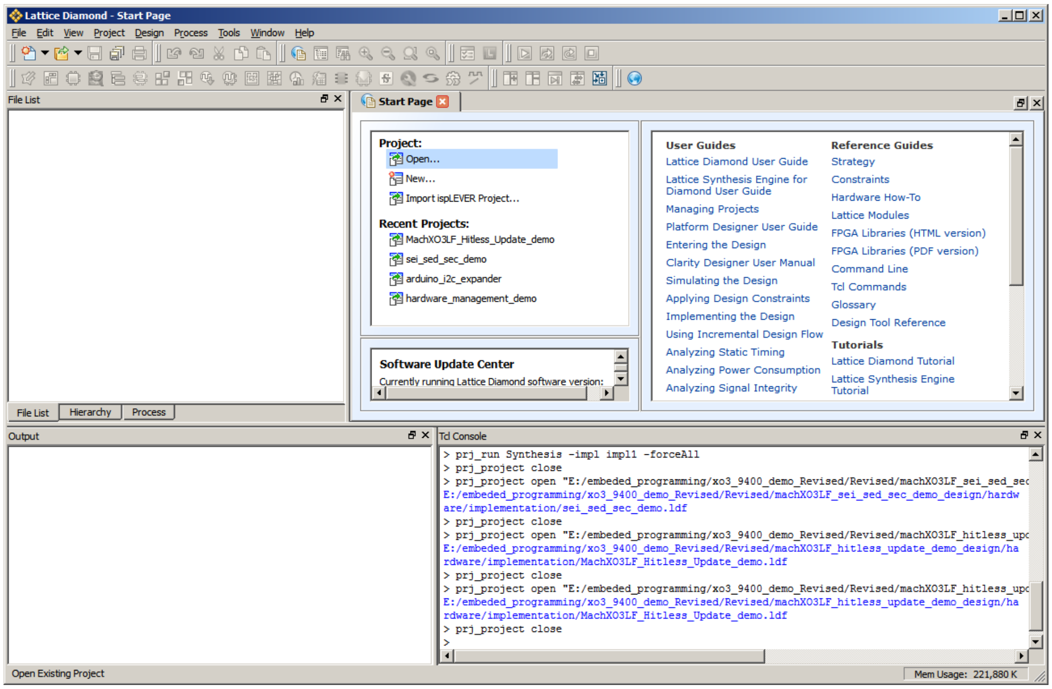
6.5. Resuming Normal Operation

When TransFR is complete, the new bitstream begins operation seamlessly, starts counting down from the LED count value counted up and preserved in the Preparing for Update section (LED OFF represents 1; LED ON represents 0). Not only has the design been successfully updated without changing or glitching the LED output count value, the new circuit is able to resume counting from the previous operation point by referring to the held output states.

7. Rebuilding the Design

To rebuild the design:

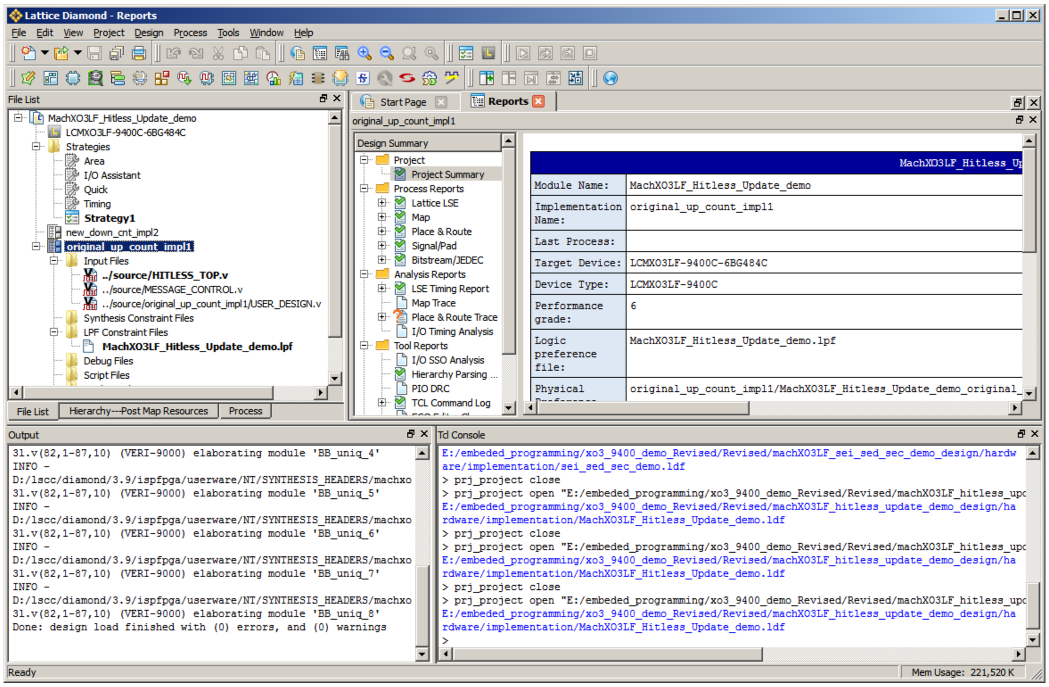
1. Open the Lattice Design file (*.ldf file) by clicking **Open** under Project.



```
> prj_run Synthesis -impl impl1 -forceAll
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_sei_sed_sec
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_sei_sed_sec_demo_design/hardw
are/implementation/sei_sed_sec_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
>
```

Figure 7.1. Opening Design File

2. There are two implementations in this project: original_up_count_impl1 and new_down_cnt_impl2. Make sure to set the appropriate implementation to active.



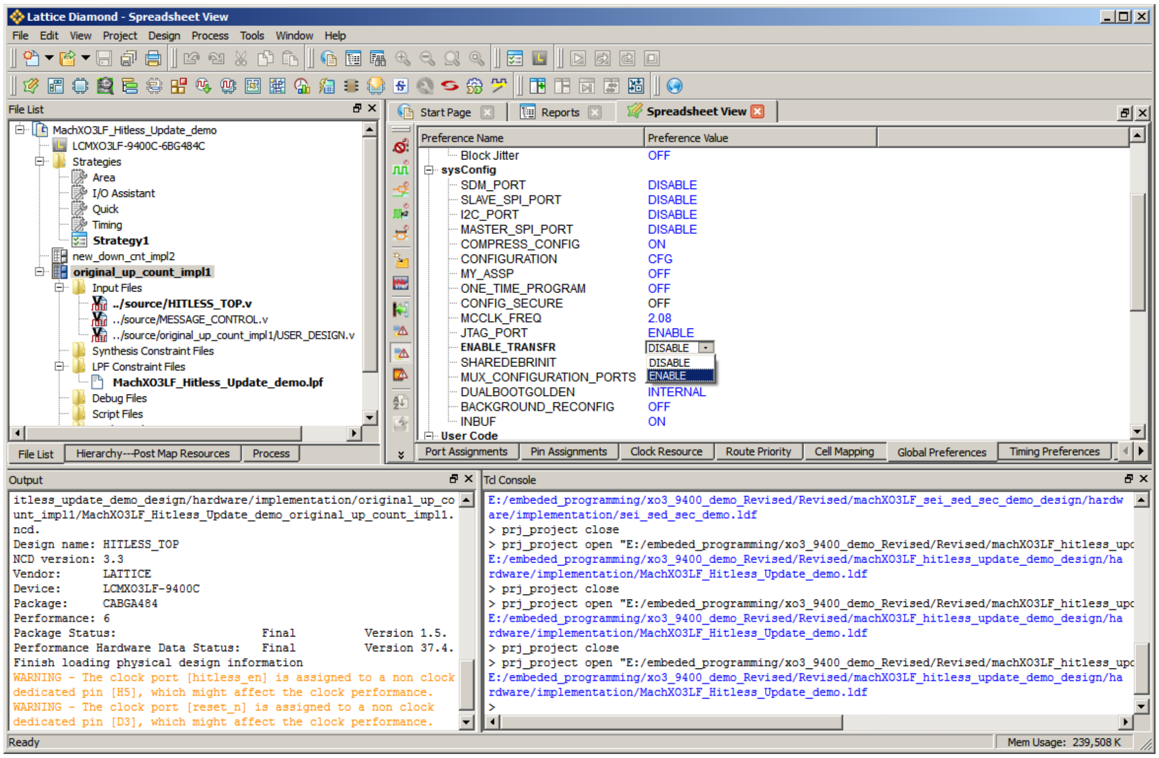
MachXO3LF_Hitless_Up	
Module Name:	MachXO3LF_Hitless_Update_demo
Implementation Name:	original_up_count_impl1
Last Process:	
Target Device:	LCMXO3LF-9400C-6BG484C
Device Type:	LCMXO3LF-9400C
Performance grade:	6
Logic preference file:	MachXO3LF_Hitless_Update_demo.lpf
Physical	original_up_count_impl1/MachXO3LF_Hitless_Update_demo_original_

```
31.v(82,1-87,10) (VERI-9000) elaborating module 'BB_uniq_4'
INFO -
D:/lscc/diamond/3.9/ispfpga/userware/NT/SYNTHESIS_HEADERS/machxo
31.v(82,1-87,10) (VERI-9000) elaborating module 'BB_uniq_5'
INFO -
D:/lscc/diamond/3.9/ispfpga/userware/NT/SYNTHESIS_HEADERS/machxo
31.v(82,1-87,10) (VERI-9000) elaborating module 'BB_uniq_6'
INFO -
D:/lscc/diamond/3.9/ispfpga/userware/NT/SYNTHESIS_HEADERS/machxo
31.v(82,1-87,10) (VERI-9000) elaborating module 'BB_uniq_7'
INFO -
D:/lscc/diamond/3.9/ispfpga/userware/NT/SYNTHESIS_HEADERS/machxo
31.v(82,1-87,10) (VERI-9000) elaborating module 'BB_uniq_8'
Done: design load finished with (0) errors, and (0) warnings
```

```
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_sei_sed_sec_demo_design/hardw
are/implementation/sei_sed_sec_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
>
```

Figure 7.2. Setting *original_up_count_impl1* Active

3. Run the Synthesize phase on the design to make sure there are no errors. When you see the green checkbox beside Synthesize Design, click **Spreadsheet View**.
4. In the **Global Preferences** tab, make sure that the **ENABLE_TRANSFR** feature is enabled. Save any changes to Spreadsheet View using **File > Save.**



```
MachXO3LF_Hitless_Update_demo
    LCMXO3LF-9400C-6BG484C
    Strategies
        Area
        I/O Assistant
        Quick
        Timing
        Strategy1
    new_down_cnt_impl2
    original_up_count_impl1
        Input Files
            ../source/HITLESS_TOP.v
            ../source/MESSAGE_CONTROL.v
            ../source/original_up_count_impl1/USER_DESIGN.v
        Synthesis Constraint Files
        LPF Constraint Files
            MachXO3LF_Hitless_Update_demo.lpf
        Debug Files
        Script Files
```

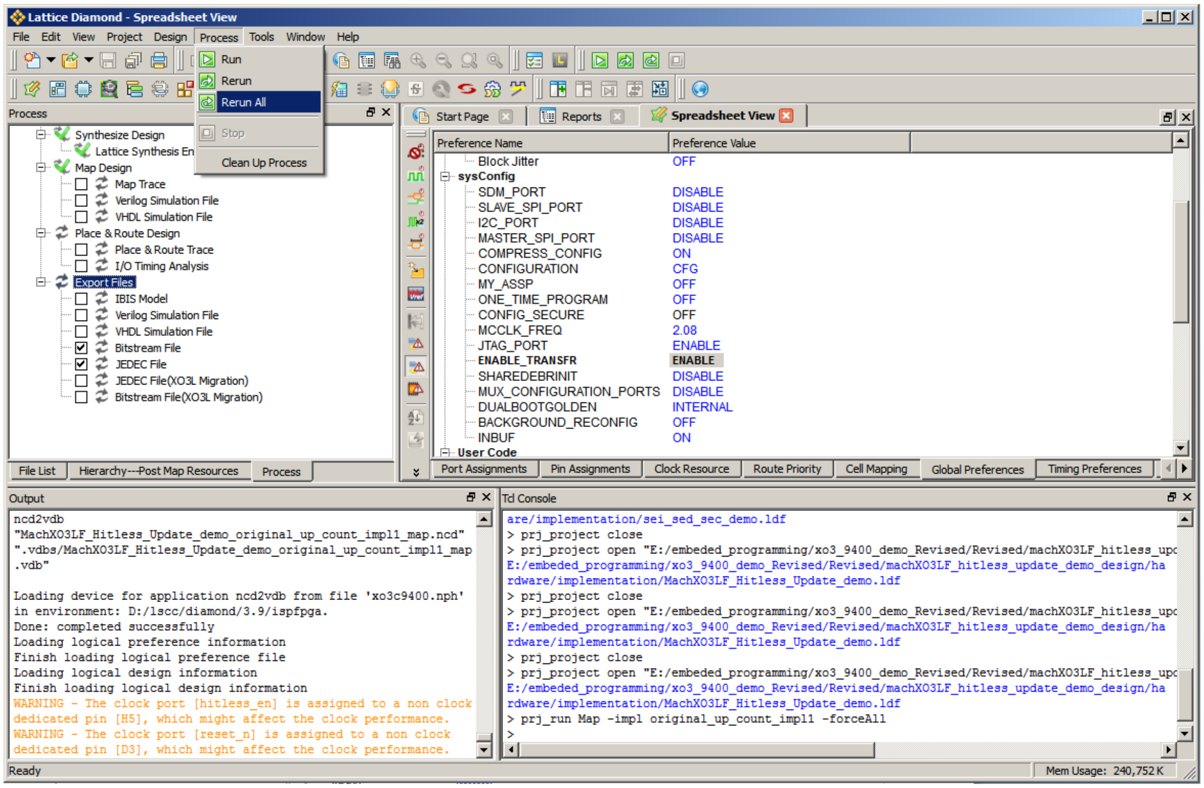
Preference Name	Preference Value
Block Jitter	OFF
sysConfig	
SDM_PORT	DISABLE
SLAVE_SPI_PORT	DISABLE
I2C_PORT	DISABLE
MASTER_SPI_PORT	DISABLE
COMPRESS_CONFIG	ON
CONFIGURATION	CFG
MY_ASSP	OFF
ONE_TIME_PROGRAM	OFF
CONFIG_SECURE	OFF
MCCLK_FREQ	2.08
JTAG_PORT	ENABLE
ENABLE_TRANSFR	DISABLE DISABLE ENABLE
SHAREDEBRINIT	
MUX_CONFIGURATION_PORTS	
DUALBOOTGOLDEN	INTERNAL
BACKGROUND_RECONFIG	OFF
INBUF	ON
User Code	

```
itless_update_demo_design/hardware/implementation/original_up_co
unt_impl1/MachXO3LF_Hitless_Update_demo_original_up_count_impl1.
ncd.
Design name: HITLESS_TOP
NCD version: 3.3
Vendor:      LATTICE
Device:      LCMXO3LF-9400C
Package:     CABGA484
Performance: 6
Package Status:                     Final          Version 1.5.
Performance Hardware Data Status:   Final          Version 37.4.
Finish loading physical design information
WARNING - The clock port [hitless_en] is assigned to a non clock
dedicated pin [H5], which might affect the clock performance.
WARNING - The clock port [reset_n] is assigned to a non clock
dedicated pin [D3], which might affect the clock performance.
```

```
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_sei_sed_sec_demo_design/hardw
are/implementation/sei_sed_sec_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
>
```

Figure 7.3. Enable Transfer

5. After these preferences are set up, run the project to generate the bitstream. Check the checkbox before Bitstream File and JEDEC File in Process View and click **Export Files**.
6. Select **Process > Rerun All** from the menu bar to run the entire process.



- Synthesize Design
  - Lattice Synthesis En
- Map Design
  - □ Map Trace
  - □ Verilog Simulation File
  - □ VHDL Simulation File
- Place & Route Design
  - □ Place & Route Trace
  - □ I/O Timing Analysis
- Export Files
  - □ IBIS Model
  - □ Verilog Simulation File
  - □ VHDL Simulation File
  - ☑ Bitstream File
  - ☑ JEDEC File
  - □ JEDEC File(XO3L Migration)
  - □ Bitstream File(XO3L Migration)

Preference Name	Preference Value
Block Jitter	OFF
sysConfig	
SDM_PORT	DISABLE
SLAVE_SPI_PORT	DISABLE
I2C_PORT	DISABLE
MASTER_SPI_PORT	DISABLE
COMPRESS_CONFIG	ON
CONFIGURATION	CFG
MY_ASSP	OFF
ONE_TIME_PROGRAM	OFF
CONFIG_SECURE	OFF
MCCLK_FREQ	2.08
JTAG_PORT	ENABLE
ENABLE_TRANSFR	**ENABLE**
SHAREDEBRINIT	DISABLE
MUX_CONFIGURATION_PORTS	DISABLE
DUALBOOTGOLDEN	INTERNAL
BACKGROUND_RECONFIG	OFF
INBUF	ON
User Code	

```
ncd2vdb
"MachXO3LF_Hitless_Update_demo_original_up_count_impl1_map.ncd"
".vdbs/MachXO3LF_Hitless_Update_demo_original_up_count_impl1_map
.vdb"

Loading device for application ncd2vdb from file 'xo3c9400.nph'
in environment: D:/lscc/diamond/3.9/ispfpga.
Done: completed successfully
Loading logical preference information
Finish loading logical preference file
Loading logical design information
Finish loading logical design information
WARNING - The clock port [hitless_en] is assigned to a non clock
dedicated pin [H5], which might affect the clock performance.
WARNING - The clock port [reset_n] is assigned to a non clock
dedicated pin [D3], which might affect the clock performance.
```

```
are/implementation/sei_sed_sec_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_project close
> prj_project open "E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_upc
E:/embeded_programming/xo3_9400_demo_Revised/Revised/machXO3LF_hitless_update_demo_design/ha
rdware/implementation/MachXO3LF_Hitless_Update_demo.ldf
> prj_run Map -impl original_up_count_impl1 -forceAll
>
```

Figure 7.4. Generating the Bitstream

The rebuilt design can be programmed in the FPGA as described in the Running the Demo section.

References

- DS1047 – MachXO3 Family Data Sheet
- FPGA-EB-02004 – MachXO3LF 9400 Development Board User Guide
- TN1087 – Minimizing System Interruption During Configuration Using TransFR Technology
- TN1279 – MachXO3 Programming and Configuration Usage Guide

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
June 2017	1.0	Initial release.

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