PN7150

High performance NFC controller with integrated firmware, supporting all NFC Forum modes

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317437

Product data sheet
COMPANY PUBLIC

1 Introduction

This document describes the functionality and electrical specification of the NFC Controller PN7150.

Additional documents describing the product functionality further are available for design-in support. Refer to the references listed in this document to get access to the full documentation provided by NXP.

2 General description

Best plug´n play and high-performance full NFC solution PN7150 is a full NFC controller solution with integrated firmware and NCI interface designed for contactless communication at 13.56 MHz. It is compatible with NFC forum requirements.

PN7150 is designed based on learnings from previous NXP NFC device generation. It is the ideal solution for rapidly integrating NFC technology in any application, especially those running O/S environment like Linux and Android, reducing Bill of Material (BOM) size and cost, thanks to:

- Full NFC forum compliancy (see [1]) with small form factor antenna
- Embedded NFC firmware providing all NFC protocols as pre-integrated feature
- Direct connection to the main host or microcontroller, by I^2C-bus physical and NCI protocol
- Ultra-low power consumption in polling loop mode
- Highly efficient integrated power management unit (PMU) allowing direct supply from a battery

PN7150 embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, MIFARE Classic IC-based card and FeliCa card specifications. It embeds an ARM Cortex-M0 microcontroller core loaded with the integrated firmware supporting the NCI 1.0 host communication. It also allows to provide a higher output power by supplying the transmitter output stage from 3.0 V to 4.75 V.

The contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor.

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN7150 can act autonomously if previously configured by the host in such a manner.

PN7150 integrated firmware provides an easy integration and validation cycle as all the NFC real-time constraints, protocols and device discovery (polling loop) are being taken care internally. In few NCI commands, host SW can configure the PN7150 to notify for card or peer detection and start communicating with them.

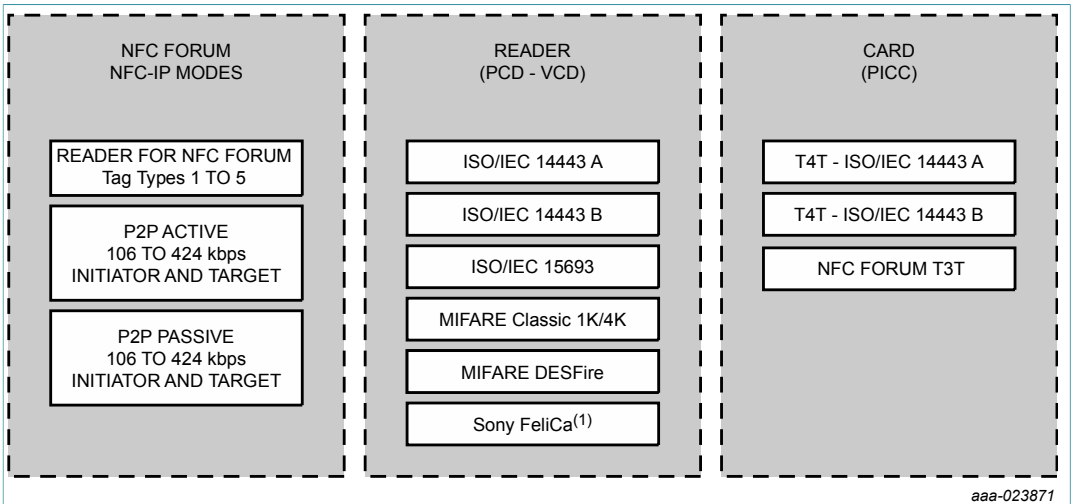


Figure 1. PN7150 transmission modes

1. According to ISO/IEC 18092 (Ecma 340) standard.

3 Features and benefits

- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- ARM Cortex-M0 microcontroller core
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - NFCIP-1, NFCIP-2 protocol (see [8] and [11])
  - ISO/IEC 14443A, ISO/IEC 14443B PICC, NFC Forum T4T modes via host interface (see [3])
  - NFC Forum T3T via host interface
  - ISO/IEC 14443A, ISO/IEC 14443B PCD designed according to NFC Forum digital protocol T4T platform and ISO-DEP (see [1])
  - FeliCa PCD mode
  - MIFARE Classic PCD encryption mechanism (MIFARE Classic 1K/4K)
  - NFC Forum tag 1 to 5 (MIFARE Ultralight, Jewel, Open FeliCa tag, MIFARE DESFire) (see [1])
  - ISO/IEC 15693/ICODE VCD mode (see [9])
- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization (see [2])
  - I^2C-bus High-speed mode (see [4])
- Integrated power management unit
  - Direct connection to a battery (2.3 V to 5.5 V voltage supply range)
  - Support different Hard Power-Down/Standby states activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer and I^2C-bus interface
- Integrated non-volatile memory to store data and executable code for customization

4 Applications

- All devices requiring NFC functionality especially those running in an Android or Linux environment
- TVs, set-top boxes, blu-ray decoders, audio devices
- Home automation, gateways, wireless routers
- Home appliances
- Wearables, remote controls, healthcare, fitness
- Printers, IP phones, gaming consoles, accessories

5 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V	[1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1] [2]	2.7	-	5.5	V
V_{DD}	supply voltage	internal supply voltage		1.65	1.8	1.95	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface					
		• 1.8 V host supply;V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
		• 3 V host supply; V_{SS} = 0 V	[1]	3.0	-	3.6	V
I_{BAT}	battery supply current	in Hard Power Down state;V_{BAT} = 3.6 V; T = 25 °C	[3]	-	10	14	µA
		in Standby state;V_{BAT} = 3.6 V; T = 25 °C		-	20	-	µA
		in Monitor state;V_{BAT} = 2.75 V; T = 25 °C		-	-	14	µA
		in low-power polling loop;V_{BAT} = 3.6 V; T = 25 °C;loop time = 500 ms	[4]	-	150	-	µA
		PCD mode at typical 3 V	[2]	-	-	190	mA
$I_{O(VDDPAD)}$	output current on pin $V_{DD(PAD)}$	total current which can be pulled on $V_{DD(PAD)}$ referenced outputs		-	-	15	mA
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin;$V_{DD(TX)}$ = 3.3 V	[2]	-	180	-	mA
P_{tot}	total power dissipation	Reader; $I_{VDD(TX)}$ = 100 mA;V_{BAT} = 5.5 V		-	-	420	mW
T_{amb}	ambient temperature	JEDEC PCB-0.5		-30	-	+85	°C

[1] V_{SS} represents $V_{SS(PAD)}$ and $V_{SS(TX)}$.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

[3] External clock on NFC_CLK_XTAL1 must be LOW.

[4] See [10] for computing the power consumption as it depends on several parameters.

6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7150B0HN/C110xx[1]	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body; 6 mm × 6 mm × 0.85 mm	SOT618-1
PN7150B0UK/C110xx[1]	WLCSP42	wafer level chip-scale package; 42 bumps; 2.88 mm × 2.80 mm × 0.54 mm (Backside coating included)	SOT1459-1

[1] xx = firmware code variant

7 Marking HVQFN40

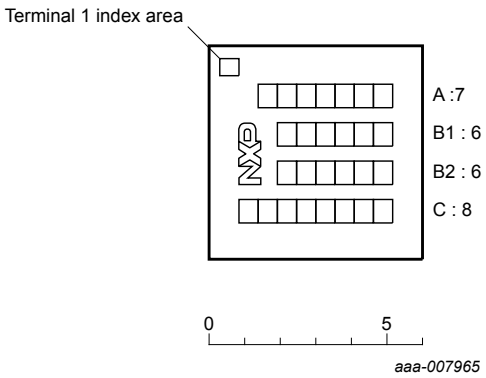


Figure 2. PN7150 package marking HVQFN40 (top view)

Table 3. Marking codes

Type number	Marking code
Line A	7 characters used: basic type number:PN7150x where x is the FW variant
Line B1	6 characters used: diffusion batch sequence number
Line B2	6 characters used: assembly ID number
Line C	7 characters used: manufacturing code including: • diffusion center code: – Z: SSMC – S: Powerchip (PTCT) • assembly center code: – S: ATKH • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

8 Marking WLCSP42

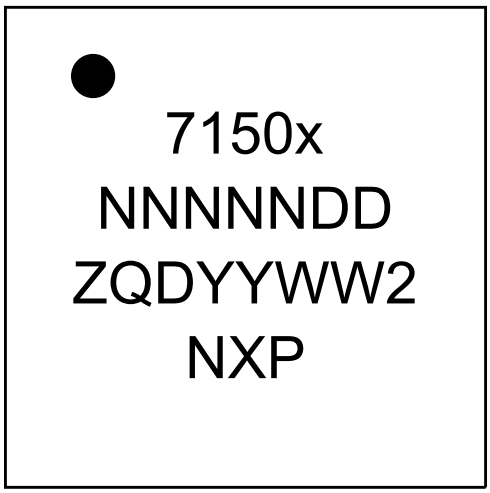


Figure 3. WLCSP42

Table 4. WLCSP package marking (top view)

Line number	Marking code
Line 1	Product identification • Product name: 7150x; where x is the variant.
Line 2	Diffusion batch sequence number • Diffusion fabrication code: NNNNN • Wafer ID: DD
Line 3	Manufacturing code including: • Diffusion center code: – Z: SSMC – s: Global Foundry – S: Powerchip (PTCT) • Assembly center code: – Q: ASE-CL • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • Manufacturing year and week; 4 digits: – YY: year – WW: week code • Mask layout version • Product life cycle status code: – X: not qualified product – Nothing means released product
Line 4	NXP logo

9 Block diagram

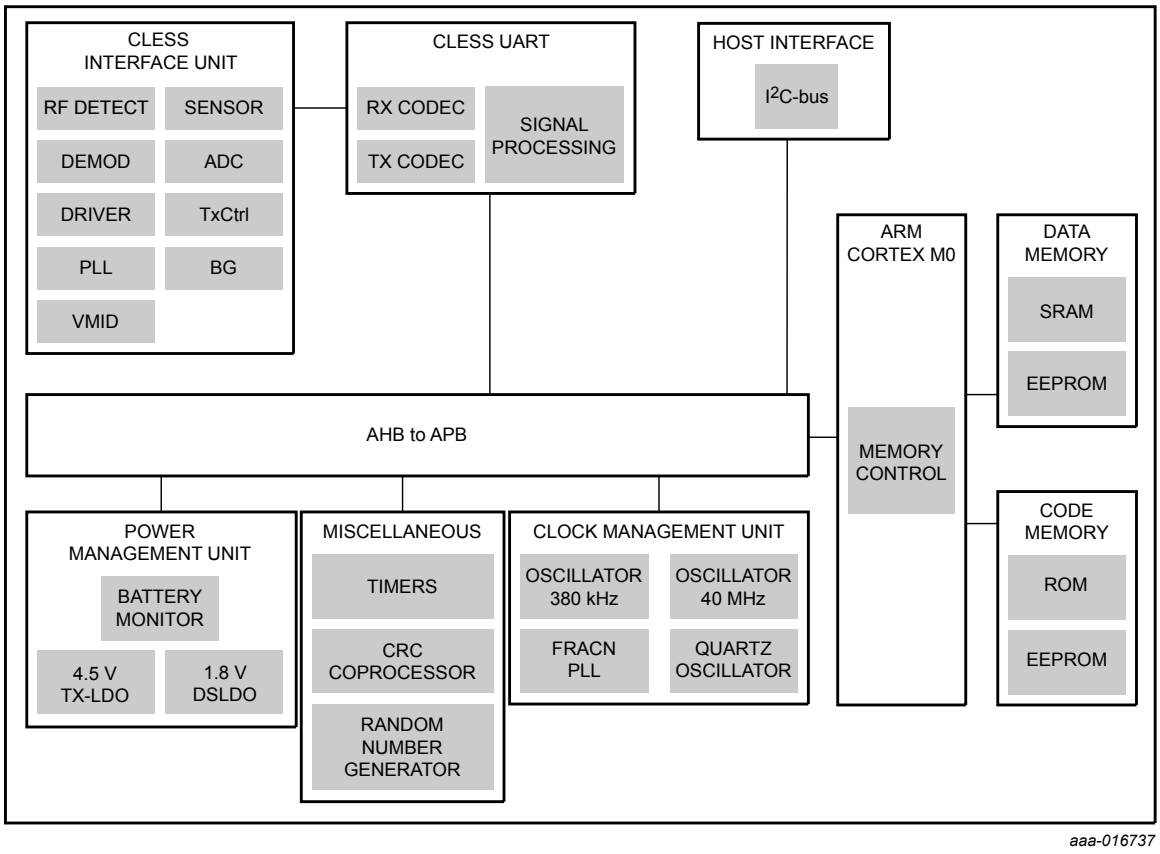


Fig 3. PN7150 block diagram

10 Pinning information

10.1 Pinning HVQFN40

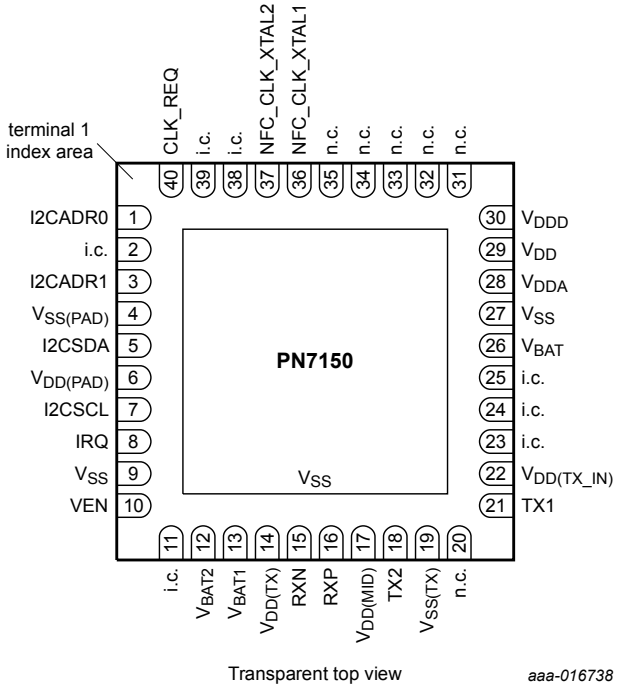


Fig 4. Pinning

Table 5. Pin description

Symbol	Pin	Type[1]	Refer	Description
I2CADR0	1	I	$V_{DD(PAD)}$	I^2C-bus address 0
i.c.	2	-	-	internally connected; must be connected to GND
I2CADR1	3	I	$V_{DD(PAD)}$	I^2C-bus address 1
$V_{SS(PAD)}$	4	G	n/a	pad ground
I2CSDA	5	I/O	$V_{DD(PAD)}$	I^2C-bus data line
$V_{DD(PAD)}$	6	P	n/a	pad supply voltage
I2CSCL	7	I	$V_{DD(PAD)}$	I^2C-bus clock line
IRQ	8	O	$V_{DD(PAD)}$	interrupt request output
V_{SS}	9	G	n/a	ground
VEN	10	I	V_{BAT}	reset pin. Set the device in Hard Power Down
i.c.	11	-	-	internally connected; leave open
V_{BAT2}	12	P	n/a	battery supply voltage; must be connected to V_{BAT}

Symbol	Pin	Type[1]	Refer	Description
V_{BAT1}	13	P	n/a	TXLDO input supply voltage
$V_{DD(TX)}$	14	P	n/a	transmitter supply voltage
RXN	15	I	V_{DD}	negative receiver input
RXP	16	I	V_{DD}	positive receiver input
$V_{DD(MID)}$	17	P	n/a	receiver reference input supply voltage
TX2	18	O	$V_{DD(TX)}$	antenna driver output
$V_{SS(TX)}$	19	G	n/a	contactless transmitter ground
n.c.	20	-	-	not connected
TX1	21	O	$V_{DD(TX)}$	antenna driver output
$V_{DD(TX\_IN)}$	22	P	n/a	transmitter input supply voltage; must be connected to $V_{DD(TX)}$
i.c.	23	-	-	internally connected; leave open
i.c.	24	-	-	internally connected; leave open
i.c.	25	-	-	internally connected; leave open
V_{BAT}	26	P	n/a	battery supply voltage
V_{SS}	27	G	n/a	ground
V_{DDA}	28	P	n/a	analog supply voltage; must be connected to V_{DD}
V_{DD}	29	P	n/a	supply voltage
V_{DDD}	30	P	n/a	digital supply voltage; must be connected to V_{DD}
n.c.	31	-	-	not connected
n.c.	32	-	-	not connected
n.c.	33	-	-	not connected
n.c.	34	-	-	not connected
n.c.	35	-	-	not connected
NFC_CLK_XTAL1	36	I	V_{DD}	oscillator input/PLL input
NFC_CLK_XTAL2	37	O	V_{DD}	oscillator output
i.c.	38	-	-	internally connected; leave open
i.c.	39	-	-	internally connected; leave open
CLK_REQ	40	O	$V_{DD(PAD)}$	clock request pin

[1] P = power supply
G = ground
I = input
O = output
I/O = input/output

10.2 Pinning WLCSP42

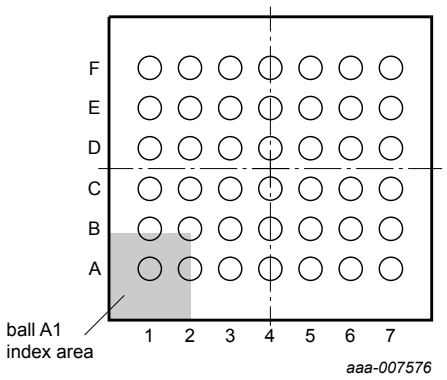


Figure 4. WLCSP42 pinning (bottom view)

Table 6. WLCSP package marking (top view)

Symbol	Pin	Type[1]	Refer	Description
V_{BAT2}	A1	P	n/a	battery supply voltage; to be connected to V_{BAT}
i.c.	A2	-	-	internally connected; leave open
V_{BAT1}	A3	P	n/a	TXLDO input supply voltage
RXN	A4	I	V_{DD}	negative receiver input
$V_{DD(MID)}$	A5	P	n/a	receiver reference input supply voltage
TX2	A6	O	$V_{DD(TX)}$	antenna driver output
TX1	A7	O	$V_{DD(TX)}$	antenna driver output
V_{SS}	B1	G	n/a	ground
V_{SS}	B2	G	n/a	ground
$V_{DD(TX)}$	B3	P	n/a	transmitter supply voltage
RXP	B4	I	V_{DD}	positive receiver input
V_{SS}	B5	G	n/a	ground
$V_{SS(TX)}$	B6	G	n/a	contactless transmitter ground
$V_{DD(TX\_IN)}$	B7	P	n/a	transmitter input supply voltage; must be connected to $V_{DD(TX)}$
IRQ	C1	O	$V_{DD(PAD)}$	interrupt request output
$V_{DD(PAD)}$	C2	P	n/a	pad supply voltage
VEN	C3	I	V_{BAT}	reset pin. Set the device in Hard Power Down
V_{SS}	C4	G	n/a	power ball. Shall be connected to ground for dissipation
V_{SS}	C5	G	n/a	power ball. Shall be connected to ground for dissipation
i.c.	C6	-	-	internally connected; leave open
i.c.	C7	-	-	internally connected; leave open
I2CSCL	D1	I	$V_{DD(PAD)}$	I^2C-bus clock line
I2CSDA	D2	I/O	$V_{DD(PAD)}$	I^2C-bus data line
CLK_REQ	D3	O	$V_{DD(PAD)}$	clock request pin

Symbol	Pin	Type[1]	Refer	Description
i.c.	D4	-	-	internally connected; leave open
i.c.	D5	-	-	internally connected; leave open
V_{DDD}	D6	P	n/a	digital supply voltage; must be connected to V_{DD}
V_{BAT}	D7	P	n/a	battery supply voltage
$V_{SS(PAD)}$	E1	G	n/a	pad ground
I2CADR1	E2	I	$V_{DD(PAD)}$	I^2C-bus address 1
i.c.	E3	-	-	internally connected; leave open
NFC_CLK_XTAL1	E4	I	V_{DD}	oscillator input/PLL input
i.c.	E5	-	-	internally connected; leave open
i.c.	E6	-	-	internally connected; leave open
V_{DD}	E7	P	n/a	LDO output supply voltage
I2CADR0	F1	I	$V_{DD(PAD)}$	I^2C-bus address 0
i.c.	F2	-	-	internally connected; must be connected to GND
NFC_CLK_XTAL2	F3	O	V_{DD}	oscillator output
i.c.	F4	-	-	internally connected; leave open
i.c.	F5	-	-	internally connected; must be connected to GND
i.c.	F6	-	-	internally connected; leave open
i.c.	F7	-	-	internally connected; leave open

[1] P = power supply
G = ground
I = input
O = output
I/O = input/output

11 Functional description

PN7150 can be connected on a host controller through I^2C-bus. The logical interface towards the host baseband is NCI-compliant [2] with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in [5].

Moreover, PN7150 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode.

In the following chapters you will find also more details about PN7150 with references to very useful application note such as:

- PN7150 User Manual ([5]):
  User Manual describes the software interfaces (API) based on the NFC forum NCI standard. It does give full description of all the NXP NCI extensions coming in addition to NCI standard ([2]).
- PN7150 Hardware Design Guide ([6]):
  Hardware Design Guide provides an overview on the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption so to enhance the battery lifetime.
- PN7150 Antenna and Tuning Design Guide ([7]):
  Antenna and Tuning Design Guide provides some guidelines regarding the way to design an NFC antenna for the PN7150 chip.
  It also explains how to determine the tuning/matching network to place between this antenna and the PN7150.
  Standalone antenna performances evaluation and final RF system validation (PN7150 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.
- PN7150 Low-Power Mode Configuration ([10]):
  Low-Power Mode Configuration documentation provides guidance on how PN7150 can be configured in order to reduce current consumption by using Low-power polling mode.

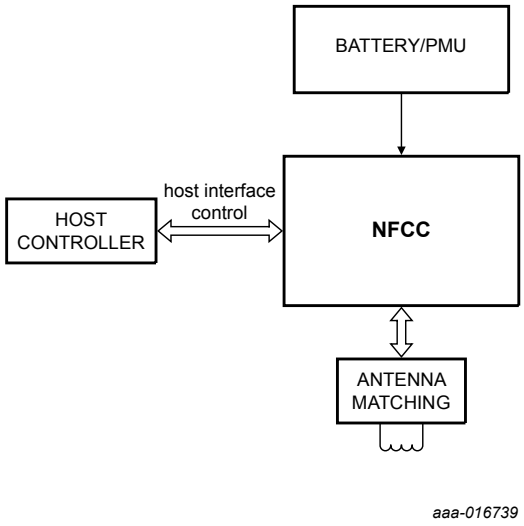


Fig 5. PN7150 connection

11.1 System modes

11.1.1 System power modes

PN7150 is designed in order to enable the different power modes from the system.

2 power modes are specified: Full power mode and Power Off mode.

Table 7. System power modes description

System power mode	Description
Full power mode	the main supply (V_{BAT}) as well as the host interface supply ($V_{DD(PAD)}$) is available, all use cases can be executed
Power Off mode	the system is kept Hard Power Down (HPD)

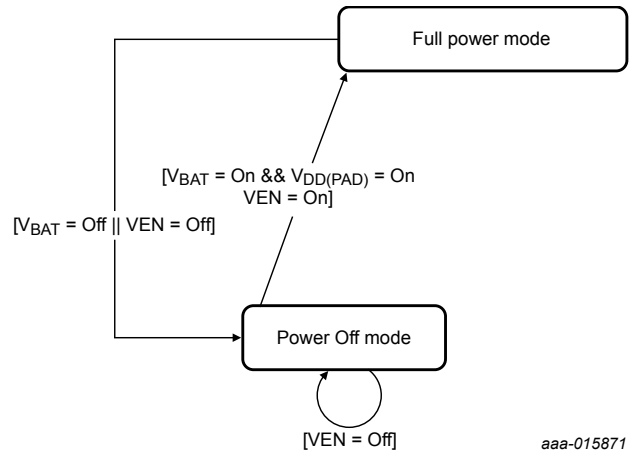


Fig 6. System power mode diagram

Table 6 summarizes the system power mode of the PN7150 depending on the status of the external supplies available in the system:

Table 8. System power modes configuration

V_{BAT}	VEN	Power mode
Off	X	Power Off mode
On	Off	Power Off mode
On	On	Full power mode

Depending on power modes, some application states are limited:

Table 9. System power modes description

System power mode	Allowed communication modes
Power Off mode	no communication mode available
Full power mode	Reader/Writer, Card Emulation, P2P modes

11.1.2 PN7150 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system thus extend the power modes.

4 power states are specified: Monitor, Hard Power Down (HPD), Standby, Active.

Table 10. PN7150 power states

Power state name	Description
Monitor	The PN7150 is supplied by V_{BAT} which voltage is below its programmable critical level, VEN voltage > 1.1 V and the Monitor state is enabled. The system power mode is Power Off mode.

Power state name	Description
Hard Power Down	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled and PN7150 is kept in Hard Power Down (VEN voltage is kept low by host or SW programming) to have the minimum power consumption. The system power mode is in Power Off.
Standby	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when the Monitor state is enabled, VEN voltage is high (by host or SW programming) and minimum part of PN7150 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field,Host interface. The system power mode is Full power mode.
Active	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled, VEN voltage is high (by host or SW programming) and the PN7150 internal blocks are supplied. 3 functional modes are defined: Idle, Target and Initiator. The system power mode is Full power mode.

At application level, the PN7150 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN7150 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of the PN7150 based NFC solution and possibility to restrict parts of the PN7150 functionality.

11.1.2.1 Monitor state

In Monitor state, the PN7150 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 27.

11.1.2.2 Hard Power Down (HPD) state

The Hard Power Down state is entered when $V_{DD(PAD)}$ and V_{BAT} are high by setting VEN voltage < 0.4 V. As these signals are under host control, the PN7150 has no influence on entering or exiting this state.

11.1.2.3 Standby state

Active state is PN7150's default state after boot sequence in order to allow a quick configuration of PN7150. It is recommended to change the default state to Standby state after first boot in order to save power. PN7150 can switch to Standby state autonomously (if configured by host).

In this state, PN7150 most blocks including CPU are no more supplied. Number of wake-up sources exist to put PN7150 into Active state:

- I^2C-bus interface wake-up event
- Antenna RF level detector
- Internal timer event when using polling loop (380 kHz Low-power oscillator is enabled)

If wake-up event occurs, PN7150 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

11.1.2.4 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different functional modes: Idle, Poller and Target.

Table 11. Functional modes in active state

Functional modes	Description
Idle	the PN7150 is active and allows host interface communication. The RF interface is not activated.
Listener	the PN7150 is active and is configured for listening to external device.
Poller	the PN7150 is active and is configured in Poller mode. It polls external device

Poller mode

In this mode, PN7150 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN7150 will switch to active battery mode (that is, switch off RF transmitter) to save energy. Poller mode shall be used with 2.7 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Poller mode shall not be used with V_{BAT} < 2.7 V. $V_{DD(PAD)}$ is within its operational range (see Table 1).

Listener mode

In this mode, PN7150 is acting as a card or as an NFC Target. Listener mode shall be used with 2.3 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V.

11.1.2.5 Polling loop

The polling loop will sequentially set PN7150 in different power states (Active or Standby). All RF technologies supported by PN7150 can be independently enabled within this polling loop.

There are 2 main phases in the polling loop:

- Listening phase. The PN7150 can be in Standby power state or Listener mode
- Polling phase. The PN7150 is in Poller mode

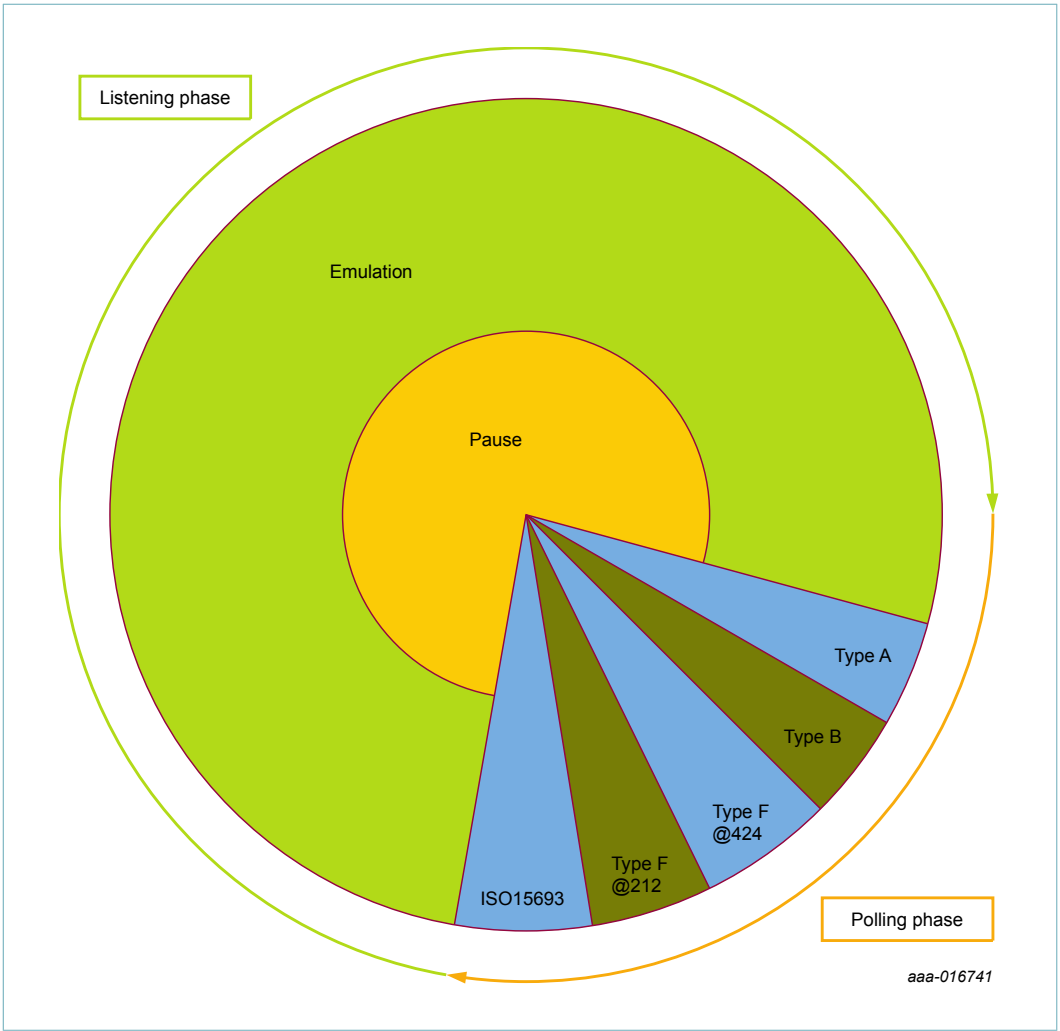


Fig 7. Polling loop: all phases enabled

Listening phase uses Standby power state (when no RF field) and PN7150 goes to Listener mode when RF field is detected. When in Polling phase, PN7150 goes to Poller mode.

To further decrease the power consumption when running the polling loop, PN7150 features a low-power RF polling. When PN7150 is in Polling phase instead of sending regularly RF command, PN7150 senses with a short RF field duration if there is any NFC Target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms (configurable duration, see [5]) listening phase duration, the average power consumption is around 150 µA.

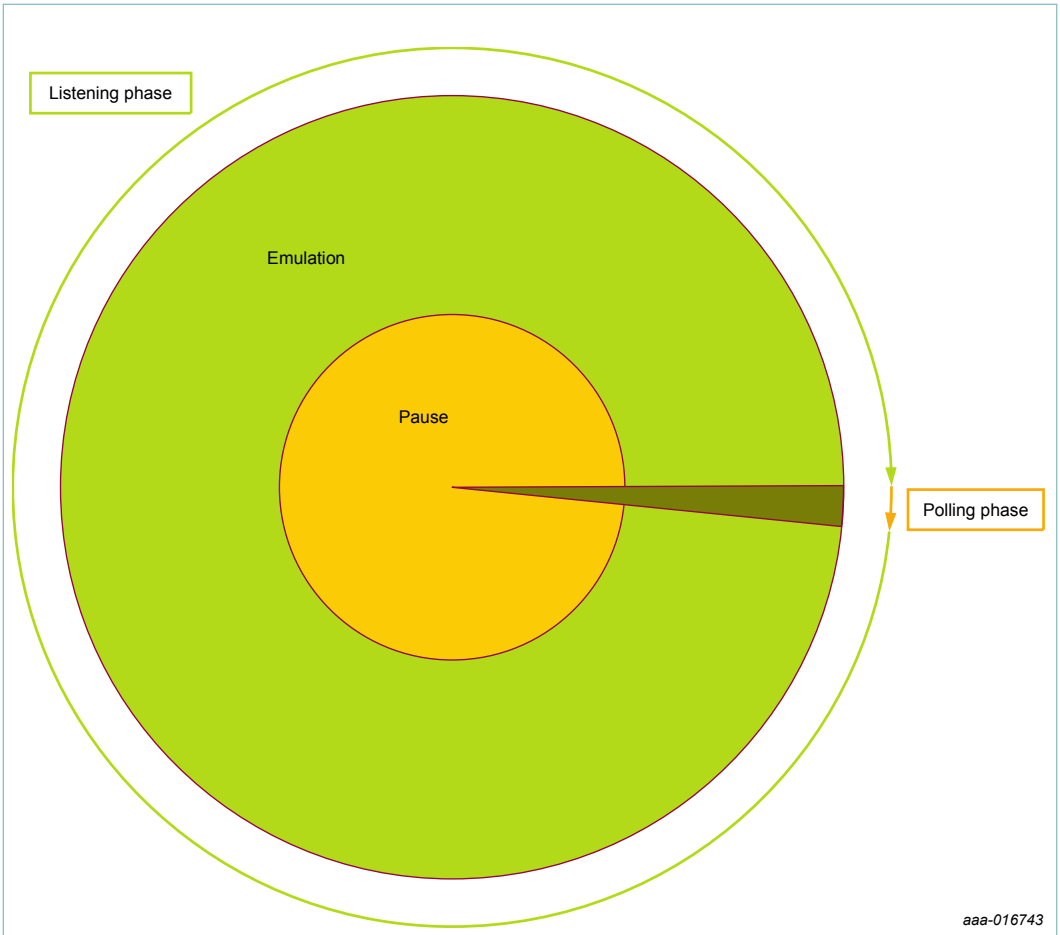


Fig 8. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in [5].

11.2 Microcontroller

PN7150 is controlled via an embedded ARM Cortex-M0 microcontroller core.

PN7150 features integrated in firmware are referenced in [5].

11.3 Host interface

PN7150 provides the support of an I^2C-bus Slave Interface, up to 3.4 MBaud.

The host interface is waken-up on I^2C-bus address.

To enable and ensure data flow control between PN7150 and host controller, additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See [5] for more information.

11.3.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCL), Fast mode (400 kHz SCL) and High-speed mode (3.4 MHz SCL) are supported.

The mains hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN7150 on its address only
- Serial clock synchronization can be used by PN7150 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification [4] except General call, 10-bit addressing and Fast mode Plus (Fm+).

11.3.1.1 I²C-bus configuration

The I²C-bus interface shares four pins with I²C-bus interface also supported by PN7150. When I²C-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 10.

Table 12. Functionality for I²C-bus interface

Pin name	Functionality
I2CADR0	I²C-bus address 0
I2CADR1	I²C-bus address 1
I2CSCL[1]	I²C-bus clock line
I2CSDA[1]	I²C-bus data line

[1] I2CSCL and I2CSDA are not fail-safe and $V_{DD(pad)}$ shall always be available when using the SCL and SDA lines connected to these pins.

PN7150 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, I2CADR1, I2CADR0, R/W.

Table 13. I²C-bus interface addressing

I2CADR1	I2CADR0	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

11.4 PN7150 clock concept

There are 4 different clock sources in PN7150:

- 27.12 MHz clock coming either/or from:

- Internal oscillator for 27.12 MHz crystal connection
- Integrated PLL unit which includes a 1 GHz VCO, taking is reference clock on pin NFC_CLK_XTAL1

- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 40 MHz
- Low-power oscillator 380 kHz

11.4.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN7150 is the time reference for the RF front end when PN7150 is behaving in Reader mode or NFCIP-1 initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 9.

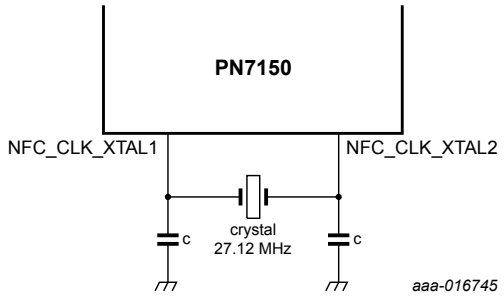


Fig 9. 27.12 MHz crystal oscillator connection

Table 12 describes the levels of accuracy and stability required on the crystal.

Table 14. Crystal requirements

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC and FCC compliancy		-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	full operating range	[1]	-100	-	+100	ppm
		all V_{BAT} range;T = 20 °C	[1]	-50	-	+50	ppm
		all temperature range;V_{BAT} = 3.6 V	[1]	-50	-	+50	ppm
ESR	equivalent series resistance			-	50	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	-	100	µW

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 14 kHz apply.

11.4.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz for an input clock 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

The 27.12 MHz of the PLL is used as the time reference for the RF front end when PN7150 is behaving in Reader mode or ISO/IEC 18092 Initiator as well as in Target when configured in Active Communication mode.

The input clock on NFC_CLK_XTAL1 shall comply with the.following phase noise requirements for the following input frequency: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz:

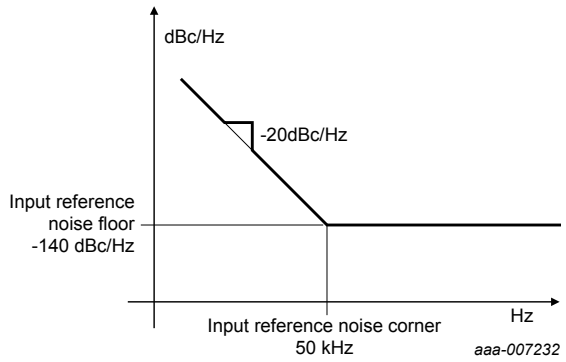


Fig 10. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to [9]. There are 6 pre-programmed and validated frequencies for the PLL: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

Table 15. PLL input requirements

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC and FCC compliancy		-	13	-	MHz
				-	19.2	-	MHz
				-	24	-	MHz
				-	26	-	MHz
				-	38.4	-	MHz
				-	52	-	MHz
$f_{i(ref)acc}$	reference input frequency accuracy	full operating range;frequencies typical values:13 MHz, 26 MHz and 52 MHz	[1]	-25	-	+25	ppm
		full operating range;frequencies typical values:19.2 MHz, 24 MHz and 38.4 MHz	[1]	-50	-	+50	ppm

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
φ_n	phase noise	input noise floor at 50 kHz		-140	-	-	dB/Hz
Sinusoidal shape							
$V_{i(p-p)}$	peak-to-peak input voltage			0.2	-	1.8	V
$V_{i(clk)}$	clock input voltage			0	-	1.8	V
Square shape							
$V_{i(clk)}$	clock input voltage			0	-	1.8 ± 10 %	V

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 400 ppm limits apply.

For detailed description of clock request mechanisms, refer to [5] and [6].

11.4.3 Low-power 40 MHz ± 2.5 % oscillator

Low-power OSC generates a 40 MHz internal clock. This frequency is divided by two to make the system clock.

11.4.4 Low-power 380 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN7150 from Standby state. This allows implementation of low-power reader polling loop at application level. Moreover, this 380 kHz is used as the reference clock for write access to EEPROM memory.

11.5 Power concept

11.5.1 PMU functional description

The Power Management Unit of PN7150 generates internal supplies required by PN7150 out of V_{BAT} input supply voltage:

- V_{DD}: internal supply voltage
- $V_{DD(TX)}$: output supply voltage for the RF transmitter

The Figure 11 describes the main blocks available in PMU:

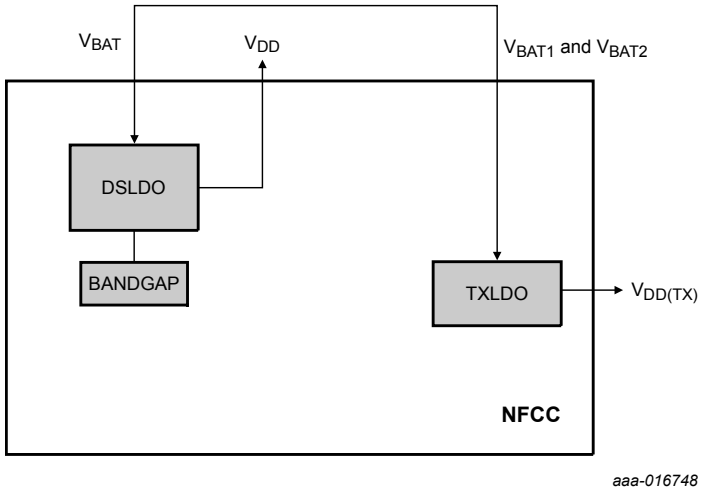


Fig 11. PMU functional diagram

11.5.2 DSLDO: Dual Supply LDO

The input pin of the DSLDO is V_{BAT}.

The Low drop-out regulator provides V_{DD} required in PN7150.

11.5.3 TXLDO

Transmitter voltage can be generated by internal LDO ($V_{DD(TX)}$) or come from an external supply source $V_{DD(TX)}$.

The regulator has been designed to work in 2 configurations:

11.5.3.1 Configuration 1: supply connection in case the battery is used to generate RF field

The Low drop Out Regulator has been designed to generate a 3.0 V, 3.3 V or 3.6 V supply voltage to a transmitter with a current load up to 180 mA.

The output is called $V_{DD(TX)}$. The input supply voltage of this regulator is a battery voltage connected to V_{BAT1} pin.

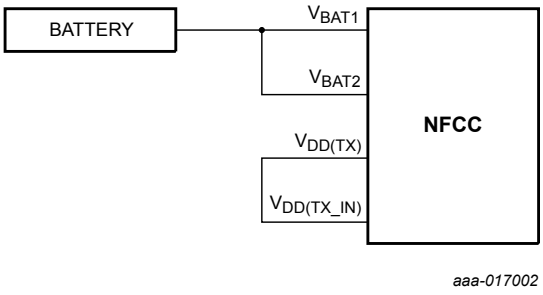


Fig 12. $V_{BAT1} = V_{BAT2}$ (between 2.3 V and 5.5 V)

$V_{DD(TX)}$ value shall be chosen according to the minimum targeted V_{BAT} value for which reader mode shall work.

- If V_{BAT} is above 3.0 V plus the regulator voltage dropout, then $V_{DD(TX)}$ = 3.0 V shall be chosen:

$$V_{BAT} \geq (3.0V + 1\Omega \times load) \Rightarrow V_{DD(TX)} = 3.0V$$

$$3.0V \geq V_{BAT} \geq 2.3V \Rightarrow V_{DD(TX)} = V_{BAT} - 1\Omega \times load$$

- If V_{BAT} is above 3.3 V plus the regulator voltage dropout, then $V_{DD(TX)}$ = 3.3 V shall be chosen:

$$V_{BAT} \geq (3.3V + 1\Omega \times load) \Rightarrow V_{DD(TX)} = 3.3V$$

$$3.3V \geq V_{BAT} \geq 2.3V \Rightarrow V_{DD(TX)} = V_{BAT} - 1\Omega \times load$$

- If V_{BAT} is above 3.6 V plus the regulator voltage dropout, then $V_{DD(TX)}$ = 3.6 V shall be chosen:

$$V_{BAT} \geq (3.6V + 1\Omega \times load) \Rightarrow V_{DD(TX)} = 3.6V$$

$$3.6V \geq V_{BAT} \geq 2.3V \Rightarrow V_{DD(TX)} = V_{BAT} - 1\Omega \times load$$

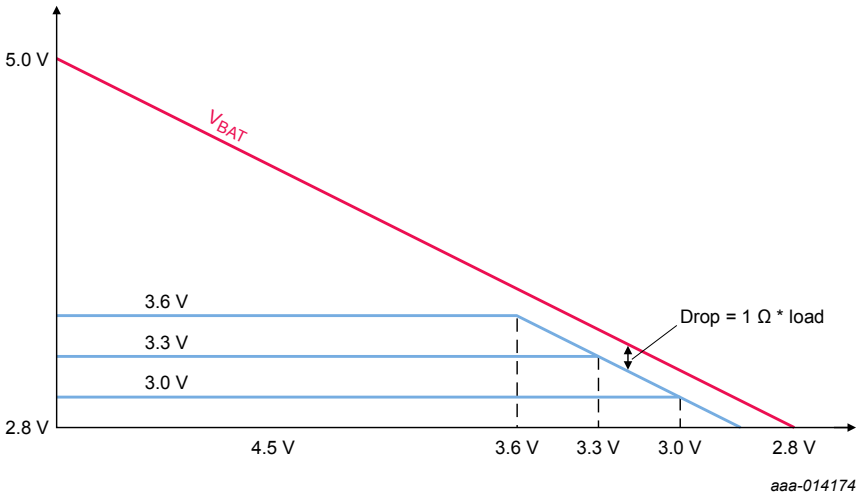


Fig 13. $V_{DD(TX)}$ offset behavior

Figure 13 shows $V_{DD(TX)}$ offset disabled behavior for both cases of $V_{DD(TX)}$ programmed for 3.0 V, 3.3 V or 3.6 V.

In Standby state, whenever $V_{DD(TX)}$ is configured for 3.0 V, 3.3 V or 3.6 V, $V_{DD(TX)}$ is regulated at 2.5 V.

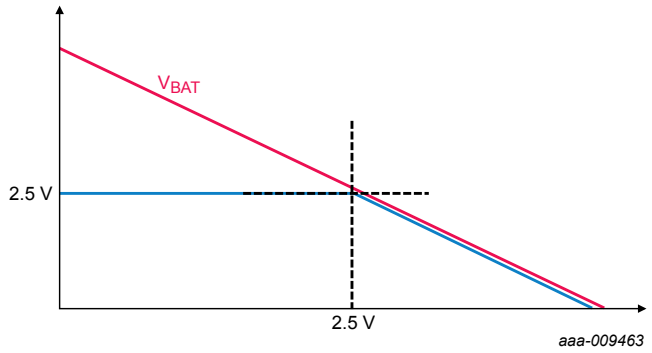


Fig 14. $V_{DD(TX)}$ behavior when PN7150 is in Standby state

Figure 14 shows the case where the PN7150 is in standby state.

11.5.3.2 Configuration 2: supply connection in case a 5 V supply is used to generate RF field with the use of TXLDO

TXLDO has also the possibility to generate 4.75 V or 4.5 V supply in case the supply of this regulator is an external 5 V supply.

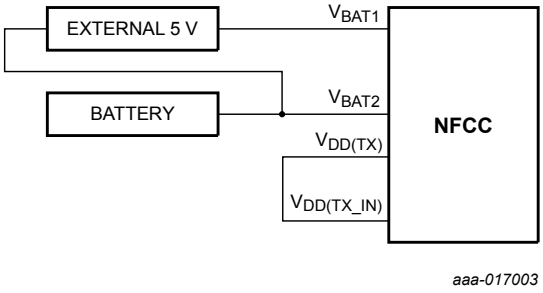


Fig 15. V_{BAT1} = 5 V, V_{BAT2} between 2.3 V and 5.5 V

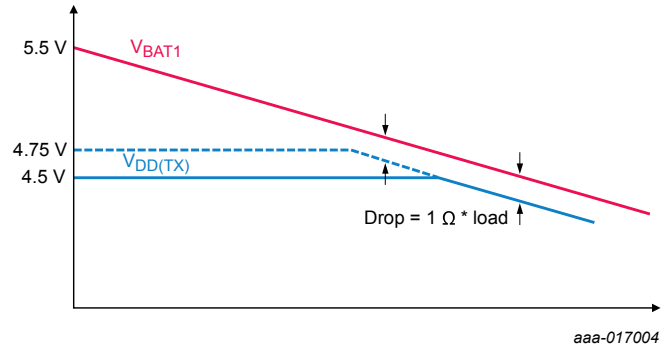


Fig 16. $V_{DD(TX)}$ behavior when PN7150 is supply using external supply on V_{BAT1}

Figure 16 shows the behavior of $V_{DD(TX)}$ depending on V_{BAT1} value.

11.5.3.3 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1, TX2 when in reader or initiator modes.

The current limiter block compares an image of the TXLDO output current to a reference. Once the reference is reached, the output current gets limited which is equivalent to a typical output current of 220 mA whatever V_{BAT} or V_{BAT1} value in the range of 2.3 V to 5.5 V.

11.5.4 Battery voltage monitor

The PN7150 features low-power V_{BAT} voltage monitor which protects mobile device battery from being discharged below critical levels. When V_{BAT} voltage goes below $V_{BATcritical}$ threshold, then the PN7150 goes in Monitor state. Refer to Figure 17 for principle schematic of the battery monitor.

The battery voltage monitor is enabled via an EEPROM setting.

At the first start-up, V_{BAT} voltage monitor functionality is OFF and then enabled if properly configured in EEPROM. The PN7150 monitors battery voltage continuously.

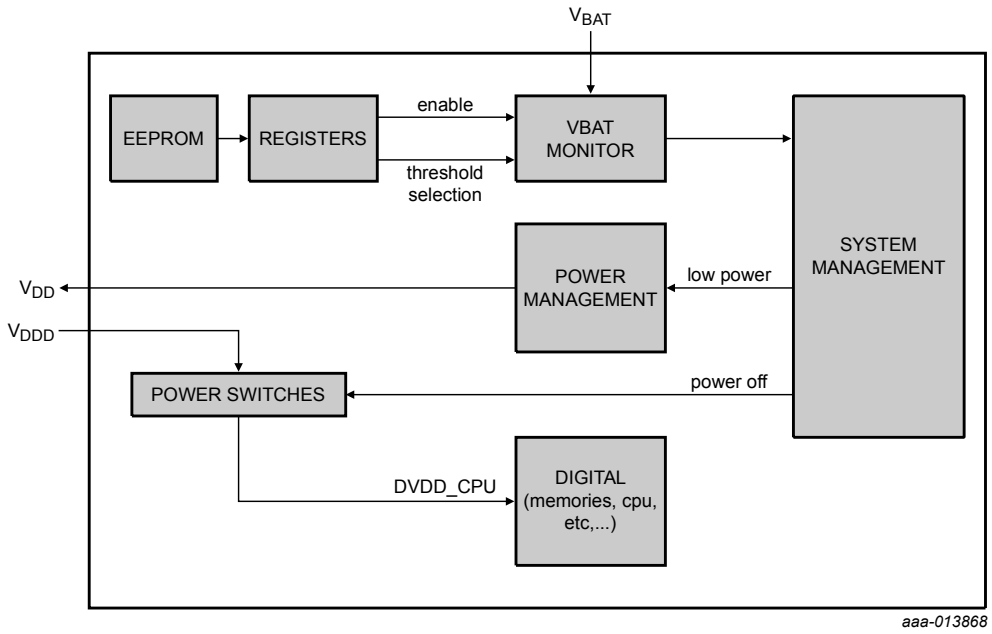


Fig 17. Battery voltage monitor principle

The value of the critical level can be configured to 2.3 V or 2.75 V by an EEPROM setting. This value has a typical hysteresis around 150 mV.

11.6 Reset concept

11.6.1 Resetting PN7150

To enter reset, there are 2 ways:

- Pulling VEN voltage low (Hard Power Down state)
- if V_{BAT} monitor is enabled: lowering V_{BAT} below the monitor threshold (Monitor state, if VEN voltage is kept above 1.1 V)

Reset means resetting the embedded FW execution and the registers values to their default values. Part of these default values is defined from EEPROM data loaded values, others are hardware defined. See [5] to know which ones are accessible to tune PN7150 to the application environment.

To get out of reset:

- Pulling VEN voltage high with V_{BAT} above V_{BAT} monitor threshold if enabled

Figure 18 shows reset done via VEN pin.

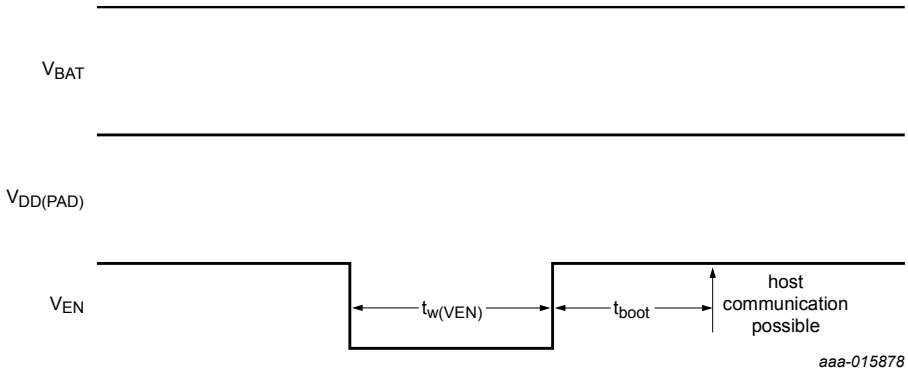


Fig 18. Resetting PN7150 via VEN pin

See Section 15.2.2 for the timings values.

11.6.2 Power-up sequences

There are 2 different supplies for PN7150. PN7150 allows these supplies to be set up independently, therefore different power-up sequences have to be considered.

11.6.2.1 V_{BAT} is set up before $V_{DD(PAD)}$

This is at least the case when V_{BAT} pin is directly connected to the battery and when PN7150 V_{BAT} is always supplied as soon the system is supplied.

As VEN pin is referred to V_{BAT} pin, VEN voltage shall go high after V_{BAT} has been set.

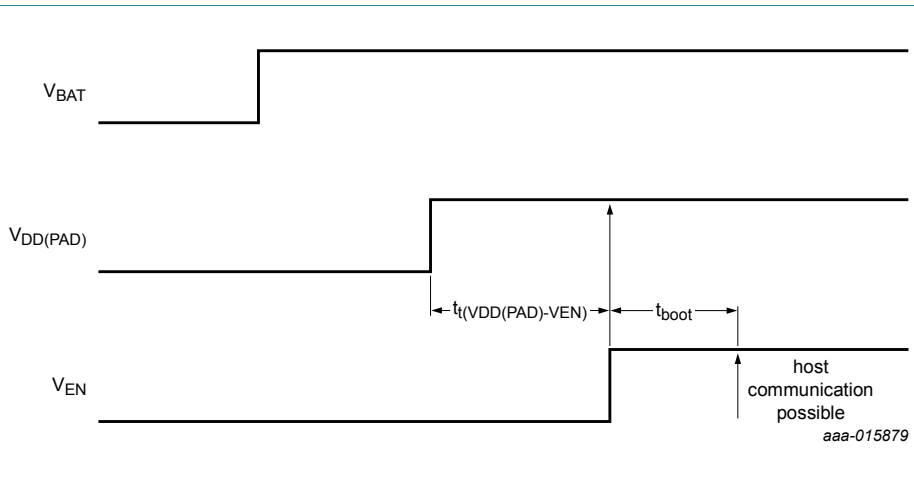


Fig 19. V_{BAT} is set up before $V_{DD(PAD)}$

See Section 15.2.3 for the timings values.

11.6.2.2 $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

It is at least the case when V_{BAT} pin is connected to a PMU/regulator which also supply $V_{DD(PAD)}$.

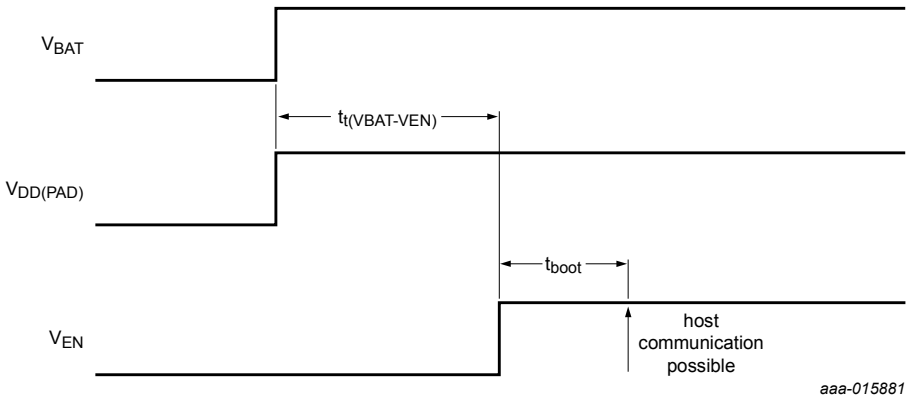


Fig 20. $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

See Section 15.2.3 for the timings values.

11.6.2.3 PN7150 has been enabled before $V_{DD(PAD)}$ is set up or before $V_{DD(PAD)}$ has been cut off

This can be the case when V_{BAT} pin is directly connected to the battery and when $V_{DD(PAD)}$ is generated from a PMU. When the battery voltage is too low, then the PMU might no more be able to generate $V_{DD(PAD)}$. When the device gets charged again, then $V_{DD(PAD)}$ is set up again.

As the pins to select the interface are biased from $V_{DD(PAD)}$, when $V_{DD(PAD)}$ disappears the pins might not be correctly biased internally and the information might be lost. Therefore it is required to make the IC boot after $V_{DD(PAD)}$ is set up again.

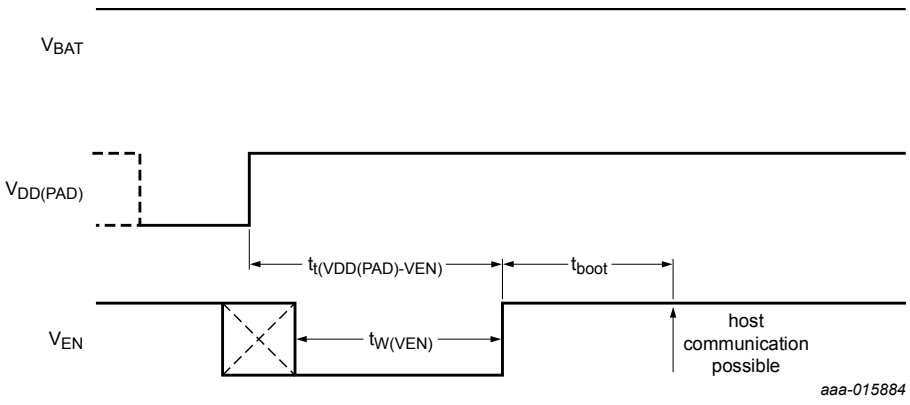
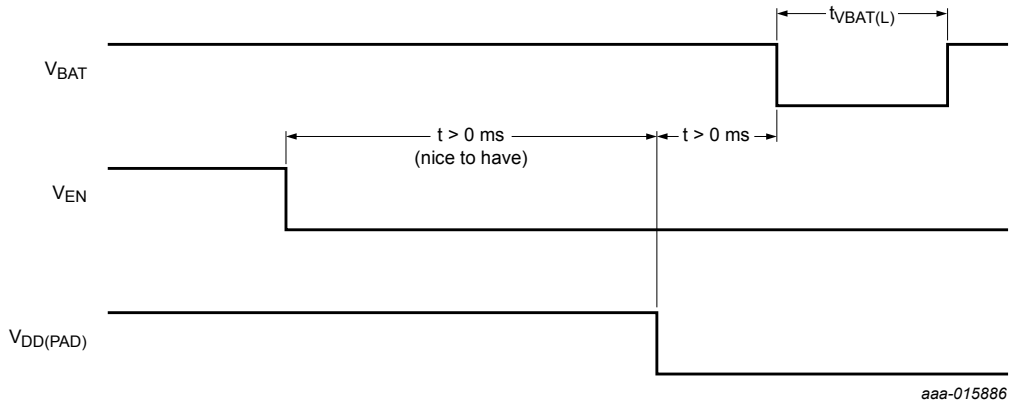


Fig 21. $V_{DD(PAD)}$ is set up or cut-off after PN7150 has been enabled

See Section 15.2.3 for the timings values.

11.6.3 Power-down sequence



PN7150Fig 22. power-down sequence

11.7 Contactless Interface Unit

PN7150 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Remark: *all indicated modulation index and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.*

11.7.1 Reader/Writer communication modes

Generally 5 Reader/Writer communication modes are supported:

- PCD Reader/Writer for ISO/IEC 14443 type A and for MIFARE Classic
- PCD Reader/Writer for Jewel/Topaz
- PCD Reader/Writer for FeliCa
- PCD Reader/Writer for ISO/IEC 14443B
- VCD Reader/Writer for ISO/IEC 15693/ICODE

11.7.1.1 Communication mode for ISO/IEC 14443 type A, MIFARE Classic and Jewel/Topaz PCD

The ISO/IEC 14443A and MIFARE Classic PCD communication mode is the general reader to card communication scheme according to the ISO/IEC 14443A specification. This modulation scheme is as well used for communications with Jewel/Topaz cards.

Figure 23 describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher data rates).

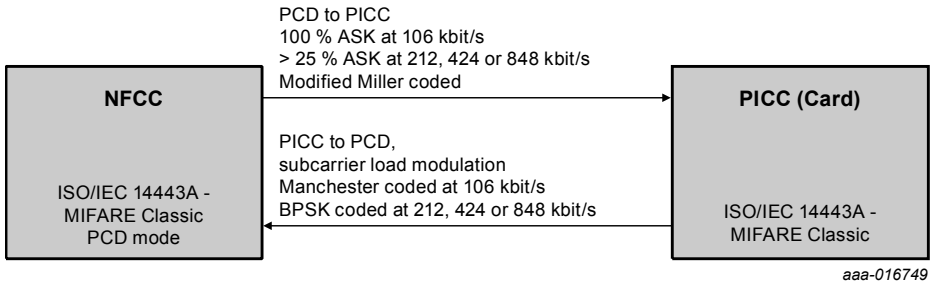


Fig 23. Read/write mode for ISO/IEC 14443 type A and read/write mode for MIFARE Classic

Table 16. Communication overview for ISO/IEC 14443 type A and read/write mode for MIFARE Classic

Communication direction		ISO/IEC 14443A/ MIFARE Classic/ Jewel/ Topaz	ISO/IEC 14443A higher transfer speeds		
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN7150 → PICC					
(data sent by PN7150 to a card)	modulation on PN7150 side	100 % ASK	> 25 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
PICC → PN7150					
(data received by PN7150 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7150 handle the complete ISO/IEC 14443A and MIFARE Classic RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

11.7.1.2 FeliCa PCD communication mode

The FeliCa communication mode is the general Reader/Writer to card communication scheme according to the FeliCa specification. Figure 24 describes the communication on a physical level, the communication overview describes the physical parameters.

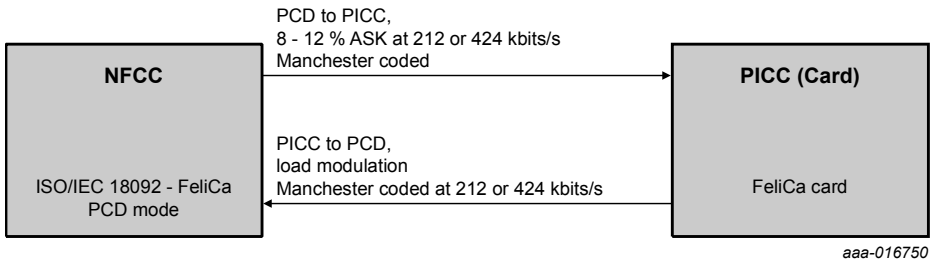


Fig 24. FeliCa Reader/Writer communication mode diagram

Table 17. Overview for FeliCa Reader/Writercommunication mode

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	212 kbit/s	424 kbit/s
	Bit length	(64/13.56) µs	(32/13.56) µs
PN7150 → PICC			
(data sent by PN7150 to a card)	modulation on PN7150 side	8 % - 12 % ASK	8 % - 12 % ASK
	bit coding	Manchester	Manchester
PICC → PN7150			
(data received by PN7150 from a card)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

The contactless coprocessor of PN7150 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

11.7.1.3 ISO/IEC 14443B PCD communication mode

The ISO/IEC 14443B PCD communication mode is the general reader to card communication scheme according to the ISO/IEC 14443B specification. Figure 25 describes the communication on a physical level, the communication table describes the physical parameters.

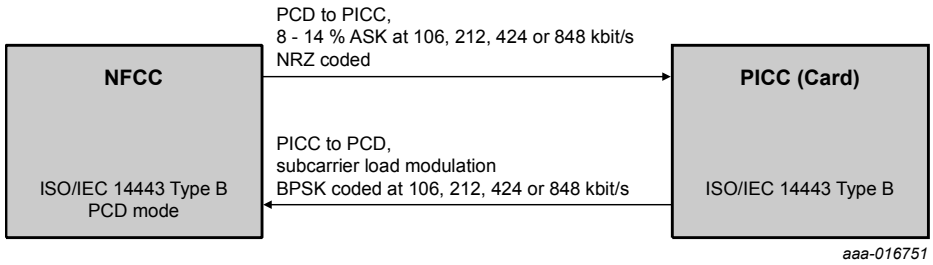


Fig 25. ISO/IEC 14443B Reader/Writer communication mode diagram

Table 18. Overview for ISO/IEC 14443B Reader/Writer communication mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN7150 → PICC					
(data sent by PN7150 to a card)	modulation on PN7150 side	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
PICC → PN7150					
(data received by PN7150 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7150 handles the complete ISO/IEC 14443B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

11.7.1.4 R/W mode for NFC forum Type 5 Tag

The R/W mode for NFC forum Type 5 Tag (T5T) is the general reader to card communication scheme according to the ISO/IEC 15693 specification. PN7150 will communicate with VICC (Type 5 Tag) using only the 26.48 kbit/s with single subcarrier data rate of the VICC.

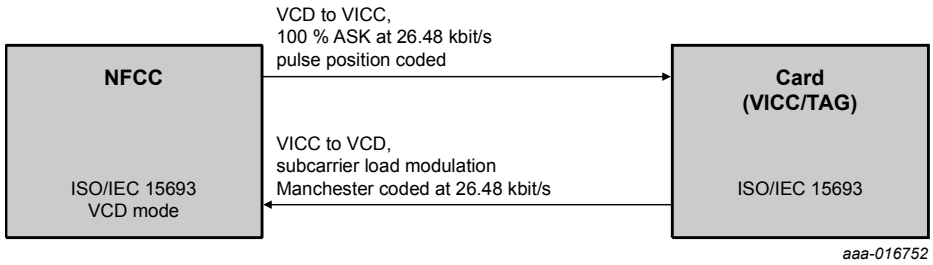


Fig 26. R/W mode for NFC forum T5T communication diagram

Figure 26 and Table 17 show the communication schemes used.

Table 19. Communication overview for NFC forum T5T R/W mode

Communication direction		
PN7150 → VICC		
(data sent by PN7150 to a tag)	transfer speed	26.48 kbit/s
	bit length	(512/13.56) µs
	modulation on PN7150 side	100 % ASK
	bit coding	pulse position modulation 1 out of 4 mode
VICC → PN7150		
(data received by PN7150 from a tag)	transfer speed	26.48 kbit/s
	bit length	(512/13.56) µs
	modulation on VICC side	subcarrier load modulation
	subcarrier frequency	single subcarrier
	bit coding	Manchester

11.7.2 ISO/IEC 18092, Ecma 340 NFCIP-1 communication modes

An NFCIP-1 communication takes place between 2 devices:

- NFC Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- NFC Target: responds to NFC Initiator command either in a load modulation scheme in Passive communication mode or using a self-generated and self-modulated RF field for Active communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data
- Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme. The NFC Initiator is active in terms of generating the RF field.

PN7150 supports the Active Target, Active Initiator, Passive Target and Passive Initiator communication modes at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

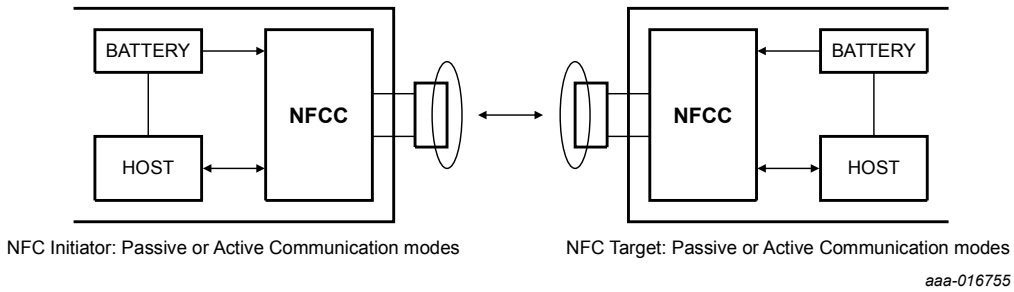


Fig 27. NFCIP-1 communication mode

Nevertheless a dedicated external host has to handle the application layer communication.

11.7.2.1 ACTIVE communication mode

Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data.

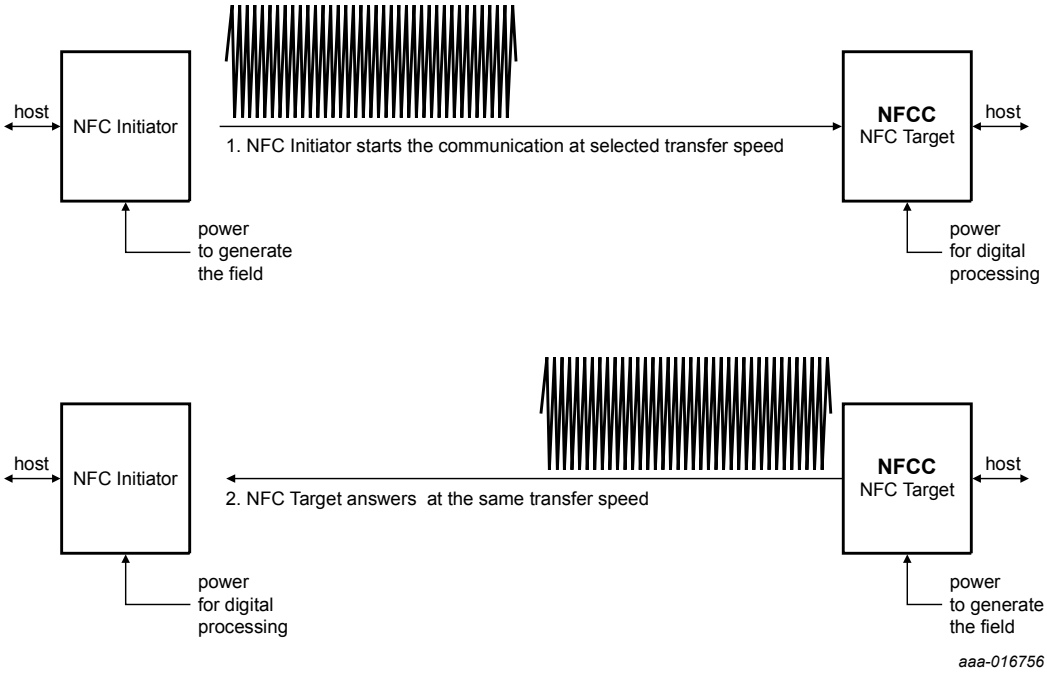


Fig 28. Active communication mode

The following table gives an overview of the Active communication modes:

Table 20. Overview for Active communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
NFC Initiator → NFC Target				
	modulation	100 % ASK	8 % - 30 % ASK[1]	8 % - 30 % ASK[1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target → NFC Initiator				
	modulation	100 % ASK	8 % - 30 % ASK[1]	8 % - 30 % ASK[1]
	bit coding	Miller	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK).

11.7.2.2 Passive communication mode

Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme.

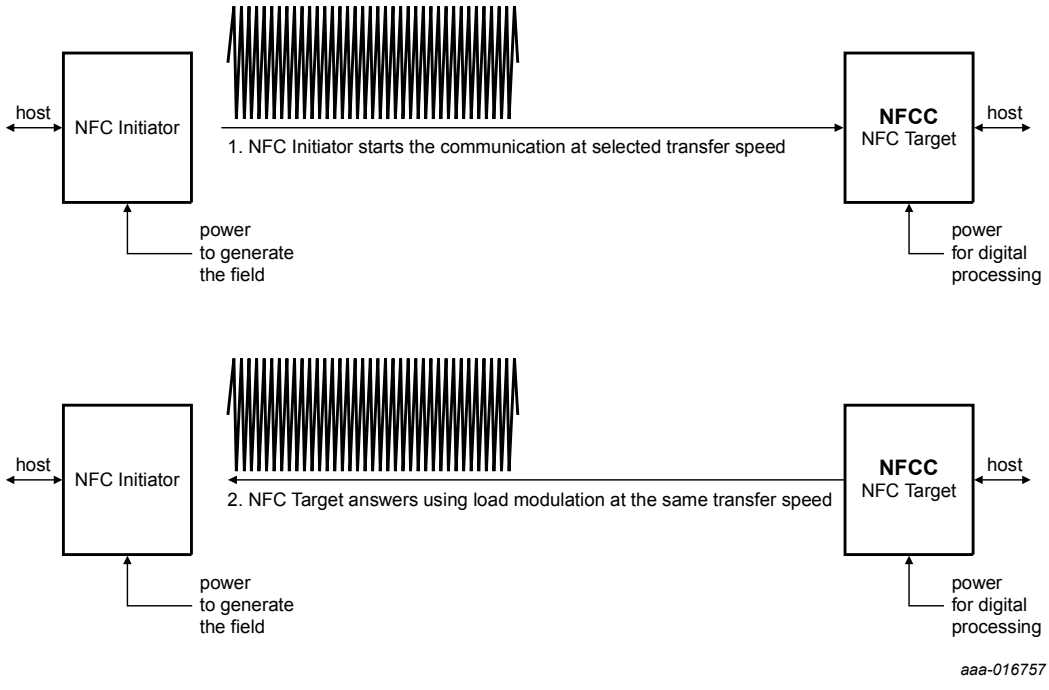


Fig 29. Passive communication mode

Table 19 gives an overview of the Passive communication modes:

Table 21. Overview for Passive communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
NFC Initiator → NFC Target				
	modulation	100 % ASK	8 % - 30 % ASK[1]	8 % - 30 % ASK[1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target → NFC Initiator				
	modulation	subcarrier load modulation	load modulation	load modulation
	subcarrier frequency	13.56 MHz/16	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index, see [7].

11.7.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or Ecma 340.

11.7.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol, refer to the ISO/IEC 18092 or Ecma 340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer

11.7.3 Card communication modes

PN7150 can be addressed as NFC forum T3T and T4T tags. This means that PN7150 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B and the Sony FeliCa interface description.

Remark: *PN7150 does not support a complete card protocol. This has to be handled by the host controller.*

Table 20, Table 21 and Table 22 describe the physical parameters.

11.7.3.1 NFC forum T4T, ISO/IEC 14443Acard mode

Table 22. Overview for NFC forum T4T, ISO/IEC 14443A card mode

Communication direction		ISO/IEC 14443A	ISO/IEC 14443A higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN7150				
(data received by PN7150 from a card)	modulation on PCD side	100 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
PN7150 → PCD				
(data sent by PN7150 to a card)	modulation on PN7150 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK

11.7.3.2 NFC forum T4T, ISO/IEC 14443B card mode

Table 23. Overview for NFC forum T4T, ISO/IEC 14443B card mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN7150				
(data received by PN7150 from a Reader)	modulation on PCD side	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK
	bit coding	NRZ	NRZ	NRZ
PN7150 → PCD				
(data sent by PN7150 to a Reader)	modulation on PN7150 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK

11.7.3.3 NFC forum T3T, Sony FeliCa card mode

Table 24. Overview for NFC forum T3T, Sony FeliCa card mode

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	212 kbit/s	424 kbit/s
	Bit length	(64/13.56) µs	(32/13.56) µs
PCD → PN7150			
(data received by PN7150 from a Reader)	modulation on PN7150 side	8 % - 12 % ASK	8 % - 12 % ASK
	bit coding	Manchester	Manchester
PN7150 → PCD			
(data sent by PN7150 to a Reader)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

11.7.4 Frequency interoperability

When in communication, PN7150 is generating some RF frequencies. PN7150 is also sensitive to some RF signals as it is looking from data in the field.

In order to avoid interference with others RF communication, it is required to tune the antenna and design the board according to [6].

Although ISO/IEC 14443 and ISO/IEC 18092/Ecma 340 allows an RF frequency of 13.56 MHz ± 7 kHz, FCC regulation does not allow this wide spread and limits the dispersion to ± 50 ppm, which is in line with PN7150 capability.

12 Limiting values

Table 25. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface		-	4.35	V
V_{BAT}	battery supply voltage			-	6	V
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF;EIA/JESD22-A114-D		-	1.5	kV
		CDM; field induced model;EIA/JESC22-C101-C		-	500	V
T_{stg}	storage temperature			-55	+150	°C
P_{tot}	total power dissipation	all modes	[1]	-	600	mW
$V_{RXN(i)}$	RXN input voltage			0	2.5	V
$V_{RXP(i)}$	RXP input voltage			0	2.5	V

[1] The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by PN7150 does not exceed this value.

13 Recommended operating conditions

Table 26. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	ambient temperature	JEDEC PCB-0.5		-30	+25	+85	°C
V_{BAT}	battery supply voltage	battery monitor enabled;V_{SS} = 0 V	[1]	2.3	-	5.5	V
		Card Emulation and Passive Target;V_{SS} = 0 V	[1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target;V_{SS} = 0 V	[1] [2]	2.7	-	5.5	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface					
		• 1.8 V host supply;V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
		• 3 V host supply;V_{SS} = 0 V	[1]	3.0	-	3.6	V
P_{tot}	total power dissipation	Reader;$I_{VDD(TX)}$ = 100 mA;V_{BAT} = 5.5 V		-	-	420	mW
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V;T = 25 °C	[3]	-	10	14	µA
		in Standby state;V_{BAT} = 3.6 V; T = 25 °C		-	20	-	µA
		in Monitor state;V_{BAT} = 2.75 V; T = 25 °C		-	-	14	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C;loop time = 500 ms	[4]	-	150	-	µA
		PCD mode at typical 3 V	[5]	-	-	190	mA
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin; $V_{DD(TX)}$ = 3.3 V	[5]	-	180	-	mA

[1] V_{SS} represents $V_{SS(PAD)}$ and $V_{SS(TX)}$.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

[3] External clock on NFC_CLK_XTAL1 must be LOW.

[4] See [10] for computing the power consumption as it depends on several parameters.

[5] The antenna shall be tuned not to exceed the maximum of I_{BAT}.

14 Thermal characteristics

14.1 Thermal characteristics HVQFN40

Table 27. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB		-	40	-	K/W

14.2 Thermal characteristics WLCSP42

Table 28. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB		-	42	-	K/W

15 Characteristics

15.1 Current consumption characteristics

Table 29. Current consumption characteristics for operating ambient temperature range

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; VEN voltage = 0 V		-	10	20	µA
		in Standby state;V_{BAT} = 3.6 V;	[1]	-	20	35	µA
		in Idle and Listener modes; V_{BAT} = 3.6 V		-	4.55	-	mA
		in Poller mode;V_{BAT} = 3.6 V		-	150	-	mA
		in Monitor state;V_{BAT} = 2.75 V	[2]	-	10	20	µA

[1] Refer to Section 10.1.2 for the description of the power modes.

[2] This is the same value for V_{BAT} = 2.3 V when the monitor threshold is set to 2.3 V.

15.2 Functional block electrical characteristics

15.2.1 Battery voltage monitor characteristics

Table 30. Battery voltage monitor characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	set to 2.3 V		2.15	2.3	2.45	V
		set to 2.75 V		2.6	2.75	2.9	V
V_{hys}	hysteresis voltage			100	150	200	mV

15.2.2 Reset via VEN

Table 31. Reset timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{W(VEN)}$	VEN pulse width	to reset		10	-	-	µs
t_{boot}	boot time			-	-	2.5	ms

15.2.3 Power-up timings

Table 32. Power-up timings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{t(VBAT-VEN)}$	transition time from pin V_{BAT} to pin VEN	V_{BAT}, VEN voltage = HIGH		0	0.5	-	ms

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{t(VDDPAD-VEN)}$	transition time from pin $V_{DD(PAD)}$ to pin VEN	$V_{DD(PAD)}$, VEN voltage = HIGH		0	0.5	-	ms
$t_{t(VBAT-VDDPAD)}$	transition time from pin V_{BAT} to pin $V_{DD(PAD)}$	V_{BAT},$V_{DD(PAD)}$ = HIGH		0	0.5	-	ms

15.2.4 Power-down timings

Table 33. Power-down timings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{VBAT(L)}$	time V_{BAT} LOW			20	-	-	ms

15.2.5 I²C-bus timings

Here below are timings and frequency specifications.

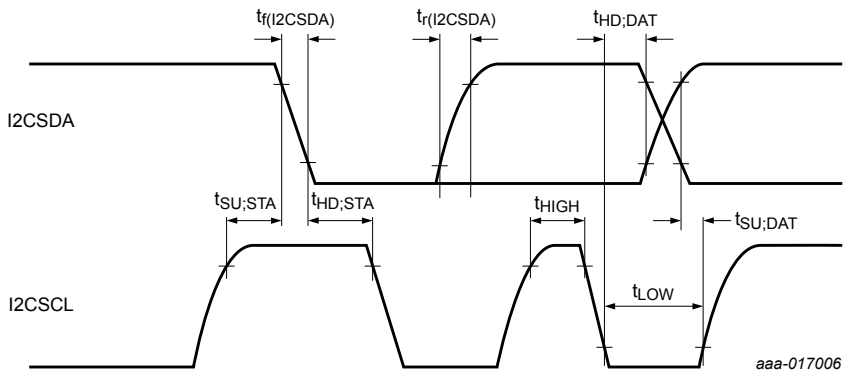


Fig 30. I²C-bus timings

Table 34. High-speed mode I²C-bus timings specification

Symbol	Parameter	Conditions		Min	Max	Unit
$f_{clk(I2CSCL)}$	clock frequency on pin I2CSCL	I²C-bus SCL;C_b < 100 pF		0	3.4	MHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 100 pF		160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 100 pF		160	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 100 pF		160	-	ns
t_{HIGH}	HIGH period of the SCL clock	C_b < 100 pF		60	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 100 pF		10	-	ns
$t_{HD;DAT}$	data hold time	C_b < 100 pF		0	-	ns

Symbol	Parameter	Conditions		Min	Max	Unit
$t_{r(I2CSDA)}$	rise time on pin I2CSDA	I^2C-bus SDA;C_b < 100 pF		10	80	ns
$t_{f(I2CSDA)}$	fall time on pin I2CSDA	I^2C-bus SDA;C_b < 100 pF		10	80	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs;C_b < 100 pF		$0.1V_{DD(PAD)}$	-	V

Table 35. Fast mode I^2C-bus timings specification

Symbol	Parameter	Conditions		Min	Max	Unit
$f_{clk(I2CSCL)}$	clock frequency on pin I2CSCL	I^2C-bus SCL;C_b < 400 pF		0	400	kHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 400 pF		600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 400 pF		600	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 400 pF		1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	C_b < 400 pF		600	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 400 pF		100	-	ns
$t_{HD;DAT}$	data hold time	C_b < 400 pF		0	900	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs;C_b < 400 pF		$0.1V_{DD(PAD)}$	-	V

15.3 Pin characteristics

15.3.1 NFC_CLK_XTAL1 and NFC_CLK_XTAL2 pins characteristics

Table 36. Input clock characteristics on NFC_CLK_XTAL1 when using PLL

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage			0.2	-	1.8	V
δ	duty cycle			35	-	65	%

Table 37. Pin characteristics for NFC_CLK_XTAL1 when PLL input

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V		-1	-	+1	µA
V_i	input voltage			-	-	V_{DD}	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage			200	-	-	mV
C_i	input capacitance	all power modes		-	2	-	pF

Table 38. Pin characteristics for 27.12 MHz crystal oscillator

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{i(NFC\_CLK\_XTAL1)}$	NFC_CLK_XTAL1 input capacitance	V_{DD} = 1.8 V		-	2	-	pF
$C_{i(NFC\_CLK\_XTAL2)}$	NFC_CLK_XTAL2 input capacitance			-	2	-	pF

Table 39. PLL accuracy

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{o(acc)}$	output frequency accuracy	deviation added to NFC_CLK_XTAL1 frequency on RF frequency generated;worst case whatever input frequency		-50	-	+50	ppm

15.3.2 VEN input pin characteristics

Table 40. VEN input pin characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage			1.1	-	V_{BAT}	V
V_{IL}	LOW-level input voltage			0	-	0.4	V
I_{IH}	HIGH-level input current	VEN voltage = V_{BAT}		-1	-	+1	µA
I_{IL}	LOW-level input current	VEN voltage = 0 V		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF

15.3.3 Pin characteristics for IRQ and CLK_REQ

Table 41. pin characteristics for IRQ and CLK_REQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA		$V_{DD(PAD)}$ - 0.4	-	$V_{DD(PAD)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA		0	-	0.4	V
C_L	load capacitance			-	-	20	pF
t_f	fall time	C_L = 12 pF max					
		• high speed		1	-	3.5	ns
		• slow speed		2	-	10	ns
t_r	rise time	C_L = 12 pF max					
		• high speed		1	-	3.5	ns
		• slow speed		2	-	10	ns
R_{pd}	pull-down resistance		[1]	0.35	-	0.85	MΩ

[1] Activated in HPD and Monitor states.

15.3.4 Input pin characteristics for RXN and RXP

Table 42. Input pin characteristics for RXN and RXP

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RXN(i)}$	RXN input voltage			0	-	V_{DD}	V
$V_{RXP(i)}$	RXP input voltage			0	-	V_{DD}	V
$C_{i(RXN)}$	RXN input capacitance			-	12	-	pF
$C_{i(RXP)}$	RXP input capacitance			-	12	-	pF
$Z_{i(RXN-VDDMID)}$	input impedance between RXN and $V_{DD(MID)}$	Reader, Card and P2P modes		0	-	15	kΩ
$Z_{i(RXP-VDDMID)}$	input impedance between RXP and $V_{DD(MID)}$	Reader, Card and P2P modes		0	-	15	kΩ
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	Miller coded					
		• 106 kbit/s		-	150	200	mV(p-p)
		• 212 kbit/s to 424 kbit/s		-	150	200	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	Miller coded					
		• 106 kbit/s		-	150	200	mV(p-p)
		• 212 kbit/s to 424 kbit/s		-	150	200	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	Manchester, NRZ or BPSK coded;106 kbit/s to 848 kbit/s		-	150	200	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	Manchester, NRZ or BPSK coded;106 kbit/s to 848 kbit/s		-	150	200	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN dynamic input voltage	All data coding;106 kbit/s to 848 kbit/s		V_{DD}	-	-	V(p-p)
$V_{i(dyn)(RXP)}$	RXP dynamic input voltage	All data coding;106 kbit/s to 848 kbit/s		V_{DD}	-	-	V(p-p)
$V_{i(RF)}$	RF input voltage	RF input voltage detected; Initiator modes			100	-	mV(p-p)

15.3.5 Output pin characteristics for TX1 and TX2

Table 43. Output pin characteristics for TX1 and TX2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TX)}$ = 3.3 V and I_{OH} = 30 mA;PMOS driver fully on		$V_{DD(TX)}$ - 150	-	-	mV
V_{OL}	LOW-level output voltage	$V_{DD(TX)}$ = 3.3 V and I_{OL} = 30 mA;NMOS driver fully on		-	-	200	mV

Table 44. Output resistance for TX1 and TX2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{OL}	LOW-level output resistance	$V_{DD(TX)}$ - 100 mV;CWGsN = 01h		-	-	85	Ω
R_{OL}	LOW-level output resistance	$V_{DD(TX)}$ - 100 mV;CWGsN = 0Fh		-	-	5	Ω
R_{OH}	HIGH-level output resistance	$V_{DD(TX)}$ - 100 mV		-	-	4	Ω

15.3.6 Input pin characteristics for I2CADR0 and I2CADR1

Table 45. Input pin characteristics for I2CADR0 and I2CADR1

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage			0.65$V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage			0	-	0.35$V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	V_I = $V_{DD(PAD)}$		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF

15.3.7 Pin characteristics for I2CSDA and I2CSCL

Table 46. Pin characteristics for I2CSDA and I2CSCL

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	[1]	0	-	0.4	V
C_L	load capacitance			-	-	10	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_f	fall time	C_L = 100 pF;Rpull-up = 2 kΩ;Standard and Fast mode	[1]	30	-	250	ns
t_f	fall time	C_L = 100 pF;Rpull-up = 1 kΩ;High-speed mode	[1]	80	-	110	ns
t_r	rise time	C_L = 100 pF;Rpull-up = 2 kΩ;Standard and Fast mode	[1]	30	-	250	ns
		C_L = 100 pF; Rpull-up = 1 kΩ; High-speed mode	[1]	10	-	100	ns
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage			0	-	$0.3V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(PAD)}$;high impedance		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V;high impedance		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF

[1] Only for pin I2CSDA as I2CSCL is only used as input.

15.3.8 V_{DD} pin characteristic

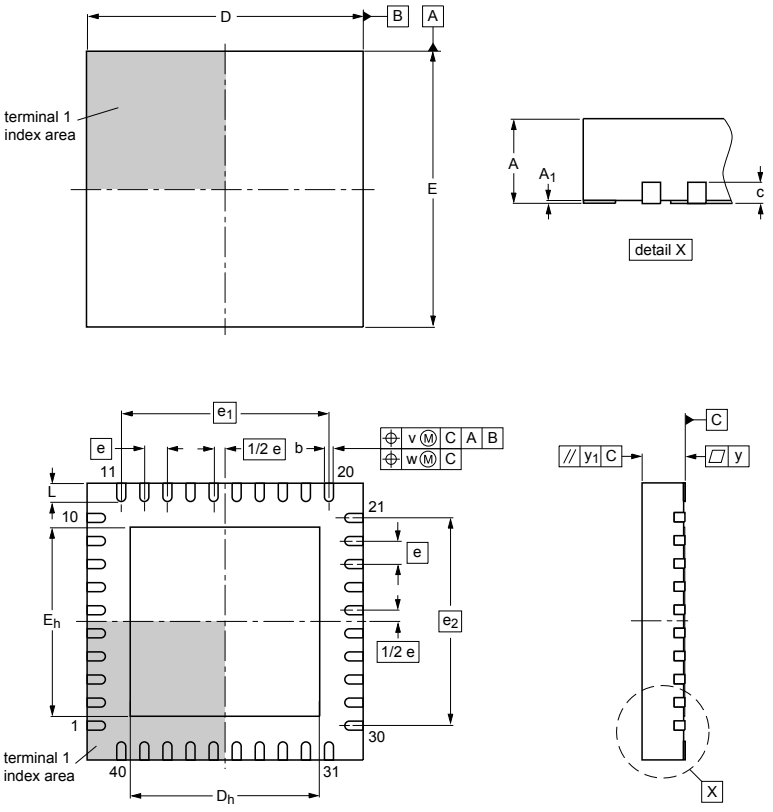
Table 47. Electrical characteristic of V_{DD}

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	V_{DD} supply voltage	V_{SS} = 0 V		1.65	1.8	1.95	V

16 Package outline

16.1 Package outline HVQFN40

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30	0.2	6.1	4.25	6.1	4.25	0.5	4.5	4.5	0.5	0.1	0.05	0.05	0.1
mm	nom	0.85	0.02	0.21		6.0	4.10	6.0	4.10				0.4				
	min	0.80	0.00	0.18		5.9	3.95	5.9	3.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

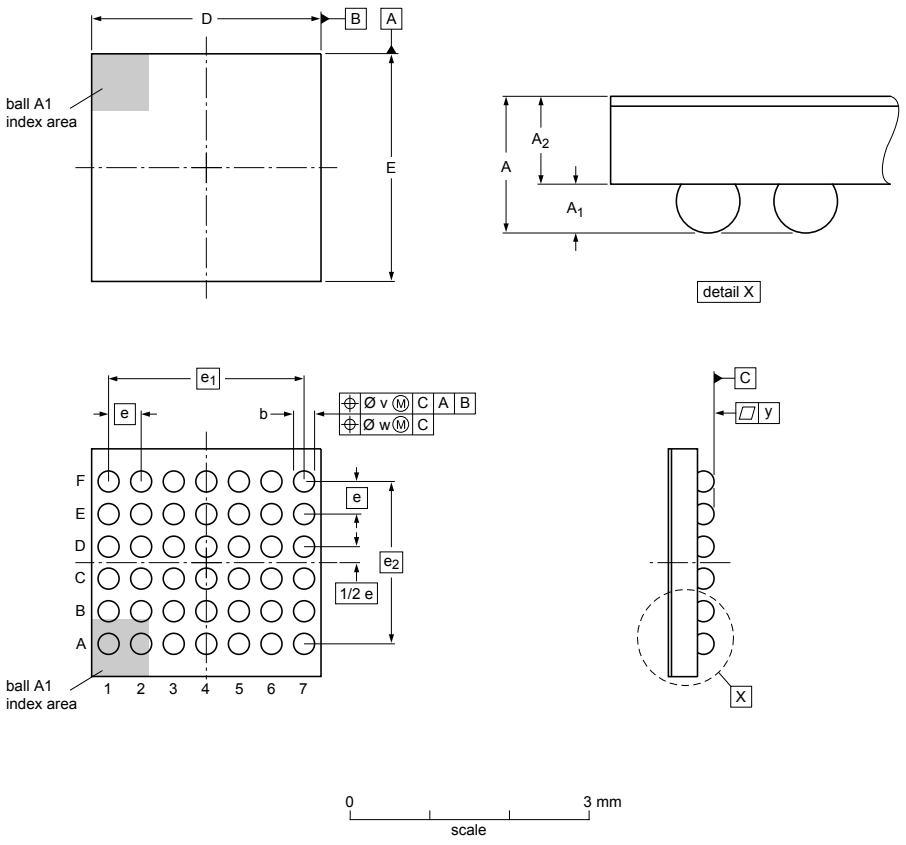
sot618-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-1		MO-220				~~02-10-22~~ 13-11-05

Figure 5. Package outline, HVQFN40, SOT618-1, MSL3

16.2 Package outline WLCSP42

WLCSP42: wafer level chip-scale package; 42 bumps; 2.88 x 2.80 x 0.54 mm (Backside coating included) **SOT1459-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.58	0.23	0.37	0.29	2.90	2.82	0.4	2.4	2.0	0.15	0.05	0.05
	nom	0.54	0.20	0.34	0.26	2.88	2.80						
	min	0.50	0.17	0.31	0.23	2.86	2.78						

Note: Backside coating 40 µm

sot1459-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1459-1	- - -	- - -				~~16-09-01~~ 16-09-02

Figure 6. Package outline, WLCSP42, SOT1459-1

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "Surface mount reflow soldering description".

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 45 and 46

Table 48. SnPb eutectic process (from J-STD-020D)

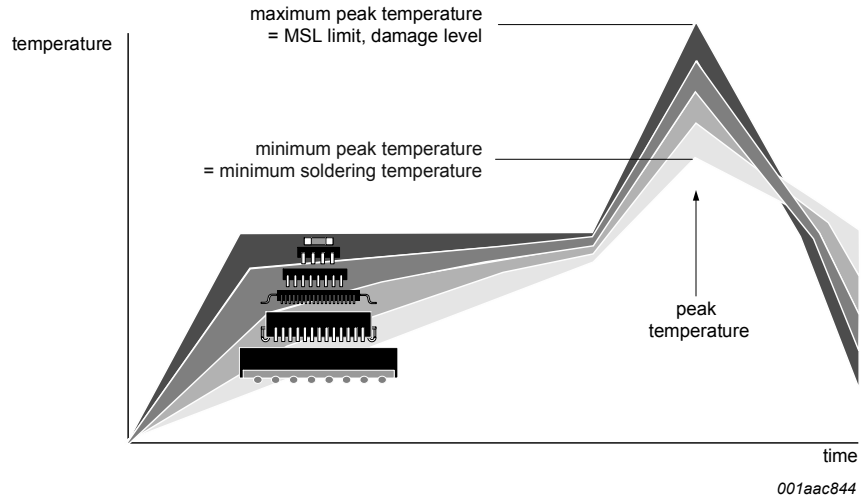
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 49. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

18 Abbreviations

Table 50. Abbreviations

Acronym	Description
API	Application Programming Interface
ASK	Amplitude Shift keying
ASK modulation index	The ASK modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) × 100%
Automatic device discovery	Detect and recognize any NFC peer devices (initiator or target) like: NFC initiator or target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Classic and MIFARE Ultralight PICC, ISO/IEC 15693 VICC
BPSK	Bit Phase Shift Keying
Card Emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller
DEP	Data Exchange Protocol
DSLDO	Dual Supplied LDO
FW	FirmWare
HPD	Hard Power Down
LDO	Low Drop Out
LFO	Low Frequency Oscillator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSL	Moisture Sensitivity Level
NCI	NFC Controller Interface
NFC	Near Field Communication
NFCC	NFC Controller, PN7150 in this data sheet
NFC Initiator	Initiator as defined in ISO/IEC 18092 or ECma 340: NFCIP-1 communication
NFCIP	NFC Interface and Protocol
NFC Target	Target as defined in ISO/IEC 18092 or ECma 340: NFCIP-1 communication
NRZ	Non-Return to Zero
P2P	Peer to Peer
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE Classic
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE Classic
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE Classic
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE Classic
PMOS	P-channel MOSFET
PMU	Power Management Unit

Acronym	Description
PSL	Parameter SeLection
TXLDO	Transmitter LDO
UM	User Manual
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification
VCO	Voltage Controlled Oscillator
VICC	Vicinity Integrated Circuit Card
WUC	Wake-Up Counter

19 References

[1] NFC Forum Device Requirements V1.3
[2] NFC Controller Interface (NCI) Technical Specification V1.0
[3] ISO/IEC 14443 parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)
[4] I^2C Specification, UM10204 rev4 (13/02/2012)
[5] UM10936 PN7150 User Manual
[6] AN11756 PN7150 Hardware Design Guide
[7] AN11755 PN7150 Antenna design and matching guide
[8] ISO/IEC 18092 (NFCIP-1) edition, 15/032013. This is similar to Ecma 340.
[9] ISO/IEC 15693 part 2: 2nd edition (15/12/2006), part 3: 1st edition (01/04/2001)
[10] AN11757 PN7150 Low-Power Mode Configuration
[11] ISO/IEC 21481 (NFCIP-2) edition, 01/07/2012. This is similar to Ecma 352.

20 Revision history

Table 51. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN7150 v3.7	20180424	Product data sheet	-	PN7150 v3.6
Modifications:	• Fixed some cross references in chapter 11.6			
PN7150 v3.6	20171127	Product data sheet	-	PN7150 v3.5
Modifications:	• Minor typos corrected. • Included new product type PN7150B0UK/C11002			
PN7150 v3.5	20171018	Product data sheet	-	PN7150 v3.4
Modifications:	• Table 19 (Communication overview for NFC Forum T5T R/W mode) updated.			
PN7150 v3.4	20171004	Product data sheet	-	PN7150 v3.3
Modifications:	• Descriptive title updated • Section 2: Figure 1 updated • MIFARE branding upated			
PN7150 v3.3	20160704	Product data sheet	-	PN7150 v3.2
Modifications:	• Figure 1: updated. • Section 10.7.1.4: updated. • Section 10.7.3: updated.			
PN7150 v3.2	201600525	Product data sheet	-	PN7150 v3.1
PN7150 v3.1	20160511	Product data sheet	-	PN7150 v3.0
PN7150 v3.0	20151209	Product data sheet	-	PN7150 v2.1
PN7150 v2.1	20151127	Preliminary data sheet	-	PN7150 v2.0
PN7150 v2.0	20150701	Preliminary data sheet	-	PN7150 v1.2
PN7150 v1.2	20150625	Objective data sheet	-	PN7150 v1.1
PN7150 v1.1	20150212	Objective data sheet	-	PN7150 v1.0
PN7150 v1.0	20150129	Objective data sheet	-	-
Modifications:	• Initial version			

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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