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# R8C/3GD Group

Hardware Manual  
Renesas MCU  
R8C Family / R8C/3x Series

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/3GD Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

| Document Type            | Description  | Document Title                              | Document No.         |
|--------------------------|--|---|----------------------|
| Shortsheet               | Hardware overview  | R8C/3GD Group Shortsheet                    | REJ03B0289           |
| Hardware manual          | Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description<br>Note: Refer to the application notes for details on using peripheral functions. | R8C/3GD Group Hardware Manual               | This hardware manual |
| Software manual          | Description of CPU instruction set   | R8C/Tiny Series Software Manual             | REJ09B0001           |
| Application note         | Information on using peripheral functions and application examples<br>Sample programs<br>Information on writing programs in assembly language and C  | Available from Renesas Technology Web site. |                      |
| Renesas technical update | Product specifications, updates on documents, etc.   |   |                      |

## 2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples      the PM03 bit in the PM0 register  
                  P3\_5 pin, VCC pin

(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples      Binary: 11b  
                  Hexadecimal: EFA0h  
                  Decimal: 1234

### 3. Register Notation

The symbols and terms used in register diagrams are described below.

#### x.x.x XXX Register (Symbol)

Address XXXXh

|             |      |      |      |      |    |    |      |      |    |
|-------------|------|------|------|------|----|----|------|------|----|
| Bit         | b7   | b6   | b5   | b4   | b3 | b2 | b1   | b0   |    |
| Symbol      | XXX7 | XXX6 | XXX5 | XXX4 | —  | —  | XXX1 | XXX0 | *1 |
| After Reset | 0    | 0    | 0    | 0    | 0  | 0  | 0    | 0    |    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | XXX0   | XXX bit   | b <sup>1</sup> b <sup>0</sup><br>0 0: XXX<br>0 1: XXX<br>1 0: Do not set.<br>1 1: XXX | R/W |
| b1  | XXX1   |   |   | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |   | —   |
| b3  | —      | Reserved bit  | Set to 0.   | R/W |
| b4  | XXX4   | XXX bit   | Function varies according to the operating mode.                                      | R/W |
| b5  | XXX5   |   |   | W   |
| b6  | XXX6   |   |   | R/W |
| b7  | XXX7   | XXX bit   | 0: XXX<br>1: XXX  | R   |

\*1

- R/W: Read and write.
- R: Read only.
- W: Write only.
- : Nothing is assigned.

\*2

- Reserved bit  
Reserved bit. Set to specified value.

\*3

- Nothing is assigned.  
Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.  
Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.  
The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.



#### 4. List of Abbreviations and Acronyms

| Abbreviation | Full Form                                    |
|--------------|--|
| ACIA         | Asynchronous Communication Interface Adapter |
| bps          | bits per second                              |
| CRC          | Cyclic Redundancy Check                      |
| DMA          | Direct Memory Access                         |
| DMAC         | Direct Memory Access Controller              |
| GSM          | Global System for Mobile Communications      |
| Hi-Z         | High Impedance                               |
| IEBus        | Inter Equipment Bus                          |
| I/O          | Input/Output                                 |
| IrDA         | Infrared Data Association                    |
| LSB          | Least Significant Bit                        |
| MSB          | Most Significant Bit                         |
| NC           | Non-Connection                               |
| PLL          | Phase Locked Loop                            |
| PWM          | Pulse Width Modulation                       |
| SIM          | Subscriber Identity Module                   |
| UART         | Universal Asynchronous Receiver/Transmitter  |
| VCO          | Voltage Controlled Oscillator                |

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# SFR Page Reference

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| 0000h   |  |          |        |
| 0001h   |  |          |        |
| 0002h   |  |          |        |
| 0003h   |  |          |        |
| 0004h   | Processor Mode Register 0                        | PM0      | 23     |
| 0005h   | Processor Mode Register 1                        | PM1      | 157    |
| 0006h   | System Clock Control Register 0                  | CM0      | 90     |
| 0007h   | System Clock Control Register 1                  | CM1      | 91     |
| 0008h   | Module Standby Control Register                  | MSTCR    | 206    |
| 0009h   | System Clock Control Register 3                  | CM3      | 92     |
| 000Ah   | Protect Register                                 | PRCR     | 119    |
| 000Bh   | Reset Source Determination Register              | RSTFR    | 23     |
| 000Ch   | Oscillation Stop Detection Register              | OSD      | 93     |
| 000Dh   | Watchdog Timer Reset Register                    | WDTR     | 157    |
| 000Eh   | Watchdog Timer Start Register                    | WDTS     | 157    |
| 000Fh   | Watchdog Timer Control Register                  | WDTC     | 158    |
| 0010h   |  |          |        |
| 0011h   |  |          |        |
| 0012h   |  |          |        |
| 0013h   |  |          |        |
| 0014h   |  |          |        |
| 0015h   | High-Speed On-Chip Oscillator Control Register 7 | FRA7     | 93     |
| 0016h   |  |          |        |
| 0017h   |  |          |        |
| 0018h   |  |          |        |
| 0019h   |  |          |        |
| 001Ah   |  |          |        |
| 001Bh   |  |          |        |
| 001Ch   | Count Source Protection Mode Register            | CSPR     | 158    |
| 001Dh   |  |          |        |
| 001Eh   |  |          |        |
| 001Fh   |  |          |        |
| 0020h   |  |          |        |
| 0021h   |  |          |        |
| 0022h   |  |          |        |
| 0023h   | High-Speed On-Chip Oscillator Control Register 0 | FRA0     | 94     |
| 0024h   | High-Speed On-Chip Oscillator Control Register 1 | FRA1     | 94     |
| 0025h   | High-Speed On-Chip Oscillator Control Register 2 | FRA2     | 95     |
| 0026h   | On-Chip Reference Voltage Control Register       | OCVREFCR | 330    |
| 0027h   |  |          |        |
| 0028h   | Clock Prescaler Reset Flag                       | CPSRF    | 95     |
| 0029h   | High-Speed On-Chip Oscillator Control Register 4 | FRA4     | 96     |
| 002Ah   | High-Speed On-Chip Oscillator Control Register 5 | FRA5     | 96     |
| 002Bh   | High-Speed On-Chip Oscillator Control Register 6 | FRA6     | 96     |
| 002Ch   |  |          |        |
| 002Dh   |  |          |        |
| 002Eh   |  |          |        |
| 002Fh   | High-Speed On-Chip Oscillator Control Register 3 | FRA3     | 96     |
| 0030h   | Voltage Monitor Circuit Control Register         | CMPA     | 36     |
| 0031h   | Voltage Monitor Circuit Edge Select Register     | VCAC     | 37     |
| 0032h   |  |          |        |
| 0033h   | Voltage Detect Register 1                        | VCA1     | 37     |
| 0034h   | Voltage Detect Register 2                        | VCA2     | 38, 97 |
| 0035h   |  |          |        |
| 0036h   | Voltage Detection 1 Level Select Register        | VD1LS    | 39     |
| 0037h   |  |          |        |
| 0038h   | Voltage Monitor 0 Circuit Control Register       | VW0C     | 40     |
| 0039h   | Voltage Monitor 1 Circuit Control Register       | VW1C     | 41     |
| 003Ah   | Voltage Monitor 2 Circuit Control Register       | VW2C     | 42     |
| 003Bh   |  |          |        |
| 003Ch   |  |          |        |
| 003Dh   |  |          |        |
| 003Eh   |  |          |        |
| 003Fh   |  |          |        |

Note:

- The blank regions are reserved. Do not access locations in these regions.

| Address | Register   | Symbol  | Page |
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| 0040h   |  |         |      |
| 0041h   | Flash Memory Ready Interrupt Control Register            | FMRDYIC | 126  |
| 0042h   |  |         |      |
| 0043h   |  |         |      |
| 0044h   |  |         |      |
| 0045h   |  |         |      |
| 0046h   |  |         |      |
| 0047h   | Timer RC Interrupt Control Register                      | TRCIC   | 126  |
| 0048h   |  |         |      |
| 0049h   |  |         |      |
| 004Ah   | Timer RE Interrupt Control Register                      | TREIC   | 125  |
| 004Bh   | UART2 Transmit Interrupt Control Register                | S2TIC   | 125  |
| 004Ch   | UART2 Receive Interrupt Control Register                 | S2RIC   | 125  |
| 004Dh   | Key Input Interrupt Control Register                     | KUPIC   | 125  |
| 004Eh   | A/D Conversion Interrupt Control Register                | ADIC    | 125  |
| 004Fh   |  |         |      |
| 0050h   |  |         |      |
| 0051h   | UART0 Transmit Interrupt Control Register                | S0TIC   | 125  |
| 0052h   | UART0 Receive Interrupt Control Register                 | S0RIC   | 125  |
| 0053h   |  |         |      |
| 0054h   |  |         |      |
| 0055h   |  |         |      |
| 0056h   | Timer RA Interrupt Control Register                      | TRAIC   | 125  |
| 0057h   |  |         |      |
| 0058h   | Timer RB Interrupt Control Register                      | TRBIC   | 125  |
| 0059h   | INT1 Interrupt Control Register                          | INT1IC  | 127  |
| 005Ah   | INT3 Interrupt Control Register                          | INT3IC  | 127  |
| 005Bh   |  |         |      |
| 005Ch   |  |         |      |
| 005Dh   | INT0 Interrupt Control Register                          | INT0IC  | 127  |
| 005Eh   | UART2 Bus Collision Detection Interrupt Control Register | U2BCNIC | 125  |
| 005Fh   |  |         |      |
| 0060h   |  |         |      |
| 0061h   |  |         |      |
| 0062h   |  |         |      |
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| 0064h   |  |         |      |
| 0065h   |  |         |      |
| 0066h   |  |         |      |
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| 0069h   |  |         |      |
| 006Ah   |  |         |      |
| 006Bh   |  |         |      |
| 006Ch   |  |         |      |
| 006Dh   |  |         |      |
| 006Eh   |  |         |      |
| 006Fh   |  |         |      |
| 0070h   |  |         |      |
| 0071h   |  |         |      |
| 0072h   | Voltage Monitor 1 Interrupt Control Register             | VCMP1IC | 125  |
| 0073h   | Voltage Monitor 2 Interrupt Control Register             | VCMP2IC | 125  |
| 0074h   |  |         |      |
| 0075h   |  |         |      |
| 0076h   |  |         |      |
| 0077h   |  |         |      |
| 0078h   |  |         |      |
| 0079h   |  |         |      |
| 007Ah   |  |         |      |
| 007Bh   |  |         |      |
| 007Ch   |  |         |      |
| 007Dh   |  |         |      |
| 007Eh   |  |         |      |
| 007Fh   |  |         |      |

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| 0084h   |   |        |      |
| 0085h   |   |        |      |
| 0086h   |   |        |      |
| 0087h   |   |        |      |
| 0088h   |   |        |      |
| 0089h   |   |        |      |
| 008Ah   |   |        |      |
| 008Bh   |   |        |      |
| 008Ch   |   |        |      |
| 008Dh   |   |        |      |
| 008Eh   |   |        |      |
| 008Fh   |   |        |      |
| 0090h   |   |        |      |
| 0091h   |   |        |      |
| 0092h   |   |        |      |
| 0093h   |   |        |      |
| 0094h   |   |        |      |
| 0095h   |   |        |      |
| 0096h   |   |        |      |
| 0097h   |   |        |      |
| 0098h   |   |        |      |
| 0099h   |   |        |      |
| 009Ah   |   |        |      |
| 009Bh   |   |        |      |
| 009Ch   |   |        |      |
| 009Dh   |   |        |      |
| 009Eh   |   |        |      |
| 009Fh   |   |        |      |
| 00A0h   | UART0 Transmit/Receive Mode Register          | U0MR   | 265  |
| 00A1h   | UART0 Bit Rate Register                       | U0BRG  | 265  |
| 00A2h   | UART0 Transmit Buffer Register                | U0TB   | 266  |
| 00A3h   |   |        |      |
| 00A4h   | UART0 Transmit/Receive Control Register 0     | U0C0   | 267  |
| 00A5h   | UART0 Transmit/Receive Control Register 1     | U0C1   | 267  |
| 00A6h   | UART0 Receive Buffer Register                 | U0RB   | 268  |
| 00A7h   |   |        |      |
| 00A8h   | UART2 Transmit/Receive Mode Register          | U2MR   | 285  |
| 00A9h   | UART2 Bit Rate Register                       | U2BRG  | 285  |
| 00AAh   | UART2 Transmit Buffer Register                | U2TB   | 286  |
| 00ABh   |   |        |      |
| 00ACh   | UART2 Transmit/Receive Control Register 0     | U2C0   | 287  |
| 00ADh   | UART2 Transmit/Receive Control Register 1     | U2C1   | 288  |
| 00AEh   | UART2 Receive Buffer Register                 | U2RB   | 289  |
| 00AFh   |   |        |      |
| 00B0h   | UART2 Digital Filter Function Select Register | URXDF  | 290  |
| 00B1h   |   |        |      |
| 00B2h   |   |        |      |
| 00B3h   |   |        |      |
| 00B4h   |   |        |      |
| 00B5h   |   |        |      |
| 00B6h   |   |        |      |
| 00B7h   |   |        |      |
| 00B8h   |   |        |      |
| 00B9h   |   |        |      |
| 00BAh   |   |        |      |
| 00BBh   | UART2 Special Mode Register 5                 | U2SMR5 | 290  |
| 00BCh   | UART2 Special Mode Register 4                 | U2SMR4 | 291  |
| 00BDh   | UART2 Special Mode Register 3                 | U2SMR3 | 291  |
| 00BEh   | UART2 Special Mode Register 2                 | U2SMR2 | 292  |
| 00BFh   | UART2 Special Mode Register                   | U2SMR  | 292  |

| Address | Register                   | Symbol  | Page |
|---------|----------------------------|---------|------|
| 00C0h   | A/D Register 0             | AD0     | 331  |
| 00C1h   |                            |         |      |
| 00C2h   | A/D Register 1             | AD1     | 331  |
| 00C3h   |                            |         |      |
| 00C4h   | A/D Register 2             | AD2     | 331  |
| 00C5h   |                            |         |      |
| 00C6h   | A/D Register 3             | AD3     | 331  |
| 00C7h   |                            |         |      |
| 00C8h   | A/D Register 4             | AD4     | 331  |
| 00C9h   |                            |         |      |
| 00CAh   | A/D Register 5             | AD5     | 331  |
| 00CBh   |                            |         |      |
| 00CCh   | A/D Register 6             | AD6     | 331  |
| 00CDh   |                            |         |      |
| 00CEh   | A/D Register 7             | AD7     | 331  |
| 00CFh   |                            |         |      |
| 00D0h   |                            |         |      |
| 00D1h   |                            |         |      |
| 00D2h   |                            |         |      |
| 00D3h   |                            |         |      |
| 00D4h   | A/D Mode Register          | ADMOD   | 332  |
| 00D5h   | A/D Input Select Register  | ADINSEL | 333  |
| 00D6h   | A/D Control Register 0     | ADCON0  | 334  |
| 00D7h   | A/D Control Register 1     | ADCON1  | 335  |
| 00D8h   |                            |         |      |
| 00D9h   |                            |         |      |
| 00DAh   |                            |         |      |
| 00DBh   |                            |         |      |
| 00DCh   |                            |         |      |
| 00DDh   |                            |         |      |
| 00DEh   |                            |         |      |
| 00DFh   |                            |         |      |
| 00E0h   | Port P0 Register           | P0      | 62   |
| 00E1h   | Port P1 Register           | P1      | 62   |
| 00E2h   | Port P0 Direction Register | PD0     | 61   |
| 00E3h   | Port P1 Direction Register | PD1     | 61   |
| 00E4h   |                            |         |      |
| 00E5h   | Port P3 Register           | P3      | 62   |
| 00E6h   |                            |         |      |
| 00E7h   | Port P3 Direction Register | PD3     | 61   |
| 00E8h   | Port P4 Register           | P4      | 62   |
| 00E9h   |                            |         |      |
| 00EAh   | Port P4 Direction Register | PD4     | 61   |
| 00EBh   |                            |         |      |
| 00ECh   |                            |         |      |
| 00EDh   |                            |         |      |
| 00EEh   |                            |         |      |
| 00EFh   |                            |         |      |
| 00F0h   |                            |         |      |
| 00F1h   |                            |         |      |
| 00F2h   |                            |         |      |
| 00F3h   |                            |         |      |
| 00F4h   |                            |         |      |
| 00F5h   |                            |         |      |
| 00F6h   |                            |         |      |
| 00F7h   |                            |         |      |
| 00F8h   |                            |         |      |
| 00F9h   |                            |         |      |
| 00FAh   |                            |         |      |
| 00FBh   |                            |         |      |
| 00FCh   |                            |         |      |
| 00FDh   |                            |         |      |
| 00FEh   |                            |         |      |
| 00FFh   |                            |         |      |

Note:  
1. The blank regions are reserved. Do not access locations in these regions.

| Address | Register                              | Symbol  | Page                         |
|---------|---------------------------------------|---------|------------------------------|
| 0100h   | Timer RA Control Register             | TRACR   | 167                          |
| 0101h   | Timer RA I/O Control Register         | TRAIOC  | 167, 170, 173, 175, 177, 180 |
| 0102h   | Timer RA Mode Register                | TRAMR   | 168                          |
| 0103h   | Timer RA Prescaler Register           | TRAPRE  | 168                          |
| 0104h   | Timer RA Register                     | TRA     | 169                          |
| 0105h   |                                       |         |                              |
| 0106h   |                                       |         |                              |
| 0107h   |                                       |         |                              |
| 0108h   | Timer RB Control Register             | TRBCR   | 184                          |
| 0109h   | Timer RB One-Shot Control Register    | TRBOCR  | 184                          |
| 010Ah   | Timer RB I/O Control Register         | TRBIOC  | 185, 188, 192, 195, 199      |
| 010Bh   | Timer RB Mode Register                | TRBMR   | 185                          |
| 010Ch   | Timer RB Prescaler Register           | TRBPRES | 186                          |
| 010Dh   | Timer RB Secondary Register           | TRBSC   | 186                          |
| 010Eh   | Timer RB Primary Register             | TRBPR   | 187                          |
| 010Fh   |                                       |         |                              |
| 0110h   |                                       |         |                              |
| 0111h   |                                       |         |                              |
| 0112h   |                                       |         |                              |
| 0113h   |                                       |         |                              |
| 0114h   |                                       |         |                              |
| 0115h   |                                       |         |                              |
| 0116h   |                                       |         |                              |
| 0117h   |                                       |         |                              |
| 0118h   | Timer RE Second Data Register         | TRESEC  | 254                          |
| 0119h   | Timer RE Minute Data Register         | TREMIN  | 254                          |
| 011Ah   | Timer RE Hour Data Register           | TREHR   | 255                          |
| 011Bh   | Timer RE Day of Week Data Register    | TREWK   | 255                          |
| 011Ch   | Timer RE Control Register 1           | TRECR1  | 256                          |
| 011Dh   | Timer RE Control Register 2           | TRECR2  | 257                          |
| 011Eh   | Timer RE Count Source Select Register | TRECSR  | 258                          |
| 011Fh   |                                       |         |                              |
| 0120h   | Timer RC Mode Register                | TRCMR   | 206                          |
| 0121h   | Timer RC Control Register 1           | TRCCR1  | 207, 228, 237, 243           |
| 0122h   | Timer RC Interrupt Enable Register    | TRCIER  | 207                          |
| 0123h   | Timer RC Status Register              | TRCSR   | 208                          |
| 0124h   | Timer RC I/O Control Register 0       | TRCIOR0 | 209, 223, 229                |
| 0125h   | Timer RC I/O Control Register 1       | TRCIOR1 | 209, 224, 230                |
| 0126h   | Timer RC Counter                      | TRC     | 210                          |
| 0127h   |                                       |         |                              |
| 0128h   | Timer RC General Register A           | TRCGRA  | 210                          |
| 0129h   |                                       |         |                              |
| 012Ah   | Timer RC General Register B           | TRCGRB  | 210                          |
| 012Bh   |                                       |         |                              |
| 012Ch   | Timer RC General Register C           | TRCGRC  | 210                          |
| 012Dh   |                                       |         |                              |
| 012Eh   | Timer RC General Register D           | TRCGRD  | 210                          |
| 012Fh   |                                       |         |                              |

| Address | Register   | Symbol  | Page               |
|---------|--|---------|--------------------|
| 0130h   | Timer RC Control Register 2                      | TRCCR2  | 211, 231, 238, 244 |
| 0131h   | Timer RC Digital Filter Function Select Register | TRCDF   | 211, 245           |
| 0132h   | Timer RC Output Master Enable Register           | TRCOER  | 212                |
| 0133h   | Timer RC Trigger Control Register                | TRCADCR | 212                |
| 0134h   |  |         |                    |
| 0135h   |  |         |                    |
| 0136h   |  |         |                    |
| 0137h   |  |         |                    |
| 0138h   |  |         |                    |
| 0139h   |  |         |                    |
| 013Ah   |  |         |                    |
| 013Bh   |  |         |                    |
| 013Ch   |  |         |                    |
| 013Dh   |  |         |                    |
| 013Eh   |  |         |                    |
| 013Fh   |  |         |                    |
| 0140h   |  |         |                    |
| 0141h   |  |         |                    |
| 0142h   |  |         |                    |
| 0143h   |  |         |                    |
| 0144h   |  |         |                    |
| 0145h   |  |         |                    |
| 0146h   |  |         |                    |
| 0147h   |  |         |                    |
| 0148h   |  |         |                    |
| 0149h   |  |         |                    |
| 014Ah   |  |         |                    |
| 014Bh   |  |         |                    |
| 014Ch   |  |         |                    |
| 014Dh   |  |         |                    |
| 014Eh   |  |         |                    |
| 014Fh   |  |         |                    |
| 0150h   |  |         |                    |
| 0151h   |  |         |                    |
| 0152h   |  |         |                    |
| 0153h   |  |         |                    |
| 0154h   |  |         |                    |
| 0155h   |  |         |                    |
| 0156h   |  |         |                    |
| 0157h   |  |         |                    |
| 0158h   |  |         |                    |
| 0159h   |  |         |                    |
| 015Ah   |  |         |                    |
| 015Bh   |  |         |                    |
| 015Ch   |  |         |                    |
| 015Dh   |  |         |                    |
| 015Eh   |  |         |                    |
| 015Fh   |  |         |                    |

Note:

1. The blank regions are reserved. Do not access locations in these regions.



| Address | Register                                | Symbol  | Page    |
|---------|---|---------|---------|
| 0160h   |   |         |         |
| 0161h   |   |         |         |
| 0162h   |   |         |         |
| 0163h   |   |         |         |
| 0164h   |   |         |         |
| 0165h   |   |         |         |
| 0166h   |   |         |         |
| 0167h   |   |         |         |
| 0168h   |   |         |         |
| 0169h   |   |         |         |
| 016Ah   |   |         |         |
| 016Bh   |   |         |         |
| 016Ch   |   |         |         |
| 016Dh   |   |         |         |
| 016Eh   |   |         |         |
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| 0177h   |   |         |         |
| 0178h   |   |         |         |
| 0179h   |   |         |         |
| 017Ah   |   |         |         |
| 017Bh   |   |         |         |
| 017Ch   |   |         |         |
| 017Dh   |   |         |         |
| 017Eh   |   |         |         |
| 017Fh   |   |         |         |
| 0180h   | Timer RA Pin Select Register            | TRASR   | 63, 169 |
| 0181h   | Timer RC Pin Select Register            | TRBRCSR | 63, 213 |
| 0182h   | Timer RC Pin Select Register 0          | TRCPSR0 | 64, 214 |
| 0183h   | Timer RC Pin Select Register 1          | TRCPSR1 | 64, 214 |
| 0184h   |   |         |         |
| 0185h   |   |         |         |
| 0186h   |   |         |         |
| 0187h   |   |         |         |
| 0188h   | UART0 Pin Select Register               | U0SR    | 65, 269 |
| 0189h   |   |         |         |
| 018Ah   | UART2 Pin Select Register 0             | U2SR0   | 66, 293 |
| 018Bh   | UART2 Pin Select Register 1             | U2SR1   | 66, 293 |
| 018Ch   |   |         |         |
| 018Dh   |   |         |         |
| 018Eh   | INT Interrupt Input Pin Select Register | INTSR   | 67, 135 |
| 018Fh   | I/O Function Pin Select Register        | PINSR   | 68      |
| 0190h   |   |         |         |
| 0191h   |   |         |         |
| 0192h   |   |         |         |
| 0193h   |   |         |         |
| 0194h   |   |         |         |
| 0195h   |   |         |         |
| 0196h   |   |         |         |
| 0197h   |   |         |         |
| 0198h   |   |         |         |
| 0199h   |   |         |         |
| 019Ah   |   |         |         |
| 019Bh   |   |         |         |
| 019Ch   |   |         |         |
| 019Dh   |   |         |         |
| 019Eh   |   |         |         |
| 019Fh   |   |         |         |

| Address | Register                                | Symbol | Page |
|---------|---|--------|------|
| 01A0h   |   |        |      |
| 01A1h   |   |        |      |
| 01A2h   |   |        |      |
| 01A3h   |   |        |      |
| 01A4h   |   |        |      |
| 01A5h   |   |        |      |
| 01A6h   |   |        |      |
| 01A7h   |   |        |      |
| 01A8h   |   |        |      |
| 01A9h   |   |        |      |
| 01AAh   |   |        |      |
| 01ABh   |   |        |      |
| 01ACh   |   |        |      |
| 01ADh   |   |        |      |
| 01AEh   |   |        |      |
| 01AFh   |   |        |      |
| 01B0h   |   |        |      |
| 01B1h   |   |        |      |
| 01B2h   | Flash Memory Status Register            | FST    | 364  |
| 01B3h   |   |        |      |
| 01B4h   | Flash Memory Control Register 0         | FMR0   | 366  |
| 01B5h   | Flash Memory Control Register 1         | FMR1   | 368  |
| 01B6h   | Flash Memory Control Register 2         | FMR2   | 369  |
| 01B7h   |   |        |      |
| 01B8h   |   |        |      |
| 01B9h   |   |        |      |
| 01BAh   |   |        |      |
| 01BBh   |   |        |      |
| 01BCh   |   |        |      |
| 01BDh   |   |        |      |
| 01BEh   |   |        |      |
| 01C0h   | Address Match Interrupt Register 0      | RMAD0  | 141  |
| 01C1h   |   |        |      |
| 01C2h   |   |        |      |
| 01C3h   | Address Match Interrupt Enable Register | AIER   | 141  |
| 01C4h   | Address Match Interrupt Register 1      | RMAD1  | 141  |
| 01C5h   |   |        |      |
| 01C6h   |   |        |      |
| 01C7h   |   |        |      |
| 01C8h   |   |        |      |
| 01C9h   |   |        |      |
| 01CAh   |   |        |      |
| 01CBh   |   |        |      |
| 01CCh   |   |        |      |
| 01CDh   |   |        |      |
| 01CEh   |   |        |      |
| 01CFh   |   |        |      |
| 01D0h   |   |        |      |
| 01D1h   |   |        |      |
| 01D2h   |   |        |      |
| 01D3h   |   |        |      |
| 01D4h   |   |        |      |
| 01D5h   |   |        |      |
| 01D6h   |   |        |      |
| 01D7h   |   |        |      |
| 01D8h   |   |        |      |
| 01D9h   |   |        |      |
| 01DAh   |   |        |      |
| 01DBh   |   |        |      |
| 01DCh   |   |        |      |
| 01DDh   |   |        |      |
| 01DEh   |   |        |      |
| 01DFh   |   |        |      |

Note:  
1. The blank regions are reserved. Do not access locations in these regions.

| Address | Register                                | Symbol | Page                  |
|---------|---|--------|-----------------------|
| 01E0h   | Pull-Up Control Register 0              | PUR0   | 69                    |
| 01E1h   | Pull-Up Control Register 1              | PUR1   | 69                    |
| 01E2h   |   |        |                       |
| 01E3h   |   |        |                       |
| 01E4h   |   |        |                       |
| 01E5h   |   |        |                       |
| 01E6h   |   |        |                       |
| 01E7h   |   |        |                       |
| 01E8h   |   |        |                       |
| 01E9h   |   |        |                       |
| 01EAh   |   |        |                       |
| 01EBh   |   |        |                       |
| 01ECh   |   |        |                       |
| 01EDh   |   |        |                       |
| 01EEh   |   |        |                       |
| 01EFh   |   |        |                       |
| 01F0h   | Port P1 Drive Capacity Control Register | P1DRR  | 70                    |
| 01F1h   |   |        |                       |
| 01F2h   | Drive Capacity Control Register 0       | DRR0   | 71                    |
| 01F3h   | Drive Capacity Control Register 1       | DRR1   | 72                    |
| 01F4h   |   |        |                       |
| 01F5h   | Input Threshold Control Register 0      | VLT0   | 73                    |
| 01F6h   | Input Threshold Control Register 1      | VLT1   | 73                    |
| 01F7h   |   |        |                       |
| 01F8h   | Comparator B Control Register 0         | INTCMP | 354                   |
| 01F9h   |   |        |                       |
| 01FAh   | External Input Enable Register 0        | INTEN  | 136, 354              |
| 01FBh   |   |        |                       |
| 01FCh   | INT Input Filter Select Register 0      | INTF   | 136, 355              |
| 01FDh   |   |        |                       |
| 01FEh   | Key Input Enable Register 0             | KIEN   | 139                   |
| 01FFh   |   |        |                       |
| FFDBh   | Option Function Select Register 2       | OFS2   | 25, 153, 160          |
| :       |   |        |                       |
| FFFFh   | Option Function Select Register         | OFS    | 24, 43, 152, 159, 362 |

Note:

1. The blank regions are reserved. Do not access locations in these regions.

## **1. Overview**

### **1.1 Features**

The R8C/3GD Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

#### **1.1.1 Applications**

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

## 1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3GD Group.

**Table 1.1 Specifications for R8C/3GD Group (1)**

| Item                           | Function                  | Specification   |
|--------------------------------|---------------------------|---|
| CPU                            | Central processing unit   | <p>R8C CPU core</p> <ul style="list-style-type: none"> <li>Number of fundamental instructions: 89</li> <li>Minimum instruction execution time:               <ul style="list-style-type: none"> <li>50 ns (<math>f(XIN) = 20</math> MHz, <math>VCC = 2.7</math> to 5.5 V)</li> <li>200 ns (<math>f(XIN) = 5</math> MHz, <math>VCC = 1.8</math> to 5.5 V)</li> </ul> </li> <li>Multiplier: 16 bits <math>\times</math> 16 bits <math>\rightarrow</math> 32 bits</li> <li>Multiply-accumulate instruction: 16 bits <math>\times</math> 16 bits + 32 bits <math>\rightarrow</math> 32 bits</li> <li>Operation mode: Single-chip mode (address space: 1 Mbyte)</li> </ul>                       |
| Memory                         | ROM, RAM                  | Refer to <b>Table 1.3 Product List for R8C/3GD Group</b> .  |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> <li>Power-on reset</li> <li>Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)</li> </ul>   |
| I/O Ports                      | Programmable I/O ports    | <ul style="list-style-type: none"> <li>Input-only: 1 pin</li> <li>CMOS I/O ports: 19, selectable pull-up resistor</li> <li>High current drive ports: 19</li> </ul>  |
| Clock                          | Clock generation circuits | <p>4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator,</p> <ul style="list-style-type: none"> <li>Oscillation stop detection: XIN clock oscillation stop detection function</li> <li>Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16</li> <li>Low power consumption modes:               <ul style="list-style-type: none"> <li>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode</li> </ul> </li> </ul> <p>Real-time clock (timer RE)</p> |
| Interrupts                     |                           | <ul style="list-style-type: none"> <li>Number of interrupt vectors: 69</li> <li>External Interrupt: 7 (<math>\overline{INT} \times 3</math>, Key input <math>\times 4</math>)</li> <li>Priority levels: 7 levels</li> </ul>   |
| Watchdog Timer                 |                           | <ul style="list-style-type: none"> <li>14 bits <math>\times</math> 1 (with prescaler)</li> <li>Reset start selectable</li> <li>Low-speed on-chip oscillator for watchdog timer selectable</li> </ul>  |
| Timer                          | Timer RA                  | <p>8 bits <math>\times</math> 1 (with 8-bit prescaler)</p> <p>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode</p>  |
|                                | Timer RB                  | <p>8 bits <math>\times</math> 1 (with 8-bit prescaler)</p> <p>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode</p>  |
|                                | Timer RC                  | <p>16 bits <math>\times</math> 1 (with 4 capture/compare registers)</p> <p>Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)</p>   |
|                                | Timer RE                  | <p>8 bits <math>\times</math> 1</p> <p>Real-time clock mode (count seconds, minutes, hours, days of week)</p>   |
| Serial Interface               | UART0                     | Clock synchronous serial I/O/UART   |
|                                | UART2                     | Clock synchronous serial I/O/UART, I <sup>2</sup> C mode (I <sup>2</sup> C-bus), multiprocessor communication function  |
| A/D Converter                  |                           | 10-bit resolution $\times$ 8 channels, includes sample and hold function, with sweep mode   |
| Comparator B                   |                           | 2 circuits  |

**Table 1.2 Specifications for R8C/3GD Group (2)**

| Item                               | Function | Specification   |
|------------------------------------|----------|---|
| Flash Memory                       |          | <ul style="list-style-type: none"> <li>• Programming and erasure voltage: VCC = 2.7 to 5.5 V</li> <li>• Programming and erasure endurance: 1,000 times (program ROM)</li> <li>• Program security: ROM code protect, ID code check</li> <li>• Debug functions: On-chip debug, on-board flash rewrite function</li> </ul> |
| Operating Frequency/Supply Voltage |          | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)   |
| Current consumption                |          | Typ. 6.5mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 3.5mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 3.5μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz))<br>Typ. 2.0μA (VCC = 3.0 V, stop mode)   |
| Operating Ambient Temperature      |          | -20 to 85°C (N version)<br>-40 to 85°C (D version) (1)  |
| Package                            |          | 24-pin LSSOP<br>Package code: PLSP0024JB-A (previous code: 24P2F-A)   |

Note:

1. Specify the D version if D version functions are to be used.

## 1.2 Product List

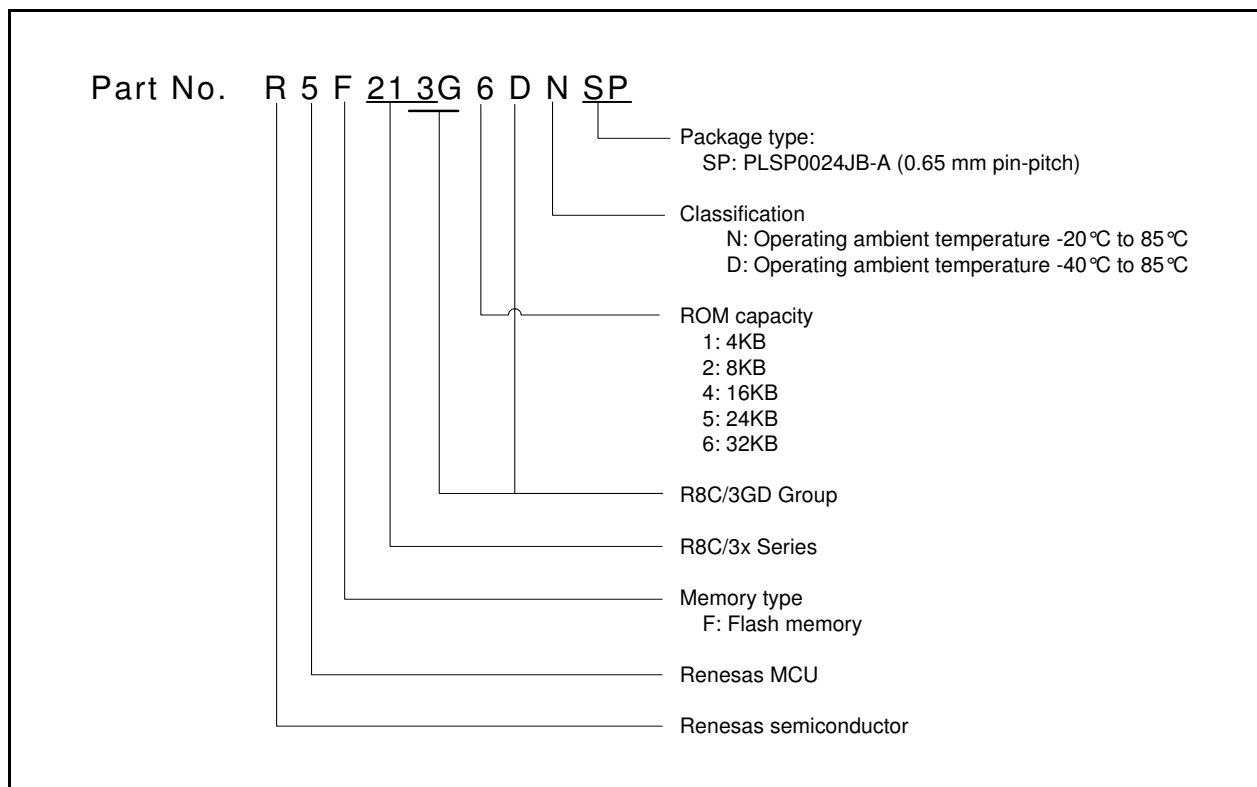
Table 1.3 lists Product List for R8C/3GD Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3GD Group.

**Table 1.3 Product List for R8C/3GD Group**

**Current of Feb. 2010**

| Part No.         | ROM Capacity | RAM Capacity | Package Type | Remarks   |
|------------------|--------------|--------------|--------------|-----------|
| R5F213G1DNSP     | 4 Kbytes     | 1 Kbyte      | PLSP0024JB-A | N version |
| R5F213G2DNSP     | 8 Kbytes     | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G4DNSP     | 16 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G5DNSP     | 24 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G6DNSP     | 32 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G1DDSP (D) | 4 Kbytes     | 1 Kbyte      | PLSP0024JB-A | D version |
| R5F213G2DDSP (D) | 8 Kbytes     | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G4DDSP (D) | 16 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G5DDSP (D) | 24 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |
| R5F213G6DDSP (D) | 32 Kbytes    | 1 Kbyte      | PLSP0024JB-A |           |

(D): Under development



**Figure 1.1 Part Number, Memory Size, and Package of R8C/3GD Group**

### 1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

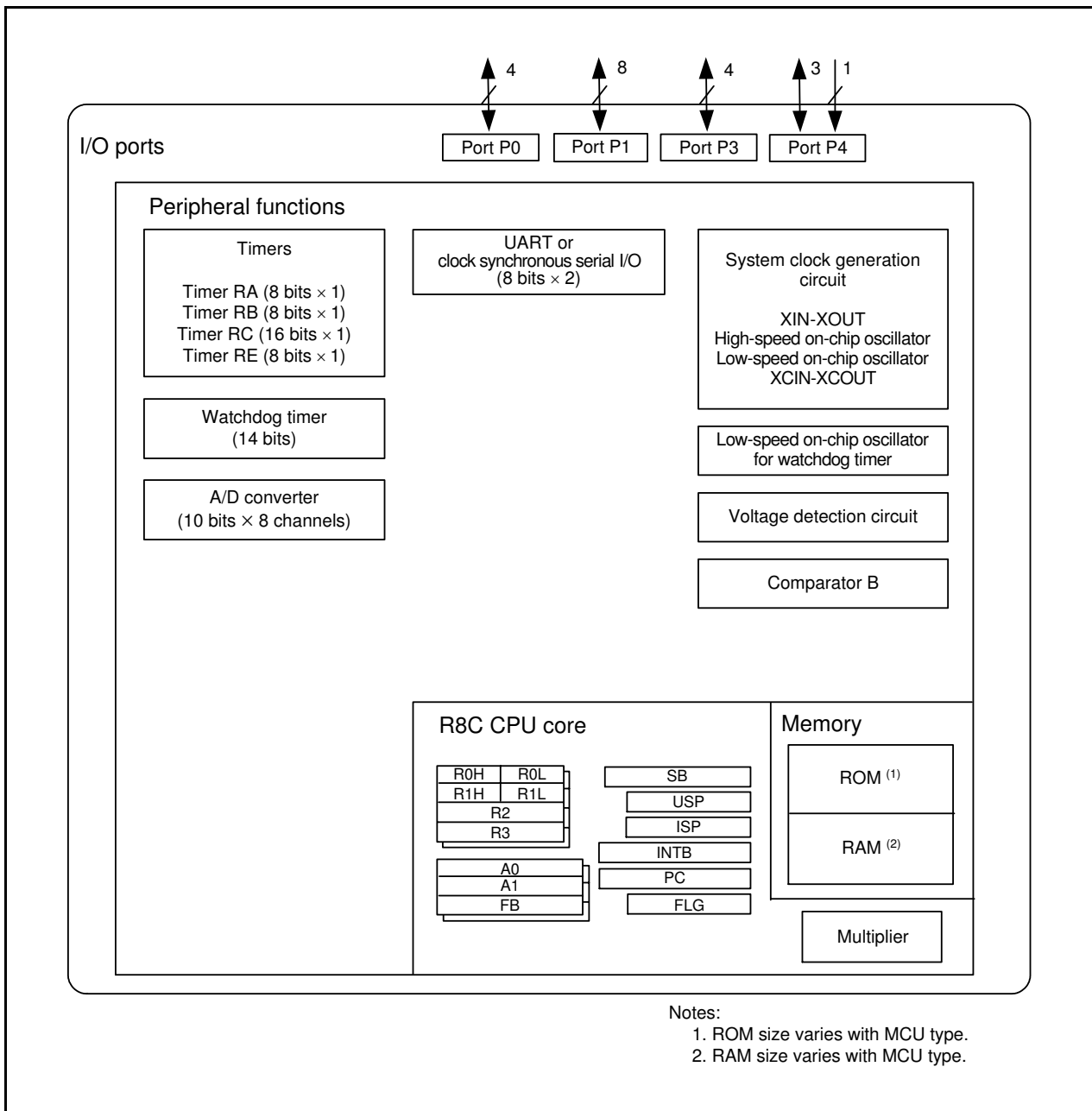
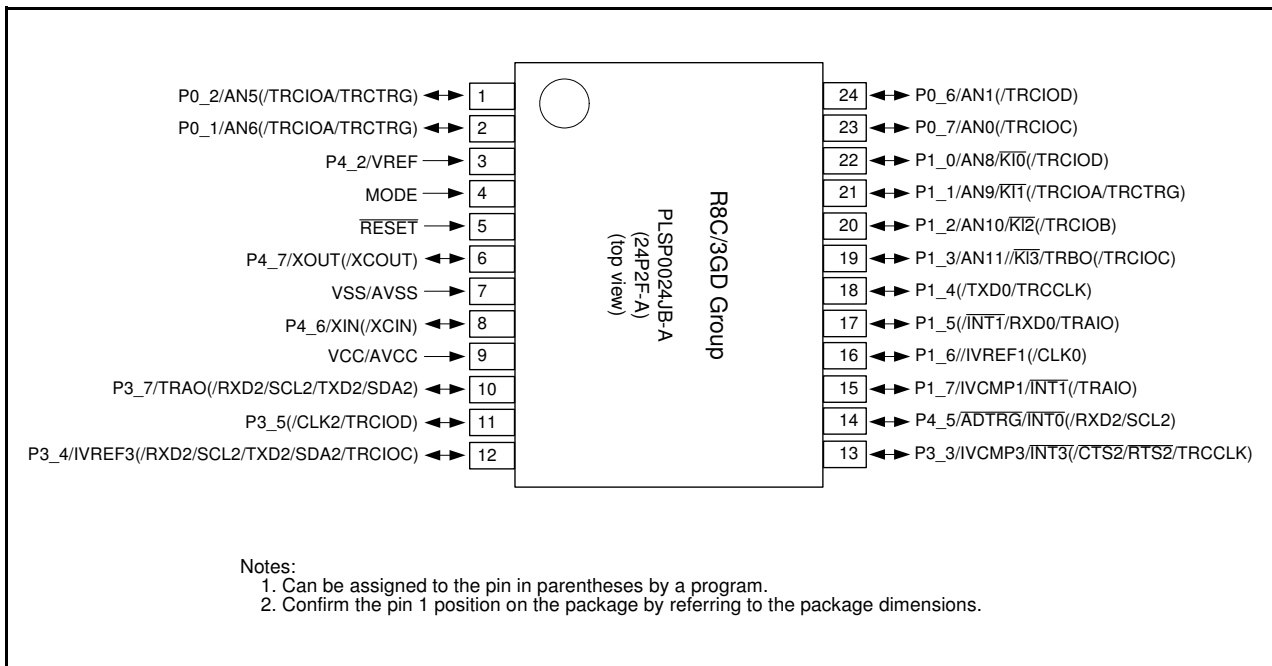


Figure 1.2 Block Diagram

## 1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.



**Figure 1.3 Pin Assignment (Top View)**



**Table 1.4 Pin Name Information by Pin Number**

| Pin Number | Control Pin               | Port | I/O Pin Functions for Peripheral Modules |                                |   |                             |
|------------|---------------------------|------|--|--------------------------------|---|-----------------------------|
|            |                           |      | Interrupt                                | Timer                          | Serial Interface  | A/D Converter, Comparator B |
| 1          |                           | P0_2 |  | (TRCIOA/TRCTR $\overline{G}$ ) |   | AN5                         |
| 2          |                           | P0_1 |  | (TRCIOA/TRCTR $\overline{G}$ ) |   | AN6                         |
| 3          |                           | P4_2 |  |                                |   | VREF                        |
| 4          | MODE                      |      |  |                                |   |                             |
| 5          | $\overline{\text{RESET}}$ |      |  |                                |   |                             |
| 6          | XOUT(/XCOUT)              | P4_7 |  |                                |   |                             |
| 7          | VSS/AVSS                  |      |  |                                |   |                             |
| 8          | XIN(/XCIN)                | P4_6 |  |                                |   |                             |
| 9          | VCC/AVCC                  |      |  |                                |   |                             |
| 10         |                           | P3_7 |  | TRAO                           | (RXD2/SCL2/<br>TXD2/SDA2)                               |                             |
| 11         |                           | P3_5 |  | (TRCIOD)                       | (CLK2)  |                             |
| 12         |                           | P3_4 |  | (TRCIOC)                       | (RXD2/SCL2/<br>TXD2/SDA2)                               | IVREF3                      |
| 13         |                           | P3_3 | $\overline{\text{INT3}}$                 | (TRCCLK)                       | ( $\overline{\text{CTS2}}$ / $\overline{\text{RTS2}}$ ) | IVCMP3                      |
| 14         |                           | P4_5 | $\overline{\text{INT0}}$                 |                                | (RXD2/SCL2)   | $\overline{\text{ADTRG}}$   |
| 15         |                           | P1_7 | $\overline{\text{INT1}}$                 | (TRAIO)                        |   | IVCMP1                      |
| 16         |                           | P1_6 |  |                                | (CLK0)  | IVREF1                      |
| 17         |                           | P1_5 | ( $\overline{\text{INT1}}$ )             | (TRAIO)                        | (RXD0)  |                             |
| 18         |                           | P1_4 |  | (TRCCLK)                       | (TXD0)  |                             |
| 19         |                           | P1_3 | $\overline{\text{K13}}$                  | TRBO(/TRCIOC)                  |   | AN11                        |
| 20         |                           | P1_2 | $\overline{\text{K12}}$                  | (TRCIOB)                       |   | AN10                        |
| 21         |                           | P1_1 | $\overline{\text{K11}}$                  | (TRCIOA/TRCTR $\overline{G}$ ) |   | AN9                         |
| 22         |                           | P1_0 | $\overline{\text{K10}}$                  | (TRCIOD)                       |   | AN8                         |
| 23         |                           | P0_7 |  | (TRCIOC)                       |   | AN0                         |
| 24         |                           | P0_6 |  | (TRCIOD)                       |   | AN1                         |

Note:

1. Can be assigned to the pin in parentheses by a program.

## 1.5 Pin Functions

Table 1.5 lists Pin Functions.

**Table 1.5 Pin Functions**

| Item                                    | Pin Name   | I/O Type                           | Description  |
|---|--|------------------------------------|--|
| Power supply input                      | VCC, VSS   | –                                  | Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.   |
| Analog power supply input               | AVCC, AVSS   | –                                  | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS.  |
| Reset input                             | $\overline{\text{RESET}}$  | I                                  | Input “L” on this pin resets the MCU.  |
| MODE                                    | MODE   | I                                  | Connect this pin to VCC via a resistor.  |
| XIN clock input                         | XIN  | I                                  | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins <sup>(1)</sup> . To use an external clock, input it to the XOUT pin and leave the XIN pin open.                                |
| XIN clock output                        | XOUT   | I/O                                |  |
| XCIN clock input                        | XCIN   | I                                  | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins <sup>(1)</sup> . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.  |
| XCIN clock output                       | XCOU   | O                                  |  |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ , $\overline{\text{INT1}}$ , $\overline{\text{INT3}}$ | I                                  | $\overline{\text{INT}}$ interrupt input pins.<br>$\overline{\text{INT0}}$ is timer RB, and RC input pin.   |
| Key input interrupt                     | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$                             | I                                  | Key input interrupt input pins   |
| Timer RA                                | TRAIO  | I/O                                | Timer RA I/O pin   |
|   | TRAO   | O                                  | Timer RA output pin  |
| Timer RB                                | TRBO   | O                                  | Timer RB output pin  |
| Timer RC                                | TRCCLK   | I                                  | External clock input pin   |
|   | TRCTR $\overline{\text{G}}$  | I                                  | External trigger input pin   |
|   | TRCIOA, TRCIOB, TRCIO $\overline{\text{C}}$ , TRCIOD                           | I/O                                | Timer RC I/O pins  |
| Serial interface                        | CLK0, CLK2   | I/O                                | Transfer clock I/O pins  |
|   | RXD0, RXD2   | I                                  | Serial data input pins   |
|   | TXD0, TXD2   | O                                  | Serial data output pins  |
|   | $\overline{\text{CTS2}}$   | I                                  | Transmission control input pin   |
|   | RTS2   | O                                  | Reception control output pin   |
|   | SCL2   | I/O                                | I <sup>2</sup> C mode clock I/O pin  |
| SDA2                                    | I/O  | I <sup>2</sup> C mode data I/O pin |  |
| Reference voltage input                 | VREF   | I                                  | Reference voltage input pin to A/D converter   |
| A/D converter                           | AN0, AN1, AN5, AN6, AN8 to AN11  | I                                  | Analog input pins to A/D converter   |
|   | $\overline{\text{ADTRG}}$  | I                                  | A/D external trigger input pin   |
| Comparator B                            | IVCMP1, IVCMP3   | I                                  | Comparator B analog voltage input pins   |
|   | IVREF1, IVREF3   | I                                  | Comparator B reference voltage input pins  |
| I/O port                                | P0_1, P0_2, P0_6, P0_7, P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5 to P4_7         | I/O                                | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>All ports can be used as LED drive ports. |
| Input port                              | P4_2   | I                                  | Input-only port  |

I: Input      O: Output      I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

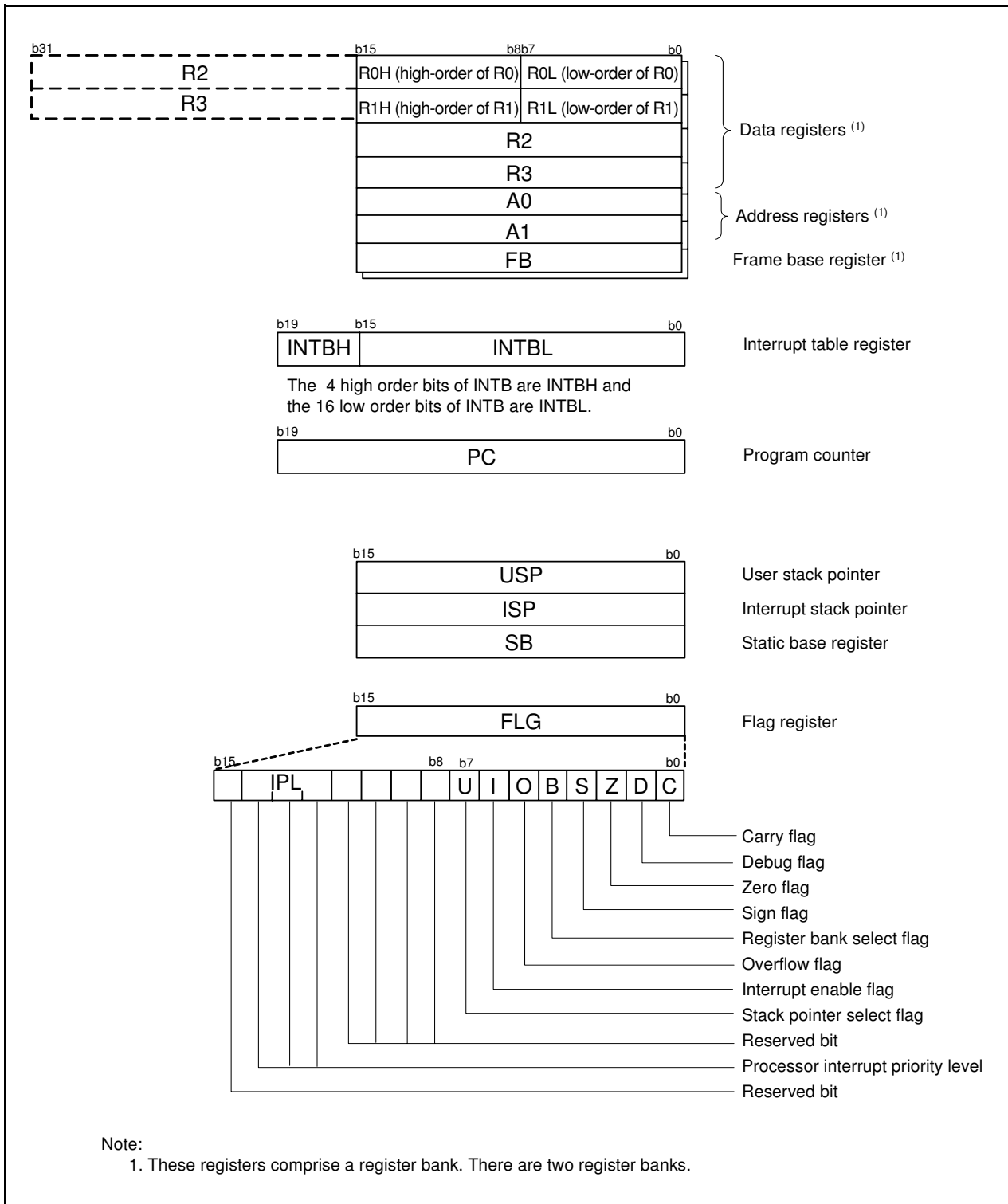


Figure 2.1 CPU Registers

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

### 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

## 3. Memory

### 3.1 R8C/3GD Group

Figure 3.1 is a Memory Map of R8C/3GD Group. The R8C/3GD Group has a 1-Mbyte address space from addresses 00000h to FFFFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh. The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

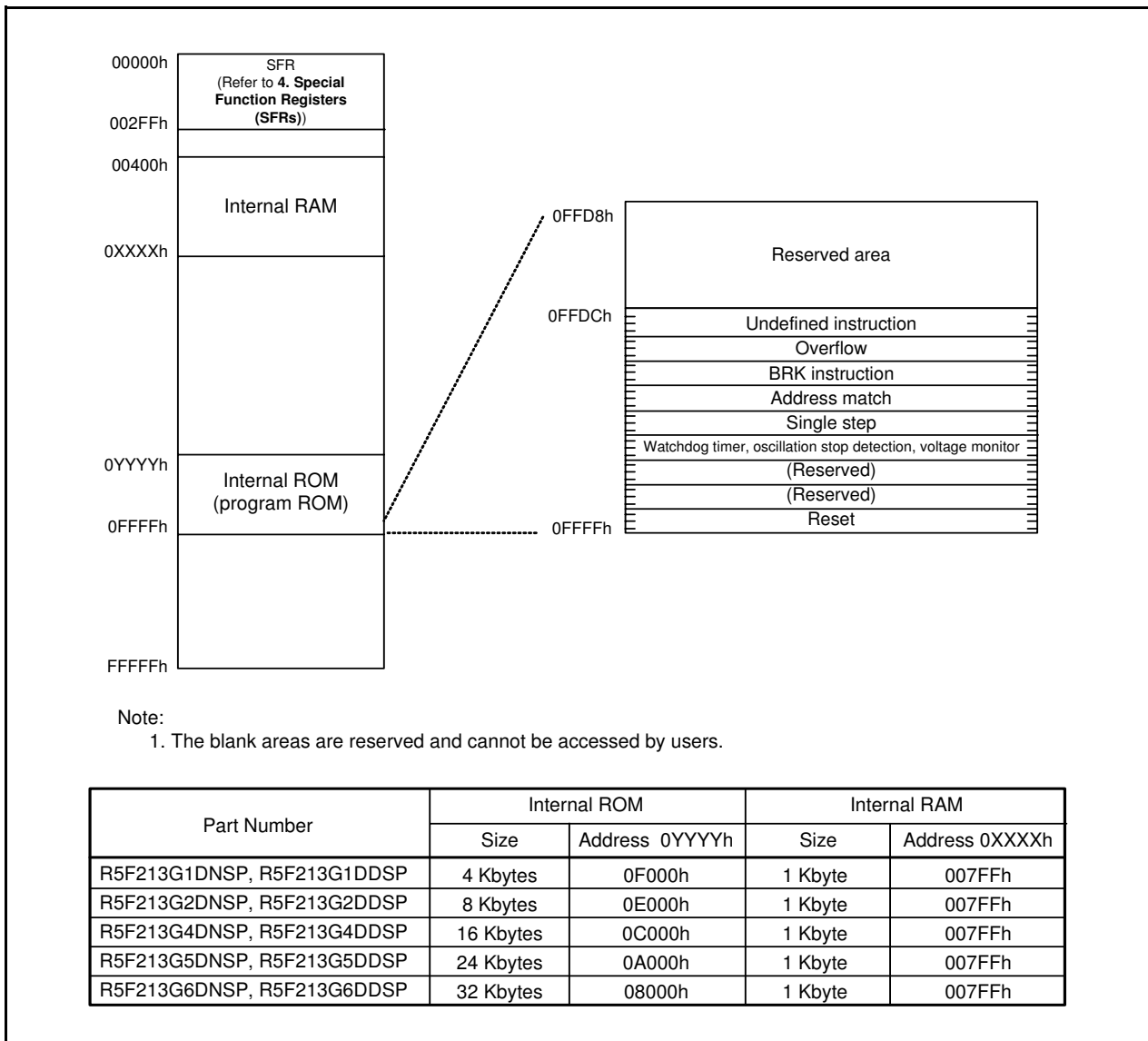


Figure 3.1 Memory Map of R8C/3GD Group

## 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers and Table 4.8 lists the ID Code Areas and Option Function Select Area.

**Table 4.1 SFR Information (1) (1)**

| Address | Register   | Symbol   | After Reset                    |
|---------|--|----------|--------------------------------|
| 0000h   |  |          |                                |
| 0001h   |  |          |                                |
| 0002h   |  |          |                                |
| 0003h   |  |          |                                |
| 0004h   | Processor Mode Register 0                        | PM0      | 00h                            |
| 0005h   | Processor Mode Register 1                        | PM1      | 00h                            |
| 0006h   | System Clock Control Register 0                  | CM0      | 00101000b                      |
| 0007h   | System Clock Control Register 1                  | CM1      | 00100000b                      |
| 0008h   | Module Standby Control Register                  | MSTCR    | 00h                            |
| 0009h   | System Clock Control Register 3                  | CM3      | 00h                            |
| 000Ah   | Protect Register                                 | PRCR     | 00h                            |
| 000Bh   | Reset Source Determination Register              | RSTFR    | 0XXXXXXb (2)                   |
| 000Ch   | Oscillation Stop Detection Register              | OCD      | 00000100b                      |
| 000Dh   | Watchdog Timer Reset Register                    | WDTR     | XXh                            |
| 000Eh   | Watchdog Timer Start Register                    | WDTS     | XXh                            |
| 000Fh   | Watchdog Timer Control Register                  | WDTC     | 00111111b                      |
| 0010h   |  |          |                                |
| 0011h   |  |          |                                |
| 0012h   |  |          |                                |
| 0013h   |  |          |                                |
| 0014h   |  |          |                                |
| 0015h   | High-Speed On-Chip Oscillator Control Register 7 | FRA7     | When shipping                  |
| 0016h   |  |          |                                |
| 0017h   |  |          |                                |
| 0018h   |  |          |                                |
| 0019h   |  |          |                                |
| 001Ah   |  |          |                                |
| 001Bh   |  |          |                                |
| 001Ch   | Count Source Protection Mode Register            | CSPR     | 00h<br>10000000b (3)           |
| 001Dh   |  |          |                                |
| 001Eh   |  |          |                                |
| 001Fh   |  |          |                                |
| 0020h   |  |          |                                |
| 0021h   |  |          |                                |
| 0022h   |  |          |                                |
| 0023h   | High-Speed On-Chip Oscillator Control Register 0 | FRA0     | 00h                            |
| 0024h   | High-Speed On-Chip Oscillator Control Register 1 | FRA1     | When shipping                  |
| 0025h   | High-Speed On-Chip Oscillator Control Register 2 | FRA2     | 00h                            |
| 0026h   | On-Chip Reference Voltage Control Register       | OCVREFCR | 00h                            |
| 0027h   |  |          |                                |
| 0028h   | Clock Prescaler Reset Flag                       | CPSRF    | 00h                            |
| 0029h   | High-Speed On-Chip Oscillator Control Register 4 | FRA4     | When Shipping                  |
| 002Ah   | High-Speed On-Chip Oscillator Control Register 5 | FRA5     | When Shipping                  |
| 002Bh   | High-Speed On-Chip Oscillator Control Register 6 | FRA6     | When Shipping                  |
| 002Ch   |  |          |                                |
| 002Dh   |  |          |                                |
| 002Eh   |  |          |                                |
| 002Fh   | High-Speed On-Chip Oscillator Control Register 3 | FRA3     | When shipping                  |
| 0030h   | Voltage Monitor Circuit Control Register         | CMPA     | 00h                            |
| 0031h   | Voltage Monitor Circuit Edge Select Register     | VCAC     | 00h                            |
| 0032h   |  |          |                                |
| 0033h   | Voltage Detect Register 1                        | VCA1     | 00001000b                      |
| 0034h   | Voltage Detect Register 2                        | VCA2     | 00h (4)<br>00100000b (5)       |
| 0035h   |  |          |                                |
| 0036h   | Voltage Detection 1 Level Select Register        | VD1LS    | 00000111b                      |
| 0037h   |  |          |                                |
| 0038h   | Voltage Monitor 0 Circuit Control Register       | VW0C     | 1100X010b (4)<br>1100X011b (5) |
| 0039h   | Voltage Monitor 1 Circuit Control Register       | VW1C     | 10001010b                      |

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

**Table 4.2 SFR Information (2) (1)**

| Address | Register   | Symbol  | After Reset |
|---------|--|---------|-------------|
| 003Ah   | Voltage Monitor 2 Circuit Control Register               | VW2C    | 1000010b    |
| 003Bh   |  |         |             |
| 003Ch   |  |         |             |
| 003Dh   |  |         |             |
| 003Eh   |  |         |             |
| 003Fh   |  |         |             |
| 0040h   |  |         |             |
| 0041h   | Flash Memory Ready Interrupt Control Register            | FMRDYIC | XXXXX000b   |
| 0042h   |  |         |             |
| 0043h   |  |         |             |
| 0044h   |  |         |             |
| 0045h   |  |         |             |
| 0046h   |  |         |             |
| 0047h   | Timer RC Interrupt Control Register                      | TRCIC   | XXXXX000b   |
| 0048h   |  |         |             |
| 0049h   |  |         |             |
| 004Ah   | Timer RE Interrupt Control Register                      | TREIC   | XXXXX000b   |
| 004Bh   | UART2 Transmit Interrupt Control Register                | S2TIC   | XXXXX000b   |
| 004Ch   | UART2 Receive Interrupt Control Register                 | S2RIC   | XXXXX000b   |
| 004Dh   | Key Input Interrupt Control Register                     | KUPIC   | XXXXX000b   |
| 004Eh   | A/D Conversion Interrupt Control Register                | ADIC    | XXXXX000b   |
| 004Fh   |  |         |             |
| 0050h   |  |         |             |
| 0051h   | UART0 Transmit Interrupt Control Register                | S0TIC   | XXXXX000b   |
| 0052h   | UART0 Receive Interrupt Control Register                 | S0RIC   | XXXXX000b   |
| 0053h   |  |         |             |
| 0054h   |  |         |             |
| 0055h   |  |         |             |
| 0056h   | Timer RA Interrupt Control Register                      | TRAIC   | XXXXX000b   |
| 0057h   |  |         |             |
| 0058h   | Timer RB Interrupt Control Register                      | TRBIC   | XXXXX000b   |
| 0059h   | INT1 Interrupt Control Register                          | INT1IC  | XX00X000b   |
| 005Ah   | INT3 Interrupt Control Register                          | INT3IC  | XX00X000b   |
| 005Bh   |  |         |             |
| 005Ch   |  |         |             |
| 005Dh   | INT0 Interrupt Control Register                          | INT0IC  | XX00X000b   |
| 005Eh   | UART2 Bus Collision Detection Interrupt Control Register | U2BCNIC | XXXXX000b   |
| 005Fh   |  |         |             |
| 0060h   |  |         |             |
| 0061h   |  |         |             |
| 0062h   |  |         |             |
| 0063h   |  |         |             |
| 0064h   |  |         |             |
| 0065h   |  |         |             |
| 0066h   |  |         |             |
| 0067h   |  |         |             |
| 0068h   |  |         |             |
| 0069h   |  |         |             |
| 006Ah   |  |         |             |
| 006Bh   |  |         |             |
| 006Ch   |  |         |             |
| 006Dh   |  |         |             |
| 006Eh   |  |         |             |
| 006Fh   |  |         |             |
| 0070h   |  |         |             |
| 0071h   |  |         |             |
| 0072h   | Voltage Monitor 1 Interrupt Control Register             | VCMP1IC | XXXXX000b   |
| 0073h   | Voltage Monitor 2 Interrupt Control Register             | VCMP2IC | XXXXX000b   |
| 0074h   |  |         |             |
| 0075h   |  |         |             |
| 0076h   |  |         |             |
| 0077h   |  |         |             |
| 0078h   |  |         |             |
| 0079h   |  |         |             |
| 007Ah   |  |         |             |
| 007Bh   |  |         |             |
| 007Ch   |  |         |             |
| 007Dh   |  |         |             |
| 007Eh   |  |         |             |
| 007Fh   |  |         |             |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.



**Table 4.3 SFR Information (3) (1)**

| Address | Register                                      | Symbol | After Reset |
|---------|---|--------|-------------|
| 0080h   |   |        |             |
| 0081h   |   |        |             |
| 0082h   |   |        |             |
| 0083h   |   |        |             |
| 0084h   |   |        |             |
| 0085h   |   |        |             |
| 0086h   |   |        |             |
| 0087h   |   |        |             |
| 0088h   |   |        |             |
| 0089h   |   |        |             |
| 008Ah   |   |        |             |
| 008Bh   |   |        |             |
| 008Ch   |   |        |             |
| 008Dh   |   |        |             |
| 008Eh   |   |        |             |
| 008Fh   |   |        |             |
| 0090h   |   |        |             |
| 0091h   |   |        |             |
| 0092h   |   |        |             |
| 0093h   |   |        |             |
| 0094h   |   |        |             |
| 0095h   |   |        |             |
| 0096h   |   |        |             |
| 0097h   |   |        |             |
| 0098h   |   |        |             |
| 0099h   |   |        |             |
| 009Ah   |   |        |             |
| 009Bh   |   |        |             |
| 009Ch   |   |        |             |
| 009Dh   |   |        |             |
| 009Eh   |   |        |             |
| 009Fh   |   |        |             |
| 00A0h   | UART0 Transmit / Receive Mode Register        | U0MR   | 00h         |
| 00A1h   | UART0 Bit Rate Register                       | U0BRG  | XXh         |
| 00A2h   | UART0 Transmit Buffer Register                | U0TB   | XXh         |
| 00A3h   |   |        | XXh         |
| 00A4h   | UART0 Transmit / Receive Control Register 0   | U0C0   | 00001000b   |
| 00A5h   | UART0 Transmit / Receive Control Register 1   | U0C1   | 00000010b   |
| 00A6h   | UART0 Receive Buffer Register                 | U0RB   | XXh         |
| 00A7h   |   |        | XXh         |
| 00A8h   | UART2 Transmit / Receive Mode Register        | U2MR   | 00h         |
| 00A9h   | UART2 Bit Rate Register                       | U2BRG  | XXh         |
| 00AAh   | UART2 Transmit Buffer Register                | U2TB   | XXh         |
| 00ABh   |   |        | XXh         |
| 00ACh   | UART2 Transmit / Receive Control Register 0   | U2C0   | 00001000b   |
| 00ADh   | UART2 Transmit / Receive Control Register 1   | U2C1   | 00000010b   |
| 00AEh   | UART2 Receive Buffer Register                 | U2RB   | XXh         |
| 00AFh   |   |        | XXh         |
| 00B0h   | UART2 Digital Filter Function Select Register | URXDF  | 00h         |
| 00B1h   |   |        |             |
| 00B2h   |   |        |             |
| 00B3h   |   |        |             |
| 00B4h   |   |        |             |
| 00B5h   |   |        |             |
| 00B6h   |   |        |             |
| 00B7h   |   |        |             |
| 00B8h   |   |        |             |
| 00B9h   |   |        |             |
| 00BAh   |   |        |             |
| 00BBh   | UART2 Special Mode Register 5                 | U2SMR5 | 00h         |
| 00BCh   | UART2 Special Mode Register 4                 | U2SMR4 | 00h         |
| 00BDh   | UART2 Special Mode Register 3                 | U2SMR3 | 000X0X0Xb   |
| 00BEh   | UART2 Special Mode Register 2                 | U2SMR2 | X0000000b   |
| 00BFh   | UART2 Special Mode Register                   | U2SMR  | X0000000b   |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.4 SFR Information (4) (1)**

| Address | Register                   | Symbol  | After Reset |
|---------|----------------------------|---------|-------------|
| 00C0h   | A/D Register 0             | AD0     | XXh         |
| 00C1h   |                            |         | 00000XXb    |
| 00C2h   | A/D Register 1             | AD1     | XXh         |
| 00C3h   |                            |         | 00000XXb    |
| 00C4h   | A/D Register 2             | AD2     | XXh         |
| 00C5h   |                            |         | 00000XXb    |
| 00C6h   | A/D Register 3             | AD3     | XXh         |
| 00C7h   |                            |         | 00000XXb    |
| 00C8h   | A/D Register 4             | AD4     | XXh         |
| 00C9h   |                            |         | 00000XXb    |
| 00CAh   | A/D Register 5             | AD5     | XXh         |
| 00CBh   |                            |         | 00000XXb    |
| 00CCh   | A/D Register 6             | AD6     | XXh         |
| 00CDh   |                            |         | 00000XXb    |
| 00CEh   | A/D Register 7             | AD7     | XXh         |
| 00CFh   |                            |         | 00000XXb    |
| 00D0h   |                            |         |             |
| 00D1h   |                            |         |             |
| 00D2h   |                            |         |             |
| 00D3h   |                            |         |             |
| 00D4h   | A/D Mode Register          | ADMOD   | 00h         |
| 00D5h   | A/D Input Select Register  | ADINSEL | 1100000b    |
| 00D6h   | A/D Control Register 0     | ADCON0  | 00h         |
| 00D7h   | A/D Control Register 1     | ADCON1  | 00h         |
| 00D8h   |                            |         |             |
| 00D9h   |                            |         |             |
| 00DAh   |                            |         |             |
| 00DBh   |                            |         |             |
| 00DCh   |                            |         |             |
| 00DDh   |                            |         |             |
| 00DEh   |                            |         |             |
| 00DFh   |                            |         |             |
| 00E0h   | Port P0 Register           | P0      | XXh         |
| 00E1h   | Port P1 Register           | P1      | XXh         |
| 00E2h   | Port P0 Direction Register | PD0     | 00h         |
| 00E3h   | Port P1 Direction Register | PD1     | 00h         |
| 00E4h   |                            |         |             |
| 00E5h   | Port P3 Register           | P3      | XXh         |
| 00E6h   |                            |         |             |
| 00E7h   | Port P3 Direction Register | PD3     | 00h         |
| 00E8h   | Port P4 Register           | P4      | XXh         |
| 00E9h   |                            |         |             |
| 00EAh   | Port P4 Direction Register | PD4     | 00h         |
| 00EBh   |                            |         |             |
| 00ECh   |                            |         |             |
| 00EDh   |                            |         |             |
| 00EEh   |                            |         |             |
| 00EFh   |                            |         |             |
| 00F0h   |                            |         |             |
| 00F1h   |                            |         |             |
| 00F2h   |                            |         |             |
| 00F3h   |                            |         |             |
| 00F4h   |                            |         |             |
| 00F5h   |                            |         |             |
| 00F6h   |                            |         |             |
| 00F7h   |                            |         |             |
| 00F8h   |                            |         |             |
| 00F9h   |                            |         |             |
| 00FAh   |                            |         |             |
| 00FBh   |                            |         |             |
| 00FCh   |                            |         |             |
| 00FDh   |                            |         |             |
| 00FEh   |                            |         |             |
| 00FFh   |                            |         |             |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.5 SFR Information (5) (1)**

| Address | Register   | Symbol  | After Reset |
|---------|--|---------|-------------|
| 0100h   | Timer RA Control Register                        | TRACR   | 00h         |
| 0101h   | Timer RA I/O Control Register                    | TRAIOC  | 00h         |
| 0102h   | Timer RA Mode Register                           | TRAMR   | 00h         |
| 0103h   | Timer RA Prescaler Register                      | TRAPRE  | FFh         |
| 0104h   | Timer RA Register                                | TRA     | FFh         |
| 0105h   |  |         |             |
| 0106h   |  |         |             |
| 0107h   |  |         |             |
| 0108h   | Timer RB Control Register                        | TRBCR   | 00h         |
| 0109h   | Timer RB One-Shot Control Register               | TRBOCR  | 00h         |
| 010Ah   | Timer RB I/O Control Register                    | TRBIOC  | 00h         |
| 010Bh   | Timer RB Mode Register                           | TRBMR   | 00h         |
| 010Ch   | Timer RB Prescaler Register                      | TRBPRE  | FFh         |
| 010Dh   | Timer RB Secondary Register                      | TRBSC   | FFh         |
| 010Eh   | Timer RB Primary Register                        | TRBPR   | FFh         |
| 010Fh   |  |         |             |
| 0110h   |  |         |             |
| 0111h   |  |         |             |
| 0112h   |  |         |             |
| 0113h   |  |         |             |
| 0114h   |  |         |             |
| 0115h   |  |         |             |
| 0116h   |  |         |             |
| 0117h   |  |         |             |
| 0118h   | Timer RE Second Data Register                    | TRESEC  | 00h         |
| 0119h   | Timer RE Minute Data Register                    | TREMIN  | 00h         |
| 011Ah   | Timer RE Hour Data Register                      | TREHR   | 00h         |
| 011Bh   | Timer RE Day of Week Data Register               | TREWK   | 00h         |
| 011Ch   | Timer RE Control Register 1                      | TRECR1  | 00h         |
| 011Dh   | Timer RE Control Register 2                      | TRECR2  | 00h         |
| 011Eh   | Timer RE Count Source Select Register            | TRECSR  | 00001000b   |
| 011Fh   |  |         |             |
| 0120h   | Timer RC Mode Register                           | TRCMR   | 01001000b   |
| 0121h   | Timer RC Control Register 1                      | TRCCR1  | 00h         |
| 0122h   | Timer RC Interrupt Enable Register               | TRCIER  | 01110000b   |
| 0123h   | Timer RC Status Register                         | TRCSR   | 01110000b   |
| 0124h   | Timer RC I/O Control Register 0                  | TRCIOR0 | 10001000b   |
| 0125h   | Timer RC I/O Control Register 1                  | TRCIOR1 | 10001000b   |
| 0126h   | Timer RC Counter                                 | TRC     | 00h         |
| 0127h   |  |         | 00h         |
| 0128h   | Timer RC General Register A                      | TRCGRA  | FFh         |
| 0129h   |  |         | FFh         |
| 012Ah   | Timer RC General Register B                      | TRCGRB  | FFh         |
| 012Bh   |  |         | FFh         |
| 012Ch   | Timer RC General Register C                      | TRCGRC  | FFh         |
| 012Dh   |  |         | FFh         |
| 012Eh   | Timer RC General Register D                      | TRCGRD  | FFh         |
| 012Fh   |  |         | FFh         |
| 0130h   | Timer RC Control Register 2                      | TRCCR2  | 00011000b   |
| 0131h   | Timer RC Digital Filter Function Select Register | TRCDF   | 00h         |
| 0132h   | Timer RC Output Master Enable Register           | TRCOER  | 01111111b   |
| 0133h   | Timer RC Trigger Control Register                | TRCADCR | 00h         |
| 0134h   |  |         |             |
| 0135h   |  |         |             |
| 0136h   |  |         |             |
| 0137h   |  |         |             |
| 0138h   |  |         |             |
| 0139h   |  |         |             |
| 013Ah   |  |         |             |
| 013Bh   |  |         |             |
| 013Ch   |  |         |             |
| 013Dh   |  |         |             |
| 013Eh   |  |         |             |
| 013Fh   |  |         |             |
| 0140h   |  |         |             |
| :       |  |         |             |
| 017Fh   |  |         |             |

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.6 SFR Information (6) (1)**

| Address | Register                                | Symbol  | After Reset |
|---------|---|---------|-------------|
| 0180h   | Timer RA Pin Select Register            | TRASR   | 00h         |
| 0181h   | Timer RC Pin Select Register            | TRBRCSR | 00h         |
| 0182h   | Timer RC Pin Select Register 0          | TRCPSR0 | 00h         |
| 0183h   | Timer RC Pin Select Register 1          | TRCPSR1 | 00h         |
| 0184h   |   |         |             |
| 0185h   |   |         |             |
| 0186h   |   |         |             |
| 0187h   |   |         |             |
| 0188h   | UART0 Pin Select Register               | U0SR    | 00h         |
| 0189h   |   |         |             |
| 018Ah   | UART2 Pin Select Register 0             | U2SR0   | 00h         |
| 018Bh   | UART2 Pin Select Register 1             | U2SR1   | 00h         |
| 018Ch   |   |         |             |
| 018Dh   |   |         |             |
| 018Eh   | INT Interrupt Input Pin Select Register | INTSR   | 00h         |
| 018Fh   | I/O Function Pin Select Register        | PINSR   | 00h         |
| 0190h   |   |         |             |
| 0191h   |   |         |             |
| 0192h   |   |         |             |
| 0193h   |   |         |             |
| 0194h   |   |         |             |
| 0195h   |   |         |             |
| 0196h   |   |         |             |
| 0197h   |   |         |             |
| 0198h   |   |         |             |
| 0199h   |   |         |             |
| 019Ah   |   |         |             |
| 019Bh   |   |         |             |
| 019Ch   |   |         |             |
| 019Dh   |   |         |             |
| 019Eh   |   |         |             |
| 019Fh   |   |         |             |
| 01A0h   |   |         |             |
| 01A1h   |   |         |             |
| 01A2h   |   |         |             |
| 01A3h   |   |         |             |
| 01A4h   |   |         |             |
| 01A5h   |   |         |             |
| 01A6h   |   |         |             |
| 01A7h   |   |         |             |
| 01A8h   |   |         |             |
| 01A9h   |   |         |             |
| 01AAh   |   |         |             |
| 01ABh   |   |         |             |
| 01ACh   |   |         |             |
| 01ADh   |   |         |             |
| 01AEh   |   |         |             |
| 01AFh   |   |         |             |
| 01B0h   |   |         |             |
| 01B1h   |   |         |             |
| 01B2h   | Flash Memory Status Register            | FST     | 10000X00b   |
| 01B3h   |   |         |             |
| 01B4h   | Flash Memory Control Register 0         | FMR0    | 00h         |
| 01B5h   | Flash Memory Control Register 1         | FMR1    | 00h         |
| 01B6h   | Flash Memory Control Register 2         | FMR2    | 00h         |
| 01B7h   |   |         |             |
| 01B8h   |   |         |             |
| 01B9h   |   |         |             |
| 01BAh   |   |         |             |
| 01BBh   |   |         |             |
| 01BCh   |   |         |             |
| 01BDh   |   |         |             |
| 01BEh   |   |         |             |
| 01BFh   |   |         |             |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.7 SFR Information (7) (1)**

| Address | Register                                | Symbol | After Reset |
|---------|---|--------|-------------|
| 01C0h   | Address Match Interrupt Register 0      | RMAD0  | XXh         |
| 01C1h   |   |        | XXh         |
| 01C2h   |   |        | 0000XXXXb   |
| 01C3h   | Address Match Interrupt Enable Register | AIER   | 00h         |
| 01C4h   | Address Match Interrupt Register 1      | RMAD1  | XXh         |
| 01C5h   |   |        | XXh         |
| 01C6h   |   |        | 0000XXXXb   |
| 01C7h   |   |        |             |
| 01C8h   |   |        |             |
| 01C9h   |   |        |             |
| 01CAh   |   |        |             |
| 01CBh   |   |        |             |
| 01CCh   |   |        |             |
| 01CDh   |   |        |             |
| 01CEh   |   |        |             |
| 01CFh   |   |        |             |
| 01D0h   |   |        |             |
| 01D1h   |   |        |             |
| 01D2h   |   |        |             |
| 01D3h   |   |        |             |
| 01D4h   |   |        |             |
| 01D5h   |   |        |             |
| 01D6h   |   |        |             |
| 01D7h   |   |        |             |
| 01D8h   |   |        |             |
| 01D9h   |   |        |             |
| 01DAh   |   |        |             |
| 01DBh   |   |        |             |
| 01DCh   |   |        |             |
| 01DDh   |   |        |             |
| 01DEh   |   |        |             |
| 01DFh   |   |        |             |
| 01E0h   | Pull-Up Control Register 0              | PUR0   | 00h         |
| 01E1h   | Pull-Up Control Register 1              | PUR1   | 00h         |
| 01E2h   |   |        |             |
| 01E3h   |   |        |             |
| 01E4h   |   |        |             |
| 01E5h   |   |        |             |
| 01E6h   |   |        |             |
| 01E7h   |   |        |             |
| 01E8h   |   |        |             |
| 01E9h   |   |        |             |
| 01EAh   |   |        |             |
| 01EBh   |   |        |             |
| 01ECh   |   |        |             |
| 01EDh   |   |        |             |
| 01EEh   |   |        |             |
| 01EFh   |   |        |             |
| 01F0h   | Port P1 Drive Capacity Control Register | P1DRR  | 00h         |
| 01F1h   |   |        |             |
| 01F2h   | Drive Capacity Control Register 0       | DRR0   | 00h         |
| 01F3h   | Drive Capacity Control Register 1       | DRR1   | 00h         |
| 01F4h   |   |        |             |
| 01F5h   | Input Threshold Control Register 0      | VLT0   | 00h         |
| 01F6h   | Input Threshold Control Register 1      | VLT1   | 00h         |
| 01F7h   |   |        |             |
| 01F8h   | Comparator B Control Register 0         | INTCMP | 00h         |
| 01F9h   |   |        |             |
| 01FAh   | External Input Enable Register 0        | INTEN  | 00h         |
| 01FBh   |   |        |             |
| 01FCh   | INT Input Filter Select Register 0      | INTF   | 00h         |
| 01FDh   |   |        |             |
| 01FEh   | Key Input Enable Register 0             | KIEN   | 00h         |
| 01FFh   |   |        |             |

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

**Table 4.8 ID Code Areas and Option Function Select Area**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| FFDBh   | Option Function Select Register 2 | OFS2   | (Note 1)    |
| FFDFh   | ID1                               |        | (Note 2)    |
| FFE3h   | ID2                               |        | (Note 2)    |
| FFEBh   | ID3                               |        | (Note 2)    |
| FEFh    | ID4                               |        | (Note 2)    |
| FFF3h   | ID5                               |        | (Note 2)    |
| FFF7h   | ID6                               |        | (Note 2)    |
| FFFBh   | ID7                               |        | (Note 2)    |
| FFFFh   | Option Function Select Register   | OFS    | (Note 1)    |

## Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.  
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user. When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh. When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user. When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

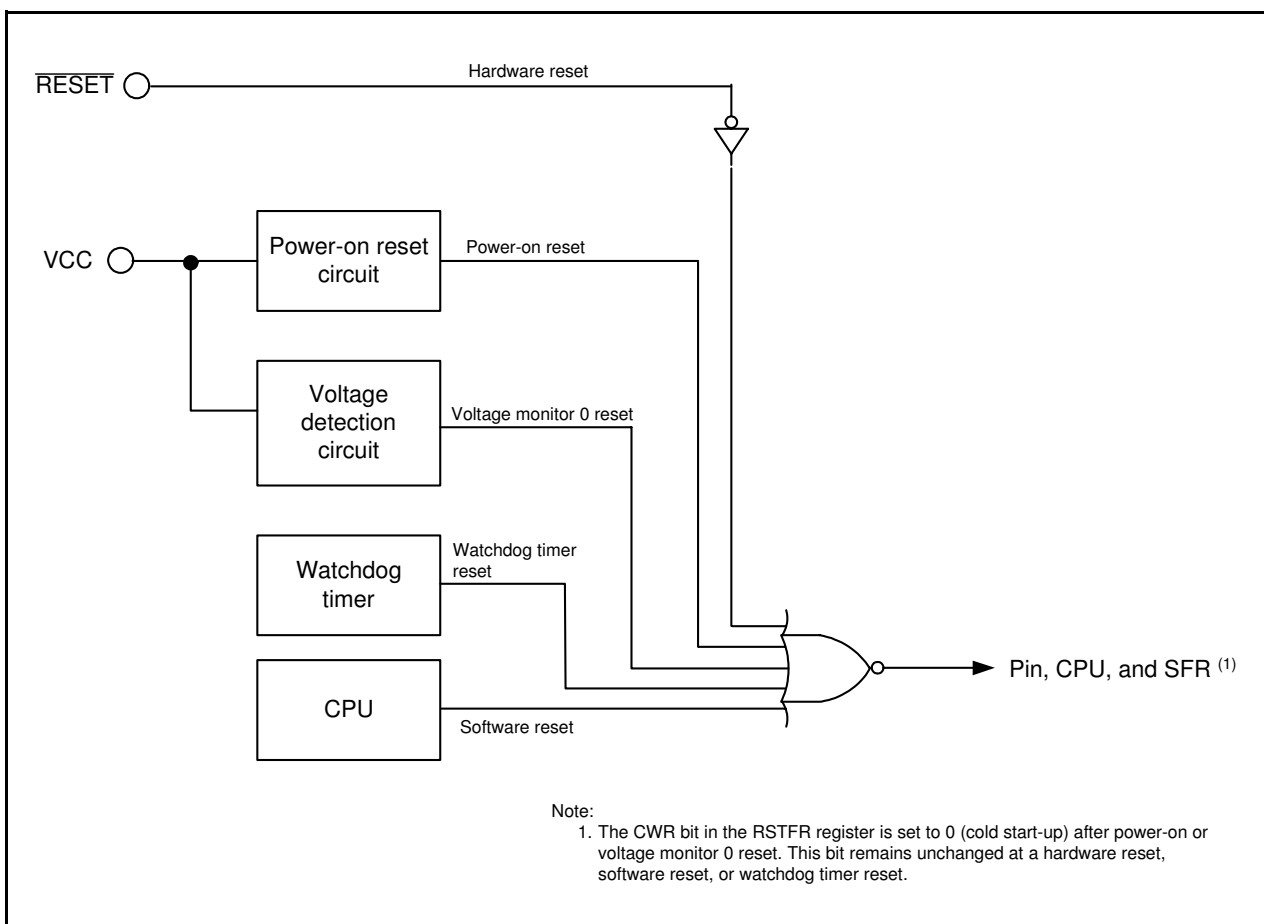
## 5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.

Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows the Block Diagram of Reset Circuit.

**Table 5.1 Reset Names and Sources**

| Reset Name              | Source   |
|-------------------------|--|
| Hardware reset          | Input voltage of $\overline{\text{RESET}}$ pin is held "L" |
| Power-on reset          | VCC rises  |
| Voltage monitor 0 reset | VCC falls (monitor voltage: Vdet0)                         |
| Watchdog timer reset    | Underflow of watchdog timer                                |
| Software reset          | Write 1 to PM03 bit in PM0 register                        |

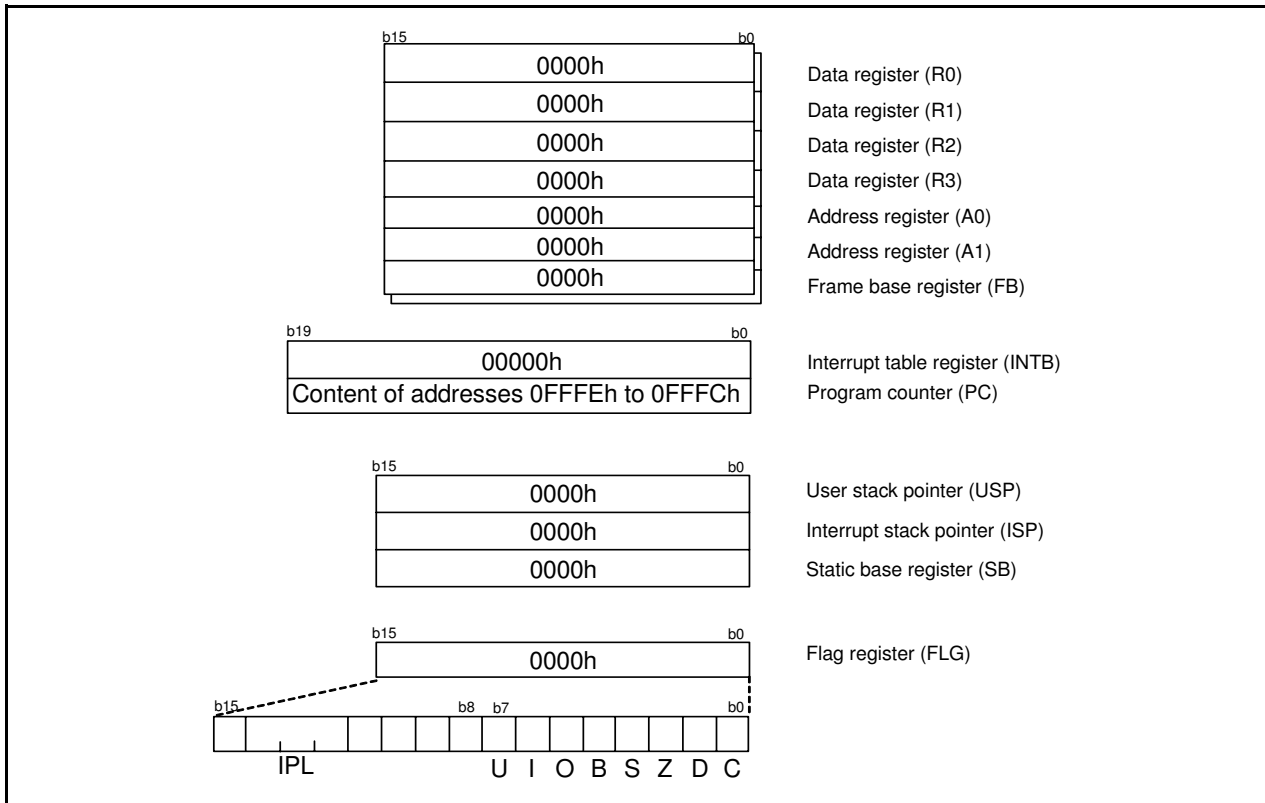


**Figure 5.1 Block Diagram of Reset Circuit**

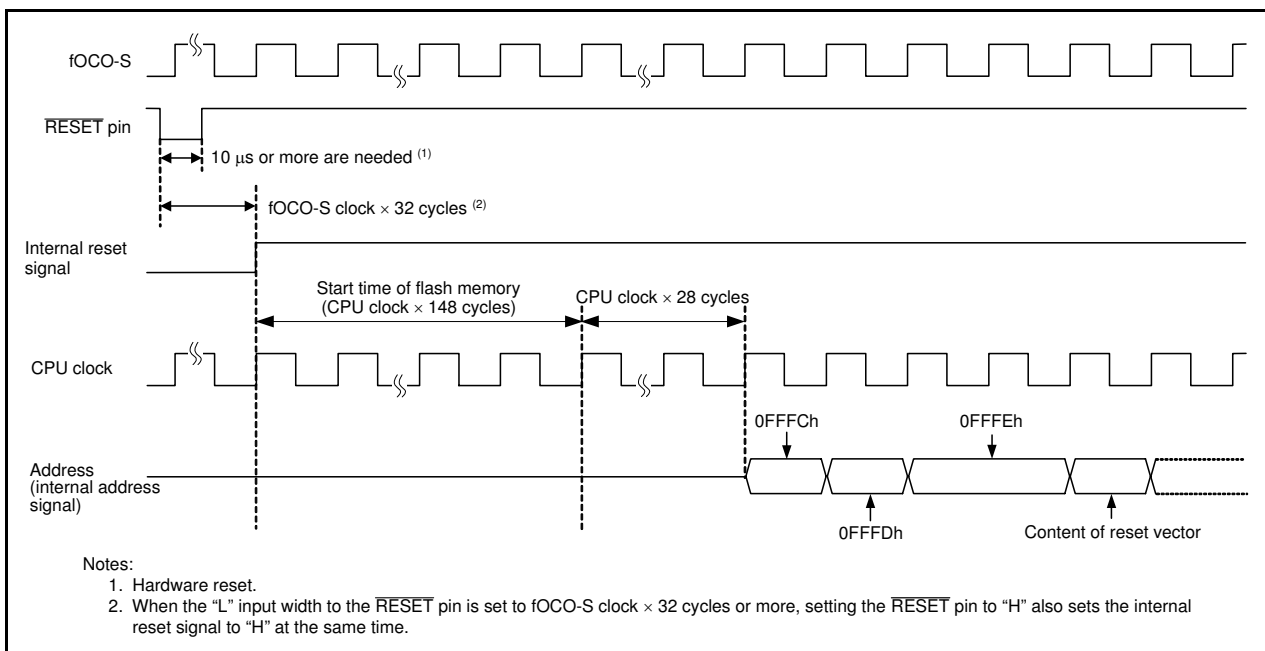
Table 5.2 lists the Pin Functions while  $\overline{\text{RESET}}$  Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence.

**Table 5.2 Pin Functions while  $\overline{\text{RESET}}$  Pin Level is “L”**

| Pin Name   | Pin Function |
|--|--------------|
| P0_1, P0_2, P0_6, P0_7, P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_2, P4_5 to P4_7 | Input port   |



**Figure 5.2 CPU Register Status after Reset**



**Figure 5.3 Reset Sequence**



## 5.1 Registers

### 5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

| Bit         | b7 | b6 | b5 | b4 | b3   | b2 | b1 | b0 |
|-------------|----|----|----|----|------|----|----|----|
| Symbol      | —  | —  | —  | —  | PM03 | —  | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 0    | 0  | 0  | 0  |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | —      | Reserved bits   | Set to 0.  | R/W |
| b1  | —      |   |  |     |
| b2  | —      |   |  |     |
| b3  | PM03   | Software reset bit  | The MCU is reset when this bit is set to 1. When read, the content is 0. | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

### 5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

| Bit         | b7 | b6 | b5 | b4 | b3  | b2  | b1  | b0  |
|-------------|----|----|----|----|-----|-----|-----|-----|
| Symbol      | —  | —  | —  | —  | WDR | SWR | HWR | CWR |
| After Reset | 0  | X  | X  | X  | X   | X   | X   | X   |

(Note 1)

| Bit | Symbol | Bit Name   | Function                             | R/W |
|-----|--------|--|--------------------------------------|-----|
| b0  | CWR    | Cold start-up/warm start-up determine flag <sup>(2, 3)</sup> | 0: Cold start-up<br>1: Warm start-up | R/W |
| b1  | HWR    | Hardware reset detect flag                                   | 0: Not detected<br>1: Detected       | R   |
| b2  | SWR    | Software reset detect flag                                   | 0: Not detected<br>1: Detected       | R   |
| b3  | WDR    | Watchdog timer reset detect flag                             | 0: Not detected<br>1: Detected       | R   |
| b4  | —      | Reserved bits  | When read, the content is undefined. | R   |
| b5  | —      |  |                                      |     |
| b6  | —      |  |                                      |     |
| b7  | —      | Reserved bit   | Set to 0.                            | R/W |

Notes:

1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. If 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VWOC0 bit in the VWOC register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.

### 5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

|             |                                   |       |        |        |        |       |    |       |
|-------------|-----------------------------------|-------|--------|--------|--------|-------|----|-------|
| Bit         | b7                                | b6    | b5     | b4     | b3     | b2    | b1 | b0    |
| Symbol      | CSPROINI                          | LVDAS | VDSEL1 | VDSEL0 | ROMCP1 | ROMCR | —  | WDTON |
| After Reset | User Setting Value <sup>(1)</sup> |       |        |        |        |       |    |       |

| Bit | Symbol   | Bit Name   | Function   | R/W |
|-----|----------|--|--|-----|
| b0  | WDTON    | Watchdog timer start select bit                      | 0: Watchdog timer automatically starts after reset.<br>1: Watchdog timer is stopped after reset.   | R/W |
| b1  | —        | Reserved bit   | Set to 1.  | R/W |
| b2  | ROMCR    | ROM code protect disable bit                         | 0: ROM code protect disabled<br>1: ROMCP1 bit enabled  | R/W |
| b3  | ROMCP1   | ROM code protect bit                                 | 0: ROM code protect enabled<br>1: ROM code protect disabled  | R/W |
| b4  | VDSEL0   | Voltage detection 0 level select bit <sup>(2)</sup>  | <sup>b5 b4</sup><br>0 0: 3.80 V selected (Vdet0_3)<br>0 1: 2.85 V selected (Vdet0_2)<br>1 0: 2.35 V selected (Vdet0_1)<br>1 1: 1.90 V selected (Vdet0_0) | R/W |
| b5  | VDSEL1   |  |  | R/W |
| b6  | LVDAS    | Voltage detection 0 circuit start bit <sup>(3)</sup> | 0: Voltage monitor 0 reset enabled after reset<br>1: Voltage monitor 0 reset disabled after reset  | R/W |
| b7  | CSPROINI | Count source protection mode after reset select bit  | 0: Count source protect mode enabled after reset<br>1: Count source protect mode disabled after reset  | R/W |

Notes:

- The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.  
When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
- The same level of the voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both functions of voltage monitor 0 reset and power-on reset.
- To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

### 5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

|             |                                   |    |    |    |         |         |         |         |
|-------------|-----------------------------------|----|----|----|---------|---------|---------|---------|
| Bit         | b7                                | b6 | b5 | b4 | b3      | b2      | b1      | b0      |
| Symbol      | —                                 | —  | —  | —  | WDTRCS1 | WDTRCS0 | WDTUFS1 | WDTUFS0 |
| After Reset | User Setting Value <sup>(1)</sup> |    |    |    |         |         |         |         |

| Bit | Symbol  | Bit Name  | Function   | R/W |
|-----|---------|---|--|-----|
| b0  | WDTUFS0 | Watchdog timer underflow period set bit               | <sup>b1 b0</sup><br>0 0: 03FFh<br>0 1: 0FFFh<br>1 0: 1FFFh<br>1 1: 3FFFh | R/W |
| b1  | WDTUFS1 |   |  | R/W |
| b2  | WDTRCS0 | Watchdog timer refresh acknowledgement period set bit | <sup>b3 b2</sup><br>0 0: 25%<br>0 1: 50%<br>1 0: 75%<br>1 1: 100%        | R/W |
| b3  | WDTRCS1 |   |  | R/W |
| b4  | —       | Reserved bits   | Set to 1.  | R/W |
| b5  | —       |   |  |     |
| b6  | —       |   |  |     |
| b7  | —       |   |  |     |

Note:

- The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.  
When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.  
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

## 5.2 Hardware Reset

A reset is applied using the  $\overline{\text{RESET}}$  pin. When an “L” signal is applied to the  $\overline{\text{RESET}}$  pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while RESET Pin Level is “L”**, **Figure 5.2 CPU Register Status after Reset**, and **Table 4.1 to Table 4.7 SFR Information**).

When the input level applied to the  $\overline{\text{RESET}}$  pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

The internal RAM is not reset. If the  $\overline{\text{RESET}}$  pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.

Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

### 5.2.1 When Power Supply is Stable

- (1) Apply “L” to the  $\overline{\text{RESET}}$  pin.
- (2) Wait for 10  $\mu\text{s}$ .
- (3) Apply “H” to the  $\overline{\text{RESET}}$  pin.

### 5.2.2 Power On

- (1) Apply “L” to the  $\overline{\text{RESET}}$  pin.
- (2) Let the supply voltage increase until it meets the recommended operating conditions.
- (3) Wait for  $t_{\text{d(P-R)}}$  or more to allow the internal power supply to stabilize (refer to **26. Electrical Characteristics**).
- (4) Wait for 10  $\mu\text{s}$ .
- (5) Apply “H” to the  $\overline{\text{RESET}}$  pin.

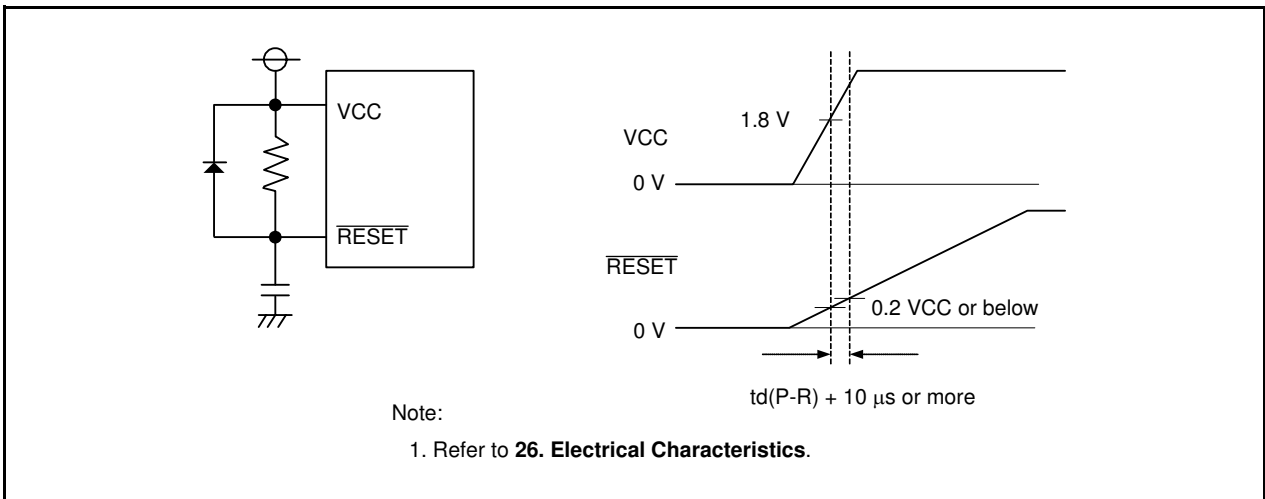


Figure 5.4 Example of Hardware Reset Circuit and Operation

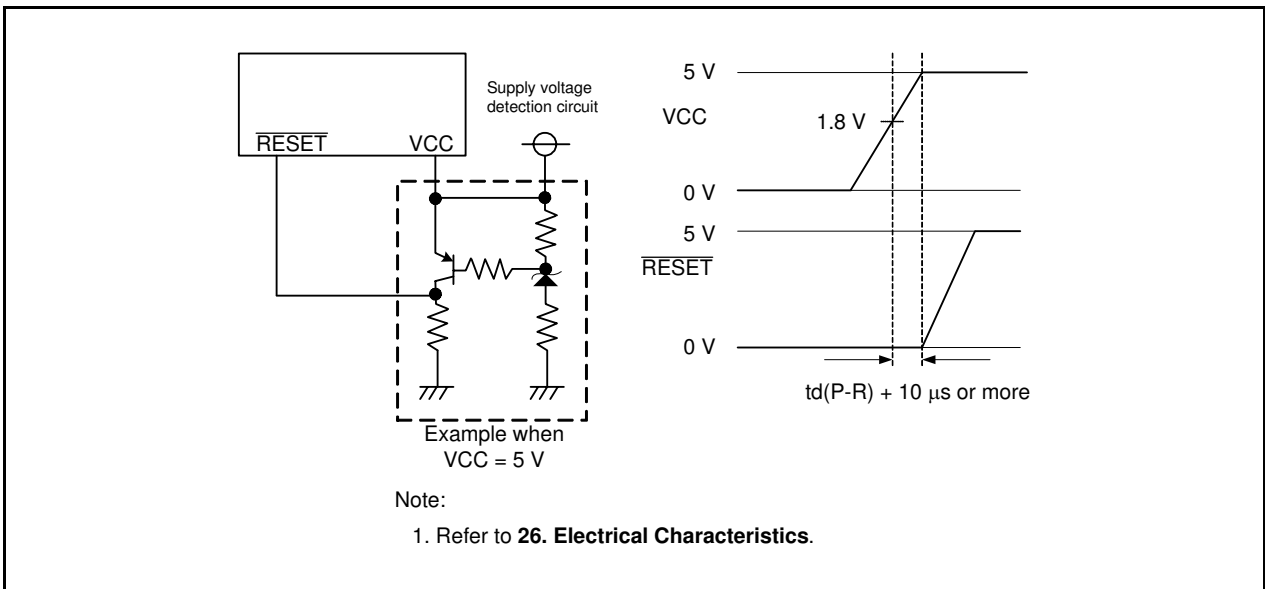


Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

### 5.3 Power-On Reset Function

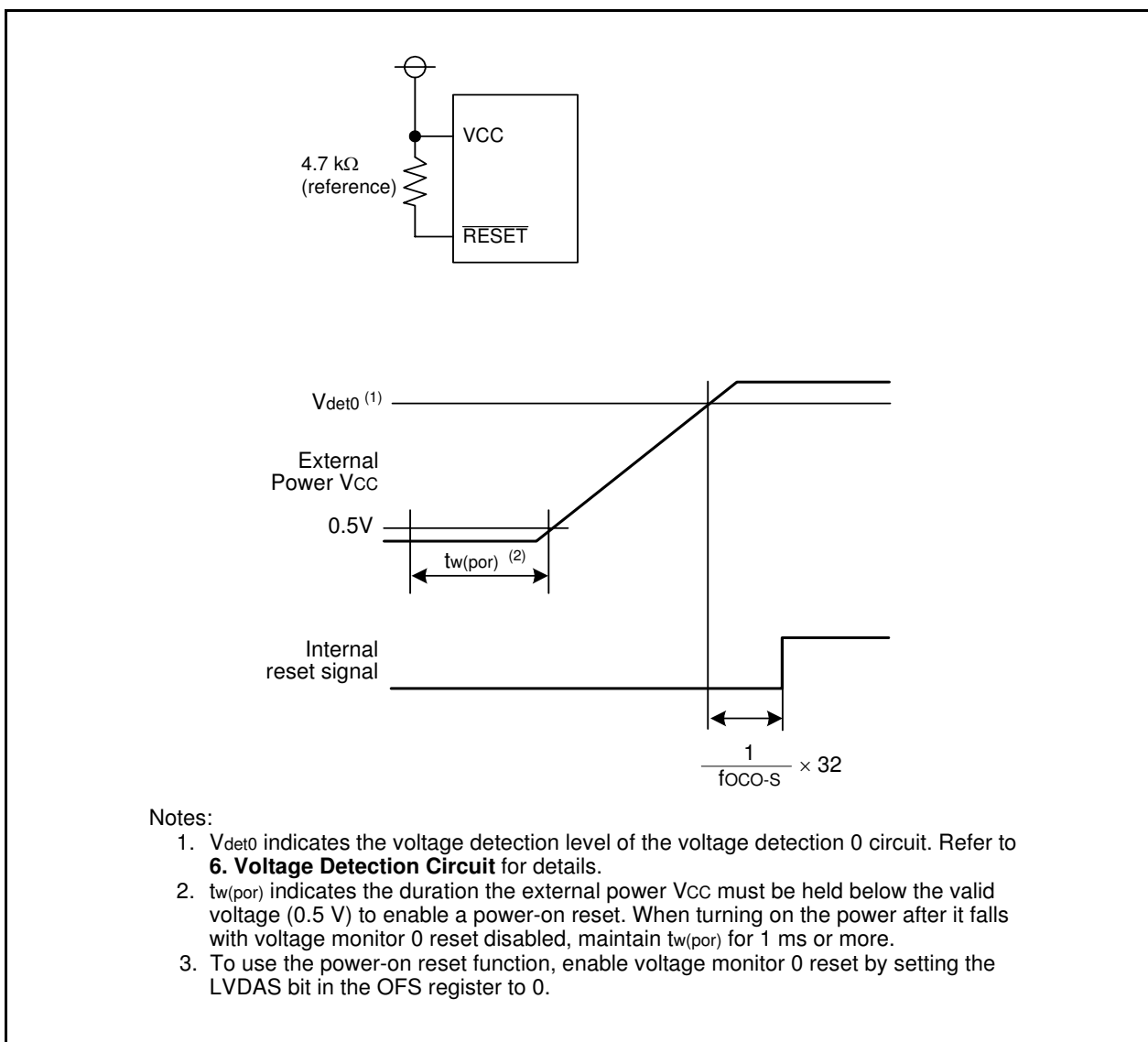
When the  $\overline{\text{RESET}}$  pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the  $\overline{\text{RESET}}$  pin, too, always keep the voltage to the  $\overline{\text{RESET}}$  pin  $0.8V_{\text{CC}}$  or more.

When the input voltage to the VCC pin reaches the  $V_{\text{det0}}$  level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFR after power-on reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



**Figure 5.6 Example of Power-On Reset Circuit and Operation**

## 5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFR are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock start counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

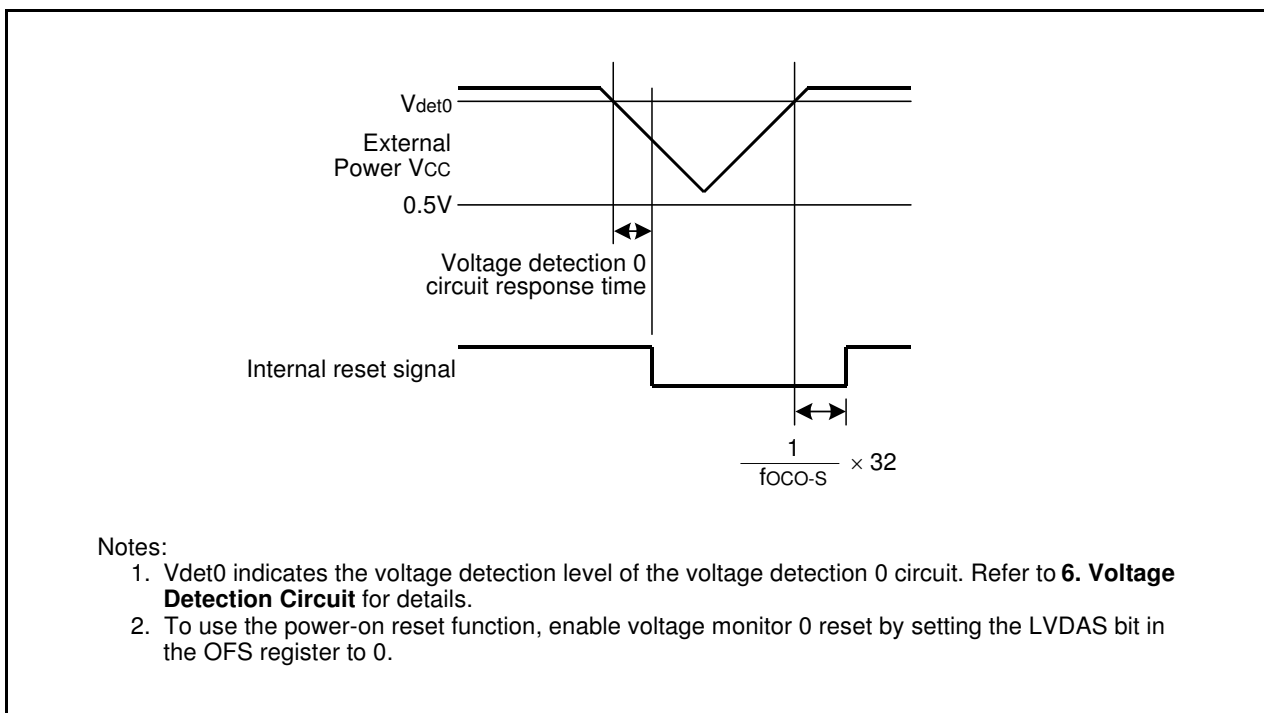
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



**Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation**

## 5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after watchdog timer reset.

The internal RAM is not reset. When the watchdog timer underflows, while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 to WDTUFS1 and bits WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.

Refer to **14. Watchdog Timer** for details of the watchdog timer.

## 5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after software reset.

The internal RAM is not reset.



## 5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.

The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.

The cold start-up/warm start-up determination function uses voltage monitor 0 reset.

Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

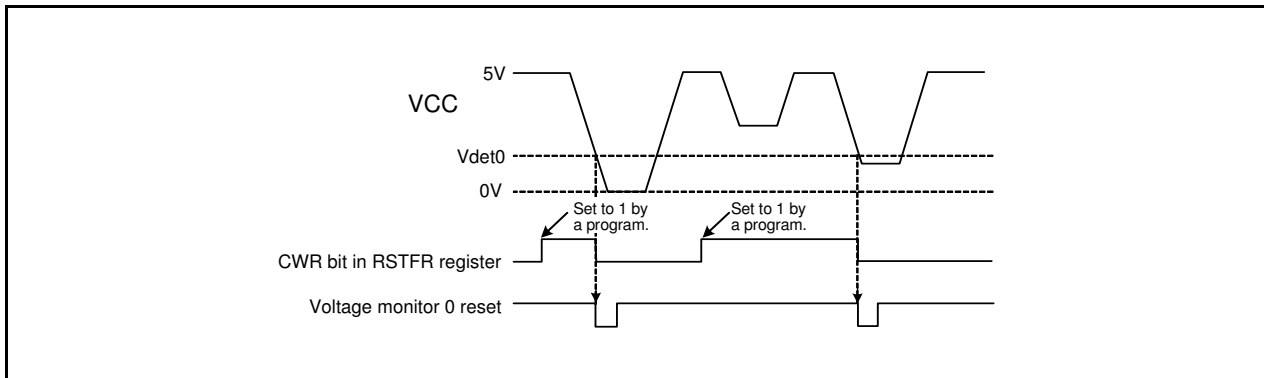


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

## 5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.

If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

## 6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

### 6.1 Overview

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.

The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.

The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

**Table 6.1 Voltage Detection Circuit Specifications**

| Item                         |                          | Voltage Monitor 0  | Voltage Monitor 1   | Voltage Monitor 2   |
|------------------------------|--------------------------|--|---|---|
| VCC monitor                  | Voltage to monitor       | Vdet0  | Vdet1   | Vdet2   |
|                              | Detection target         | Whether passing through Vdet0 by falling                       | Whether passing through Vdet1 by rising or falling                              | Whether passing through Vdet2 by rising or falling                              |
|                              | Detection voltage        | Selectable among 4 levels using the OFS register.              | Selectable among 16 levels using the VD1LS register.                            | The fixed level   |
|                              | Monitor                  | None   | The VW1C3 bit in the VW1C register<br>Whether VCC is higher or lower than Vdet1 | The VCA13 bit in the VCA1 register<br>Whether VCC is higher or lower than Vdet2 |
| Process at voltage detection | Reset                    | Voltage monitor 0 reset  | None  | None  |
|                              |                          | Reset at Vdet0 > VCC;<br>CPU operation restarts at VCC > Vdet0 |   |   |
|                              | Interrupts               | None   | Voltage monitor 1 interrupt<br>Non-maskable or maskable selectable              | Voltage monitor 2 interrupt<br>Non-maskable or maskable selectable              |
|                              |                          |  | Interrupt request at:<br>Vdet1 > VCC<br>and/or<br>VCC > Vdet1                   | Interrupt request at:<br>Vdet2 > VCC<br>and/or<br>VCC > Vdet2                   |
| Digital filter               | Switching enable/disable | No digital filter function                                     | Supported   | Supported   |
|                              | Sampling time            | —  | (fOCO-S divided by n) × 2<br>n: 1, 2, 4, and 8                                  | (fOCO-S divided by n) × 2<br>n: 1, 2, 4, and 8                                  |

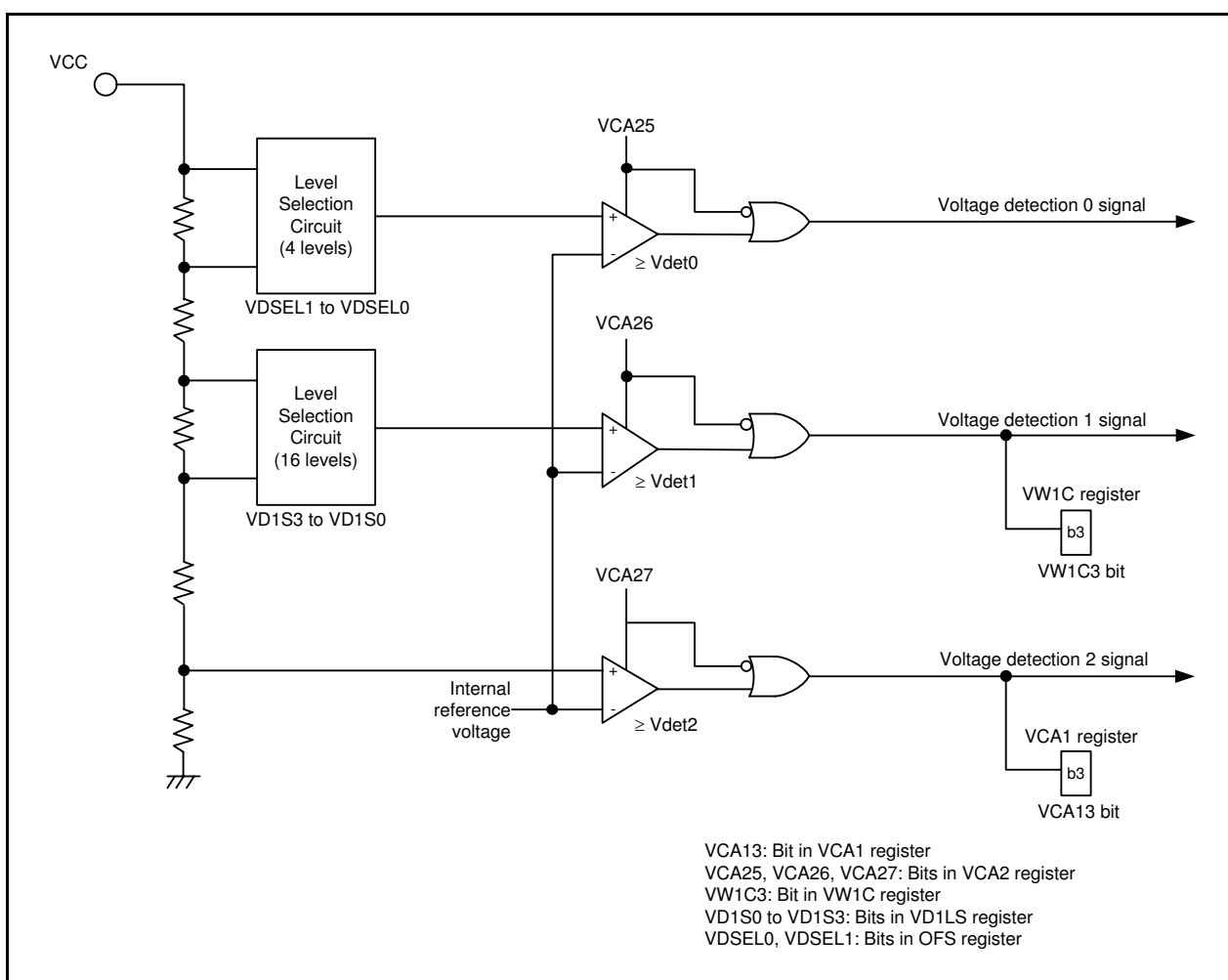


Figure 6.1 Voltage Detection Circuit Block Diagram

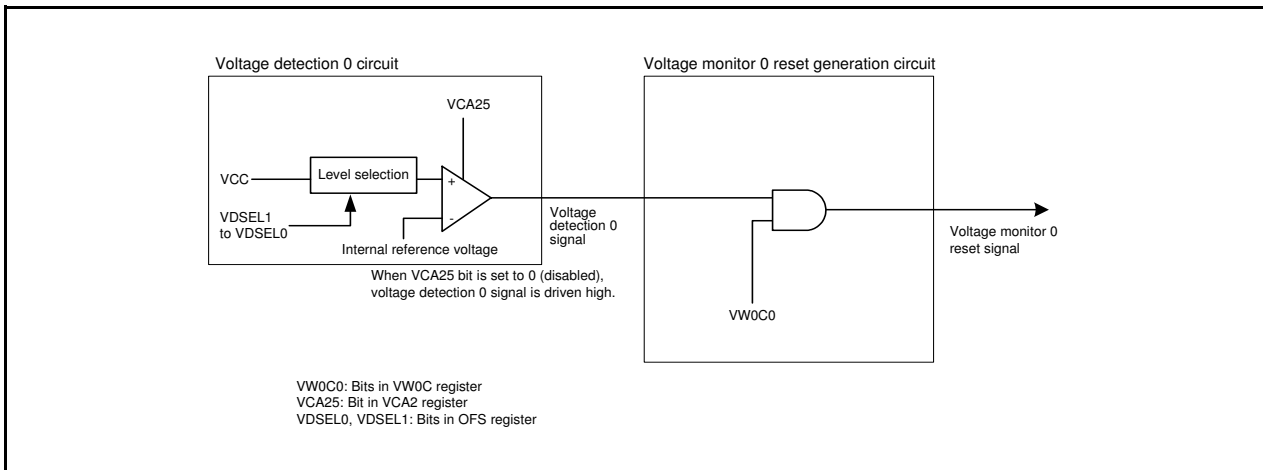


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

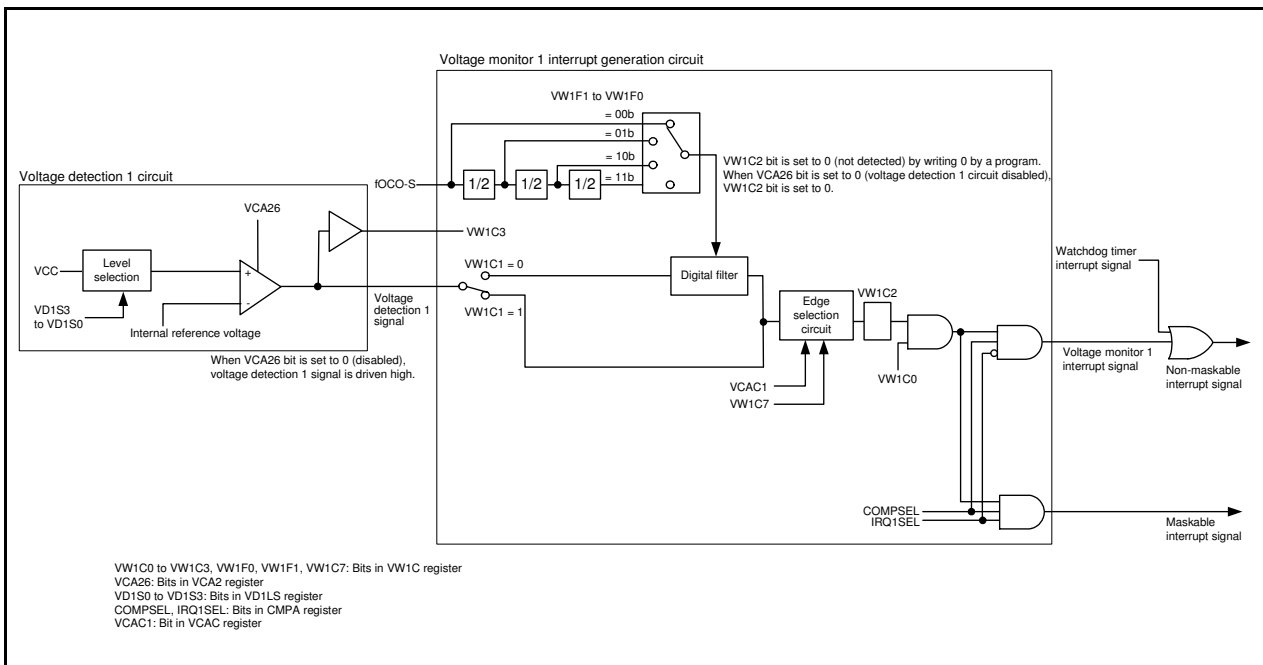
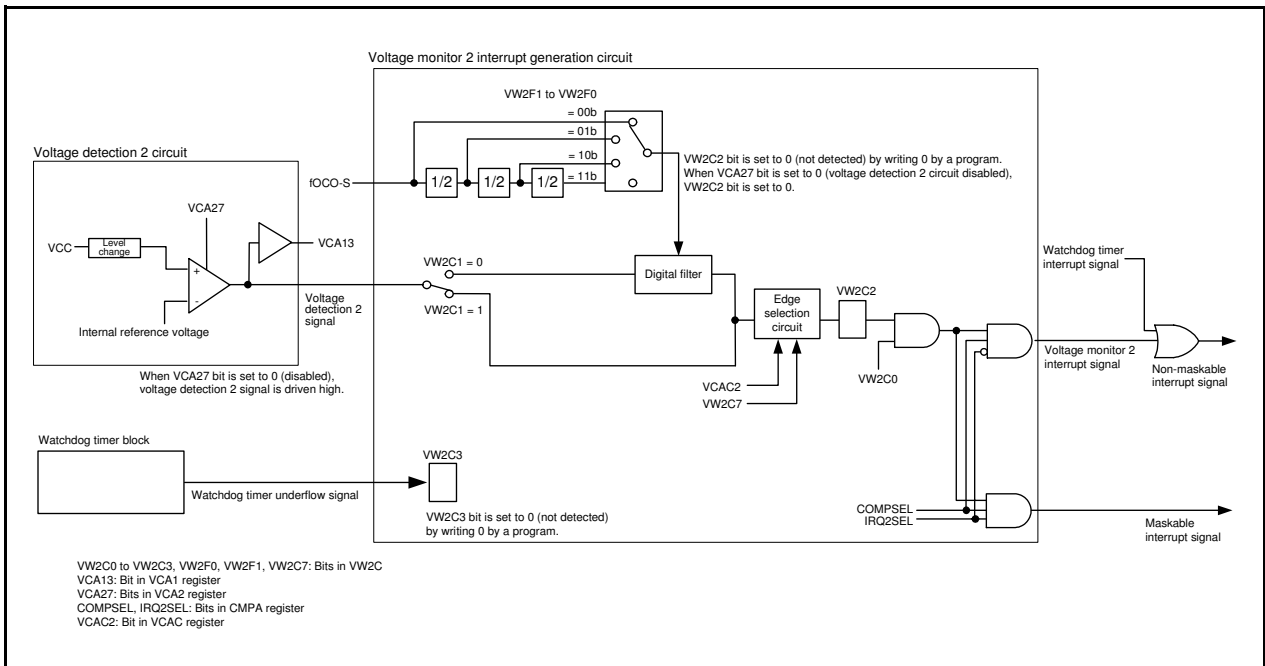


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit



**Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit**

## 6.2 Registers

### 6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

|             |         |    |         |         |    |    |    |    |
|-------------|---------|----|---------|---------|----|----|----|----|
| Bit         | b7      | b6 | b5      | b4      | b3 | b2 | b1 | b0 |
| Symbol      | COMPSEL | —  | IRQ2SEL | IRQ1SEL | —  | —  | —  | —  |
| After Reset | 0       | 0  | 0       | 0       | 0  | 0  | 0  | 0  |

| Bit | Symbol  | Bit Name  | Function  | R/W |
|-----|---------|---|---|-----|
| b0  | —       | Reserved bits   | Set to 0.   | R/W |
| b1  | —       |   |   |     |
| b2  | —       |   |   |     |
| b3  | —       |   |   |     |
| b4  | IRQ1SEL | Voltage monitor 1 interrupt type select bit <sup>(1)</sup>            | 0: Non-maskable interrupt<br>1: Maskable interrupt                          | R/W |
| b5  | IRQ2SEL | Voltage monitor 2 interrupt type select bit <sup>(2)</sup>            | 0: Non-maskable interrupt<br>1: Maskable interrupt                          | R/W |
| b6  | —       | Reserved bit  | Set to 0.   | R/W |
| b7  | COMPSEL | Voltage monitor interrupt type selection enable bit <sup>(1, 2)</sup> | 0: Bits IRQ1SEL and IRQ2SEL disabled<br>1: Bits IRQ1SEL and IRQ2SEL enabled | R/W |

Notes:

1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

## 6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

|             |    |    |    |    |    |       |       |    |
|-------------|----|----|----|----|----|-------|-------|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1    | b0 |
| Symbol      | —  | —  | —  | —  | —  | VCAC2 | VCAC1 | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0     | 0     | 0  |

| Bit | Symbol | Bit Name  | Function                     | R/W |
|-----|--------|---|------------------------------|-----|
| b0  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                              | —   |
| b1  | VCAC1  | Voltage monitor 1 circuit edge select bit <sup>(1)</sup>                  | 0: One edge<br>1: Both edges | R/W |
| b2  | VCAC2  | Voltage monitor 2 circuit edge select bit <sup>(2)</sup>                  | 0: One edge<br>1: Both edges | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                              | —   |
| b4  | —      |   |                              |     |
| b5  | —      |   |                              |     |
| b6  | —      |   |                              |     |
| b7  | —      |   |                              |     |

Notes:

- When the VCAC1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
- When the VCAC2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

## 6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

|             |    |    |    |    |       |    |    |    |
|-------------|----|----|----|----|-------|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3    | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | VCA13 | —  | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 1     | 0  | 0  | 0  |

| Bit | Symbol | Bit Name   | Function  | R/W |
|-----|--------|--|---|-----|
| b0  | —      | Reserved bits  | Set to 0.   | R/W |
| b1  | —      |  |   |     |
| b2  | —      |  |   |     |
| b3  | VCA13  | Voltage detection 2 signal monitor flag <sup>(1)</sup> | 0: VCC < Vdet2<br>1: VCC ≥ Vdet2<br>or voltage detection 2 circuit disabled | R   |
| b4  | —      | Reserved bits  | Set to 0.   | R/W |
| b5  | —      |  |   |     |
| b6  | —      |  |   |     |
| b7  | —      |  |   |     |

Note:

- When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.  
When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

## 6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

| Bit         | b7  | b6    | b5    | b4 | b3 | b2 | b1 | b0    |
|-------------|---|-------|-------|----|----|----|----|-------|
| Symbol      | VCA27   | VCA26 | VCA25 | —  | —  | —  | —  | VCA20 |
| After Reset | 0   | 0     | 0     | 0  | 0  | 0  | 0  | 0     |
|             | The above applies when the LVDAS bit in the OFS register is set to 1. |       |       |    |    |    |    |       |
| After Reset | 0   | 0     | 1     | 0  | 0  | 0  | 0  | 0     |
|             | The above applies when the LVDAS bit in the OFS register is set to 0. |       |       |    |    |    |    |       |

| Bit | Symbol | Bit Name   | Function  | R/W |
|-----|--------|--|---|-----|
| b0  | VCA20  | Internal power low consumption enable bit <sup>(1)</sup> | 0: Low consumption disabled<br>1: Low consumption enabled <sup>(2)</sup>          | R/W |
| b1  | —      | Reserved bits  | Set to 0.   | R/W |
| b2  | —      |  |   |     |
| b3  | —      |  |   |     |
| b4  | —      |  |   |     |
| b5  | VCA25  | Voltage detection 0 enable bit <sup>(3)</sup>            | 0: Voltage detection 0 circuit disabled<br>1: Voltage detection 0 circuit enabled | R/W |
| b6  | VCA26  | Voltage detection 1 enable bit <sup>(4)</sup>            | 0: Voltage detection 1 circuit disabled<br>1: Voltage detection 1 circuit enabled | R/W |
| b7  | VCA27  | Voltage detection 2 enable bit <sup>(5)</sup>            | 0: Voltage detection 2 circuit disabled<br>1: Voltage detection 2 circuit enabled | R/W |

Notes:

1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.



## 6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

|             |    |    |    |    |       |       |       |       |
|-------------|----|----|----|----|-------|-------|-------|-------|
| Bit         | b7 | b6 | b5 | b4 | b3    | b2    | b1    | b0    |
| Symbol      | —  | —  | —  | —  | VD1S3 | VD1S2 | VD1S1 | VD1S0 |
| After Reset | 0  | 0  | 0  | 0  | 0     | 1     | 1     | 1     |

| Bit | Symbol | Bit Name   | Function                                 | R/W |
|-----|--------|--|--|-----|
| b0  | VD1S0  | Voltage detection 1 level select bit<br>(Reference voltage when the voltage falls) | b3 b2 b1 b0<br>0 0 0 0: 2.20 V (Vdet1_0) | R/W |
| b1  | VD1S1  |  | 0 0 0 1: 2.35 V (Vdet1_1)                | R/W |
| b2  | VD1S2  |  | 0 0 1 0: 2.50 V (Vdet1_2)                | R/W |
| b3  | VD1S3  |  | 0 0 1 1: 2.65 V (Vdet1_3)                | R/W |
|     |        |  | 0 1 0 0: 2.80 V (Vdet1_4)                |     |
|     |        |  | 0 1 0 1: 2.95 V (Vdet1_5)                |     |
|     |        |  | 0 1 1 0: 3.10 V (Vdet1_6)                |     |
|     |        |  | 0 1 1 1: 3.25 V (Vdet1_7)                |     |
|     |        | 1 0 0 0: 3.40 V (Vdet1_8)  |  |     |
|     |        | 1 0 0 1: 3.55 V (Vdet1_9)  |  |     |
|     |        | 1 0 1 0: 3.70 V (Vdet1_A)  |  |     |
|     |        | 1 0 1 1: 3.85 V (Vdet1_B)  |  |     |
|     |        | 1 1 0 0: 4.00 V (Vdet1_C)  |  |     |
|     |        | 1 1 0 1: 4.15 V (Vdet1_D)  |  |     |
|     |        | 1 1 1 0: 4.30 V (Vdet1_E)  |  |     |
|     |        | 1 1 1 1: 4.45 V (Vdet1_F)  |  |     |
| b4  | —      | Reserved bits  | Set to 0.                                | R/W |
| b5  | —      |  |  |     |
| b6  | —      |  |  |     |
| b7  | —      |  |  |     |

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

### 6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

| Bit         | b7  | b6 | b5 | b4 | b3 | b2 | b1 | b0    |
|-------------|---|----|----|----|----|----|----|-------|
| Symbol      | —   | —  | —  | —  | —  | —  | —  | VW0C0 |
| After Reset | 1   | 1  | 0  | 0  | X  | 0  | 1  | 0     |
|             | The above applies when the LVDAS bit in the OFS register is set to 1. |    |    |    |    |    |    |       |
| After Reset | 1   | 1  | 0  | 0  | X  | 0  | 1  | 1     |
|             | The above applies when the LVDAS bit in the OFS register is set to 0. |    |    |    |    |    |    |       |

| Bit | Symbol | Bit Name  | Function                             | R/W |
|-----|--------|---|--------------------------------------|-----|
| b0  | VW0C0  | Voltage monitor 0 reset enable bit <sup>(1)</sup> | 0: Disabled<br>1: Enabled            | R/W |
| b1  | —      | Reserved bit                                      | Set to 1.                            | R/W |
| b2  | —      | Reserved bit                                      | Set to 0.                            | R/W |
| b3  | —      | Reserved bit                                      | When read, the content is undefined. | R   |
| b4  | —      | Reserved bits                                     | Set to 0.                            | R/W |
| b5  | —      |   |                                      |     |
| b6  | —      | Reserved bits                                     | Set to 1.                            | R/W |
| b7  | —      |   |                                      |     |

Note:

1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

## 6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

|             |       |    |       |       |       |       |       |       |
|-------------|-------|----|-------|-------|-------|-------|-------|-------|
| Bit         | b7    | b6 | b5    | b4    | b3    | b2    | b1    | b0    |
| Symbol      | VW1C7 | —  | VW1F1 | VW1F0 | VW1C3 | VW1C2 | VW1C1 | VW1C0 |
| After Reset | 1     | 0  | 0     | 0     | 1     | 0     | 1     | 0     |

| Bit | Symbol | Bit Name   | Function  | R/W |
|-----|--------|--|---|-----|
| b0  | VW1C0  | Voltage monitor 1 interrupt enable bit <sup>(1)</sup>                      | 0: Disabled<br>1: Enabled   | R/W |
| b1  | VW1C1  | Voltage monitor 1 digital filter disable mode select bit <sup>(2, 6)</sup> | 0: Digital filter enabled mode (digital filter circuit enabled)<br>1: Digital filter disable mode (digital filter circuit disabled) | R/W |
| b2  | VW1C2  | Voltage change detection flag <sup>(3, 4)</sup>                            | 0: Not detected<br>1: Vdet1 passing detected  | R/W |
| b3  | VW1C3  | Voltage detection 1 signal monitor flag <sup>(3)</sup>                     | 0: VCC < Vdet1<br>1: VCC ≥ Vdet1<br>or voltage detection 1 circuit disabled   | R   |
| b4  | VW1F0  | Sampling clock select bit <sup>(6)</sup>                                   | b5 b4<br>0 0: fOCO-S divided by 1<br>0 1: fOCO-S divided by 2<br>1 0: fOCO-S divided by 4<br>1 1: fOCO-S divided by 8               | R/W |
| b5  | VW1F1  |  |   | R/W |
| b6  | —      | Reserved bit   | Set to 0.   | R/W |
| b7  | VW1C7  | Voltage monitor 1 interrupt generation condition select bit <sup>(5)</sup> | 0: When VCC reaches Vdet1 or above.<br>1: When VCC reaches Vdet1 or below.  | R/W |

## Notes:

- The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled). To set the VW0C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
- When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on). To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
- Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
- Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
- The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
- When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.

Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

## 6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

|             |       |    |       |       |       |       |       |       |
|-------------|-------|----|-------|-------|-------|-------|-------|-------|
| Bit         | b7    | b6 | b5    | b4    | b3    | b2    | b1    | b0    |
| Symbol      | VW2C7 | —  | VW2F1 | VW2F0 | VW2C3 | VW2C2 | VW2C1 | VW2C0 |
| After Reset | 1     | 0  | 0     | 0     | 0     | 0     | 1     | 0     |

| Bit | Symbol | Bit Name   | Function   | R/W |
|-----|--------|--|--|-----|
| b0  | VW2C0  | Voltage monitor 2 interrupt enable bit <sup>(1)</sup>                      | 0: Disabled<br>1: Enabled  | R/W |
| b1  | VW2C1  | Voltage monitor 2 digital filter disable mode select bit <sup>(2, 6)</sup> | 0: Digital filter enable mode (digital filter circuit enabled)<br>1: Digital filter disable mode (digital filter circuit disabled) | R/W |
| b2  | VW2C2  | Voltage change detection flag <sup>(3, 4)</sup>                            | 0: Not detected<br>1: Vdet2 passing detected   | R/W |
| b3  | VW2C3  | WDT detection monitor flag <sup>(4)</sup>                                  | 0: Not detected<br>1: Detected   | R/W |
| b4  | VW2F0  | Sampling clock select bit <sup>(6)</sup>                                   | b5 b4<br>0 0: fOCO-S divided by 1<br>0 1: fOCO-S divided by 2<br>1 0: fOCO-S divided by 4<br>1 1: fOCO-S divided by 8              | R/W |
| b5  | VW2F1  |  |  | R/W |
| b6  | —      | Reserved bit   | Set to 0.  | R/W |
| b7  | VW2C7  | Voltage monitor 2 interrupt generation condition select bit <sup>(5)</sup> | 0: When VCC reaches Vdet2 or above.<br>1: When VCC reaches Vdet2 or below.   | R/W |

## Notes:

- The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled). To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
- When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on). To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
- The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
- Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
- The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
- When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.

Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

### 6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

|             |                                   |       |        |        |        |       |    |       |
|-------------|-----------------------------------|-------|--------|--------|--------|-------|----|-------|
| Bit         | b7                                | b6    | b5     | b4     | b3     | b2    | b1 | b0    |
| Symbol      | CSPROINI                          | LVDAS | VDSEL1 | VDSEL0 | ROMCP1 | ROMCR | —  | WDTON |
| After Reset | User Setting Value <sup>(1)</sup> |       |        |        |        |       |    |       |

| Bit | Symbol   | Bit Name   | Function  | R/W |
|-----|----------|--|---|-----|
| b0  | WDTON    | Watchdog timer start select bit                      | 0: Watchdog timer automatically starts after reset.<br>1: Watchdog timer is stopped after reset.  | R/W |
| b1  | —        | Reserved bit   | Set to 1.   | R/W |
| b2  | ROMCR    | ROM code protect disable bit                         | 0: ROM code protect disabled<br>1: ROMCP1 bit enabled   | R/W |
| b3  | ROMCP1   | ROM code protect bit                                 | 0: ROM code protect enabled<br>1: ROM code protect disabled   | R/W |
| b4  | VDSEL0   | Voltage detection 0 level select bit <sup>(2)</sup>  | b5 b4<br>0 0: 3.80 V selected (Vdet0_3)<br>0 1: 2.85 V selected (Vdet0_2)<br>1 0: 2.35 V selected (Vdet0_1)<br>1 1: 1.90 V selected (Vdet0_0) | R/W |
| b5  | VDSEL1   |  |   | R/W |
| b6  | LVDAS    | Voltage detection 0 circuit start bit <sup>(3)</sup> | 0: Voltage monitor 0 reset enabled after reset<br>1: Voltage monitor 0 reset disabled after reset   | R/W |
| b7  | CSPROINI | Count source protection mode after reset select bit  | 0: Count source protect mode enabled after reset<br>1: Count source protect mode disabled after reset   | R/W |

Notes:

- The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.  
When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
- The same level of the voltage detection 0 level selected by bits VDSEL0 and VDES1 is set in both functions of voltage monitor 0 reset and power-on reset.
- To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

## 6.3 VCC Input Voltage

### 6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

### 6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after  $t_d(E-A)$  has elapsed (refer to **26. Electrical Characteristics**).

- (1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
- (2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

### 6.3.3 Monitoring Vdet2

Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after  $t_d(E-A)$  has elapsed (refer to **26. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

## 6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.

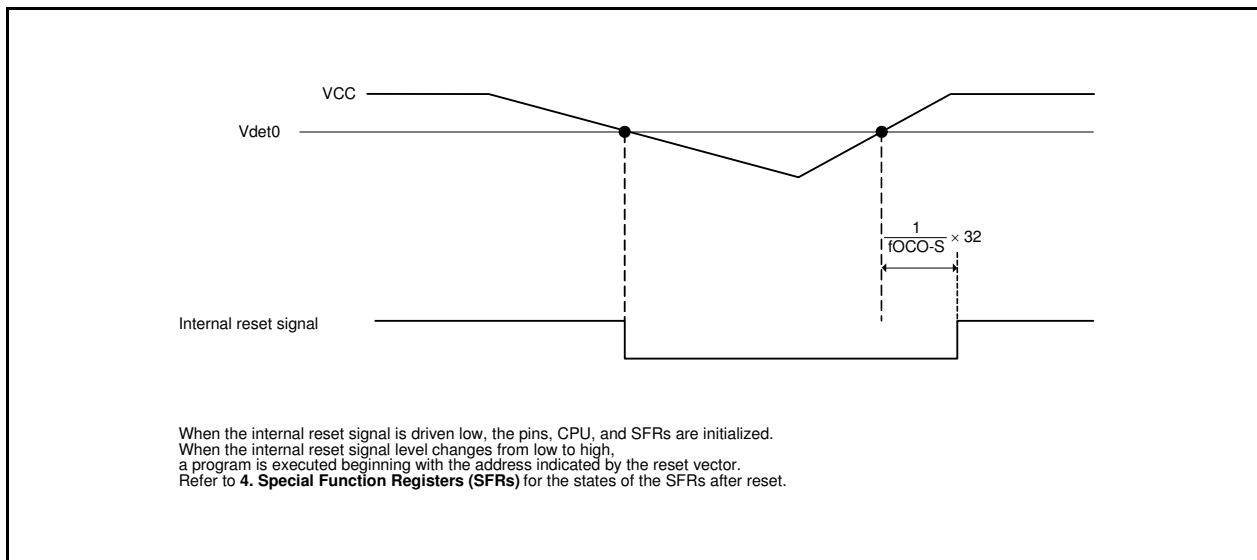


Figure 6.5 Operating Example of Voltage Monitor 0 Reset

## 6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.

To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

**Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**

| Step   | When Using Digital Filter   | When Using No Digital Filter   |
|--------|---|--|
| 1      | Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.                    |  |
| 2      | Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).                                |  |
| 3      | Wait for $t_d(E-A)$ .   |  |
| 4      | Set the COMPSEL bit in the CMPA register to 1.  |  |
| 5 (1)  | Select the interrupt type by the IRQ1SEL in the CMPA register.  |  |
| 6      | Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.                     | Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled). |
| 7 (2)  | Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).   | –  |
| 8      | Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register. |  |
| 9      | Set the VW1C2 bit in the VW1C register to 0.  |  |
| 10     | Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)                                       | –  |
| 11     | Wait for 2 cycles of the sampling clock of the digital filter   | – (No wait time required)  |
| 12 (3) | Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)                                 |  |

**Notes:**

- When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
- When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
- When making the setting while the voltage monitor 1 interrupt is disabled (the VW1C0 bit in the VW1C register is 0 and the VCA26 bit in the VCA2 register is 0), no interrupt request is generated if  $VCC < V_{det1}$  (or  $VCC > V_{det1}$ ) is detected before enabling the voltage monitor interrupt in step 12. If  $VCC < V_{det1}$  (or  $VCC > V_{det1}$ ) is detected between step 10 and step 12, the VW1C2 bit is set to 1. Read the VW1C2 bit after step 12. If this bit is read as 1, perform the processing to be executed when the above state is detected.



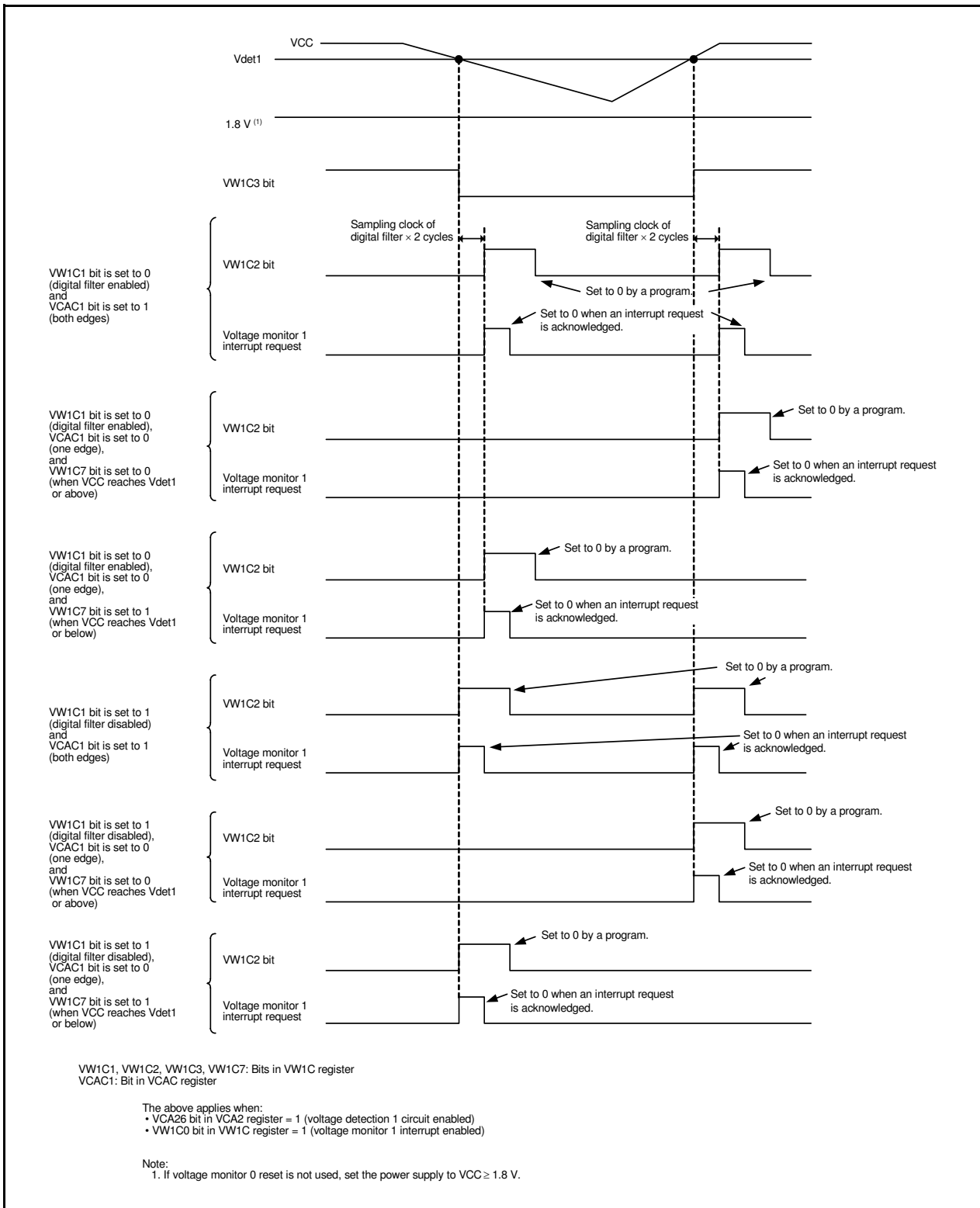


Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

## 6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.

To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

**Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**

| Step   | When Using Digital Filter   | When Using No Digital Filter   |
|--------|---|--|
| 1      | Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).                                |  |
| 2      | Wait for $t_d(E-A)$ .   |  |
| 3      | Set the COMPSEL bit in the CMPA register to 1.  |  |
| 4 (1)  | Select the interrupt type by the IRQ2SEL in the CMPA register.  |  |
| 5      | Select the sampling clock of the digital filter by bits VW2F0 and VW2F1 in the VW2C register.                     | Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled). |
| 6 (2)  | Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).   | –  |
| 7      | Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register. |  |
| 8      | Set the VW2C2 bit in the VW2C register to 0.  |  |
| 9      | Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).                                      | –  |
| 10     | Wait for 2 cycles of the sampling clock of the digital filter.  | – (No wait time required)  |
| 11 (3) | Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).                                |  |

Notes:

- When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
- When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
- When making the setting while the voltage monitor 2 interrupt is disabled (the VW2C0 bit in the VW2C register is 0 and the VCA27 bit in the VCA2 register is 0), no interrupt request is generated if  $VCC < V_{det2}$  (or  $VCC > V_{det2}$ ) is detected before enabling the voltage monitor interrupt in step 11. If  $VCC < V_{det2}$  (or  $VCC > V_{det2}$ ) is detected between step 9 and step 11, the VW2C2 bit is set to 1. Read the VW2C2 bit after step 11. If this bit is read as 1, perform the processing to be executed when the above state is detected.

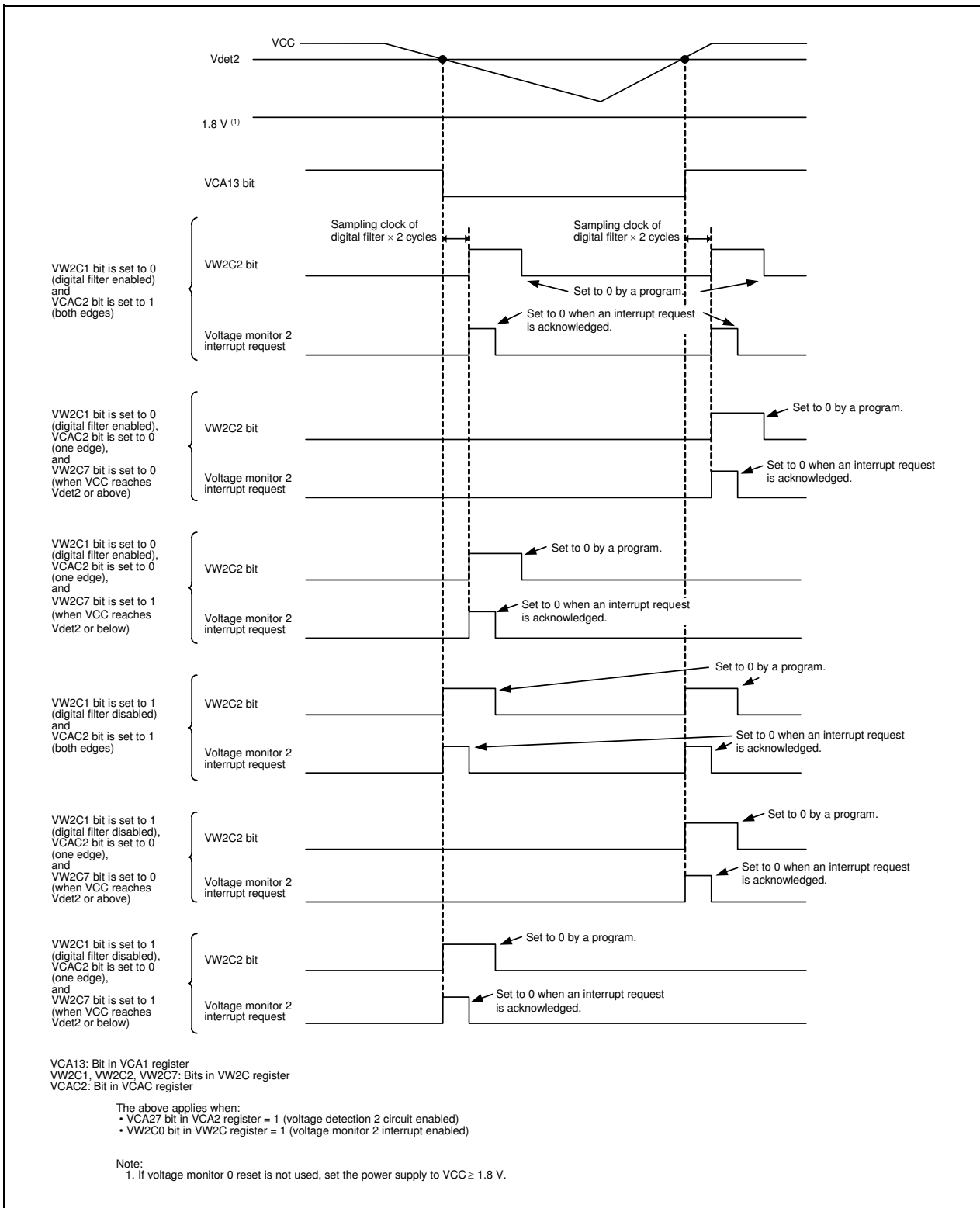


Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

## 7. I/O Ports

There are 19 I/O ports P0\_1, P0\_2, P0\_6, P0\_7, P1, P3\_3 to P3\_5, P3\_7, and P4\_5 to P4\_7 (P4\_6 and P4\_7 can be used as I/O ports if the XIN clock oscillation circuit and the XCIN clock oscillation circuit are not used.).

If A/D converter is not used, P4\_2 can be used as an input-only port.

Table 7.1 lists an Overview of I/O Ports.

**Table 7.1 Overview of I/O Ports**

| Ports   | I/O | Type of Output       | I/O Setting        | Internal Pull-Up Resister         | Drive Capacity Switch             | Input Level Switch                |
|---|-----|----------------------|--------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| P0_1, P0_2, P0_6, P0_7                          | I/O | CMOS3 state          | Set in 1-bit units | Set in 2-bit units <sup>(1)</sup> | Set in 2-bit units <sup>(3)</sup> | Set in 4-bit units <sup>(4)</sup> |
| P1  | I/O | CMOS3 state          | Set in 1-bit units | Set in 4-bit units <sup>(1)</sup> | Set in 1-bit units <sup>(2)</sup> | Set in 8-bit units <sup>(4)</sup> |
| P3_3  | I/O | CMOS3 state          | Set in 1-bit units | Set in 1-bit units <sup>(1)</sup> | Set in 1-bit units <sup>(3)</sup> | Set in 4-bit units <sup>(4)</sup> |
| P3_4, P3_5, P3_7                                | I/O | CMOS3 state          | Set in 1-bit units | Set in 3-bit units <sup>(1)</sup> | Set in 3-bit units <sup>(3)</sup> |                                   |
| P4_5, P4_6 <sup>(5)</sup> , P4_7 <sup>(5)</sup> | I/O | CMOS3 state          | Set in 1-bit units | Set in 3-bit units <sup>(1)</sup> | Set in 3-bit units <sup>(3)</sup> | Set in 4-bit units <sup>(4)</sup> |
| P4_2 <sup>(6)</sup>                             | I   | (No output function) | None               | None                              | None                              |                                   |

Notes:

1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0 and PUR1.
2. Whether the drive capacity of the output transistor is set to low or high can be selected using registers P1DRR and P2DRR.
3. Whether the drive capacity of the output transistor is set to low or high can be selected using registers DRR0 and DRR1.
4. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.
5. When the XIN clock oscillation circuit and the XCIN clock oscillation circuit are not used, these ports can be used as I/O ports.
6. When A/D converter is not used, this port can be used as an input-only ports.

### 7.1 Functions of I/O Ports

The PDi\_j (j = 0 to 7) bit in the PDi (i = 0 to 1, 3 to 4) register controls I/O of the ports P0\_1, P0\_2, P0\_6, P0\_7, P1, P3\_3 to P3\_5, P3\_7, and P4\_5 to P4\_7. The Pi register consists of a port latch to hold output data and a circuit to read pin states.

Figures 7.1 to 7.8 show the Configurations of I/O Ports. Table 7.2 lists the Functions of I/O Ports.

**Table 7.2 Functions of I/O Ports**

| Operation When Accessing Pi Register | Value of PDi_j Bit in PDi Register <sup>(1)</sup> |  |
|--------------------------------------|---|--|
|                                      | When PDi_j Bit is Set to 0 (Input Mode)           | When PDi_j Bit is Set to 1 (Output Mode)   |
| Read                                 | Read the pin input level.                         | Read the port latch.   |
| Write                                | Write to the port latch.                          | Write to the port latch. The value written to the port latch is output from the pin. |

i = 0 to 1, 3 to 4, j = 0 to 7

Note:

1. Nothing is assigned to bits PD4\_0 to PD4\_2.

## 7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (Refer to **Table 1.4 Pin Name Information by Pin Number**).

Table 7.3 lists the Setting of PDi\_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 1, 3 to 4, j = 0 to 7).

Refer to the description of each function for information on how to set peripheral functions.

**Table 7.3 Setting of PDi\_j Bit when Functioning as I/O Ports for Peripheral Functions  
(i = 0 to 1, 3 to 4, j = 0 to 7)**

| I/O of Peripheral Function | PDi_j Bit Settings for Shared Pin Function                                    |
|----------------------------|---|
| Input                      | Set this bit to 0 (input mode).   |
| Output                     | This bit can be set to either 0 or 1 (output regardless of the port setting). |

## 7.3 Pins Other than I/O Ports

Figure 7.9 shows the Configuration of I/O Pins.

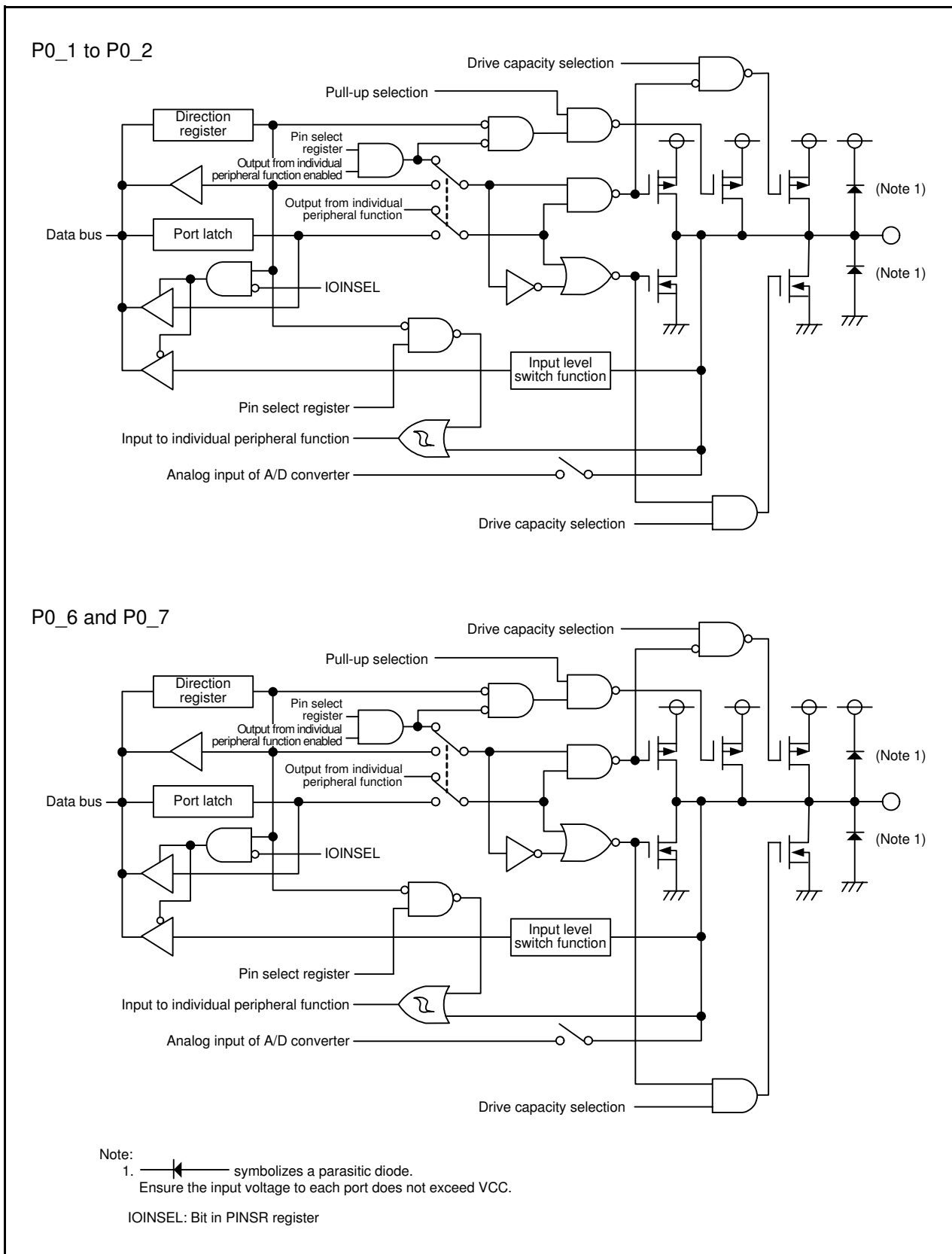


Figure 7.1 Configuration of I/O Ports (1)

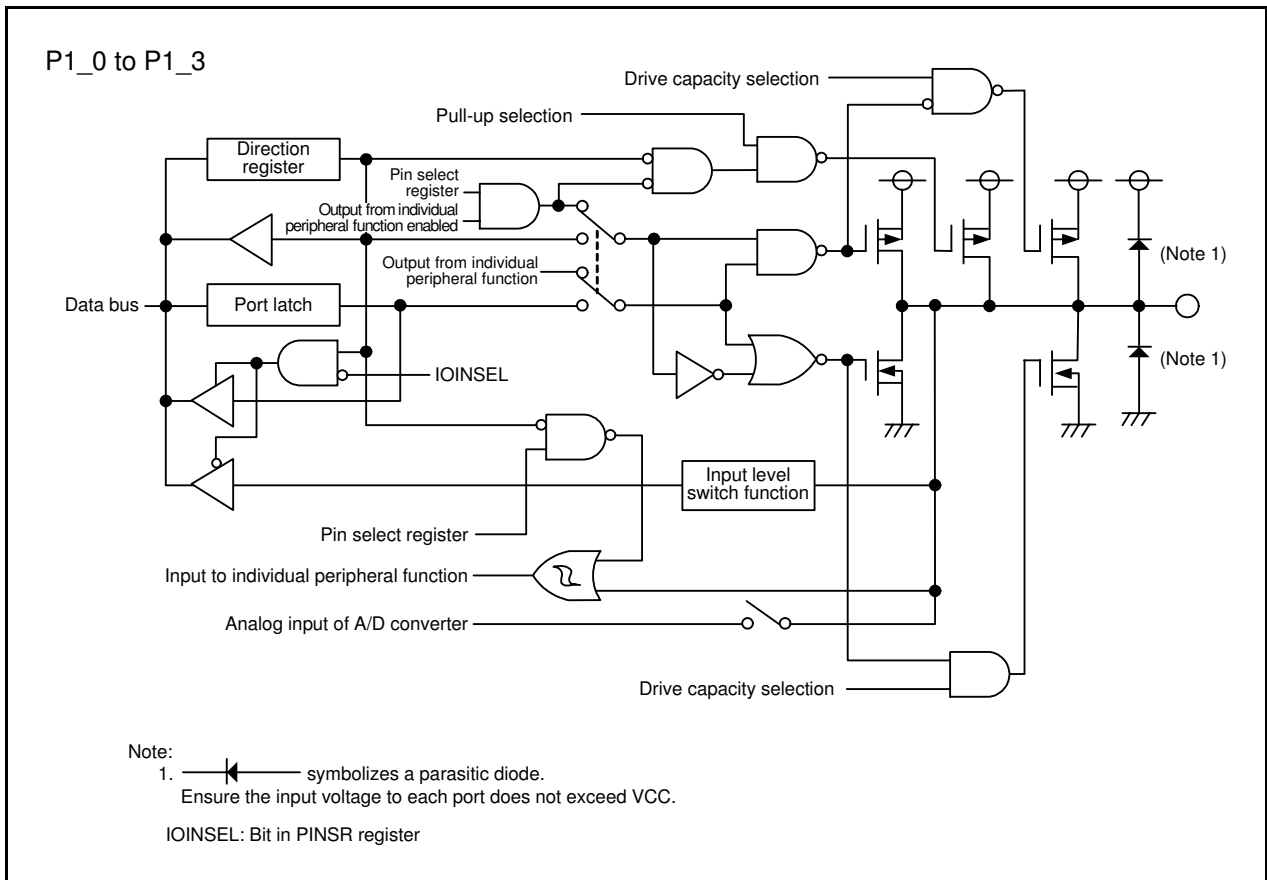


Figure 7.2 Configuration of I/O Ports (2)

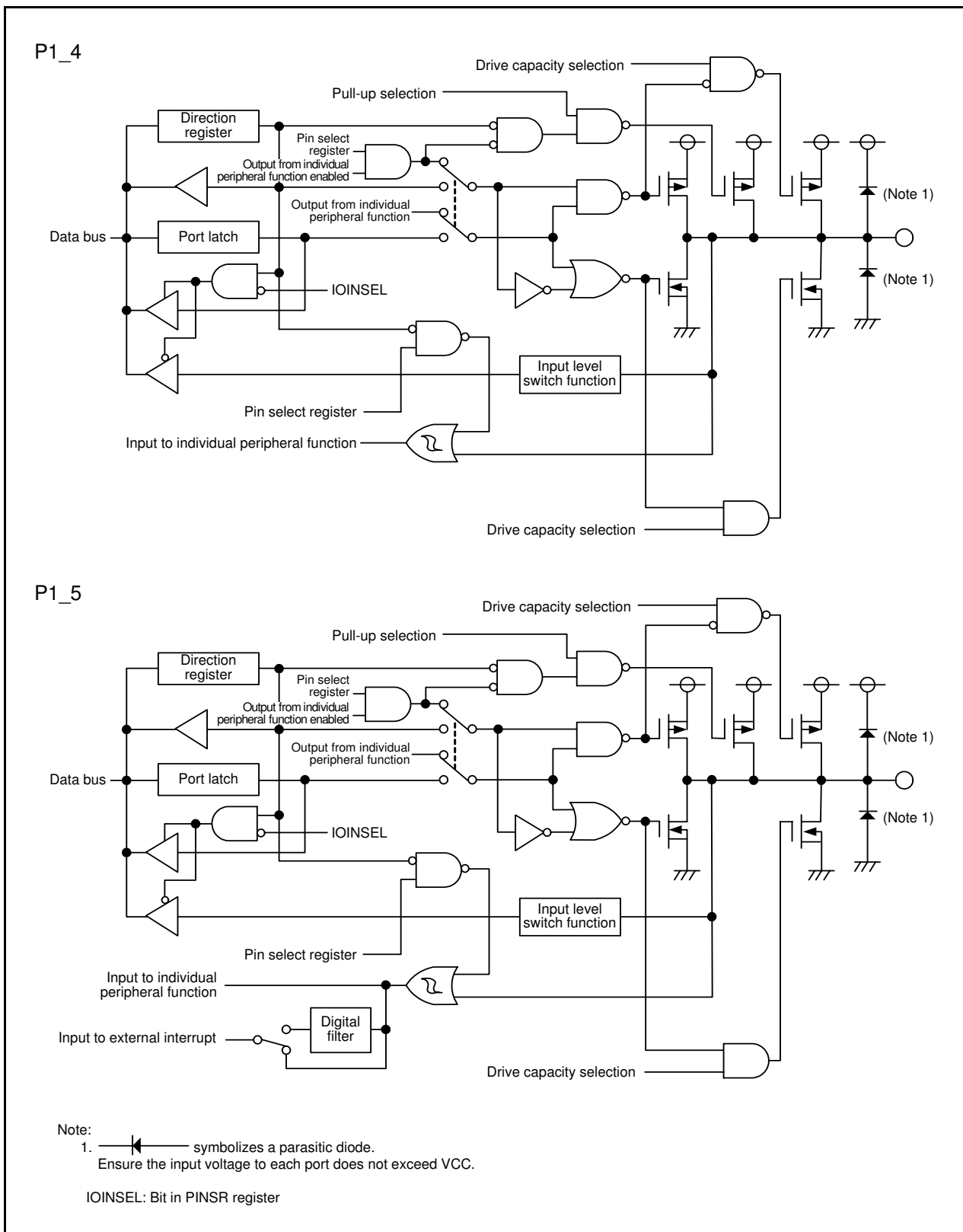


Figure 7.3 Configuration of I/O Ports (3)



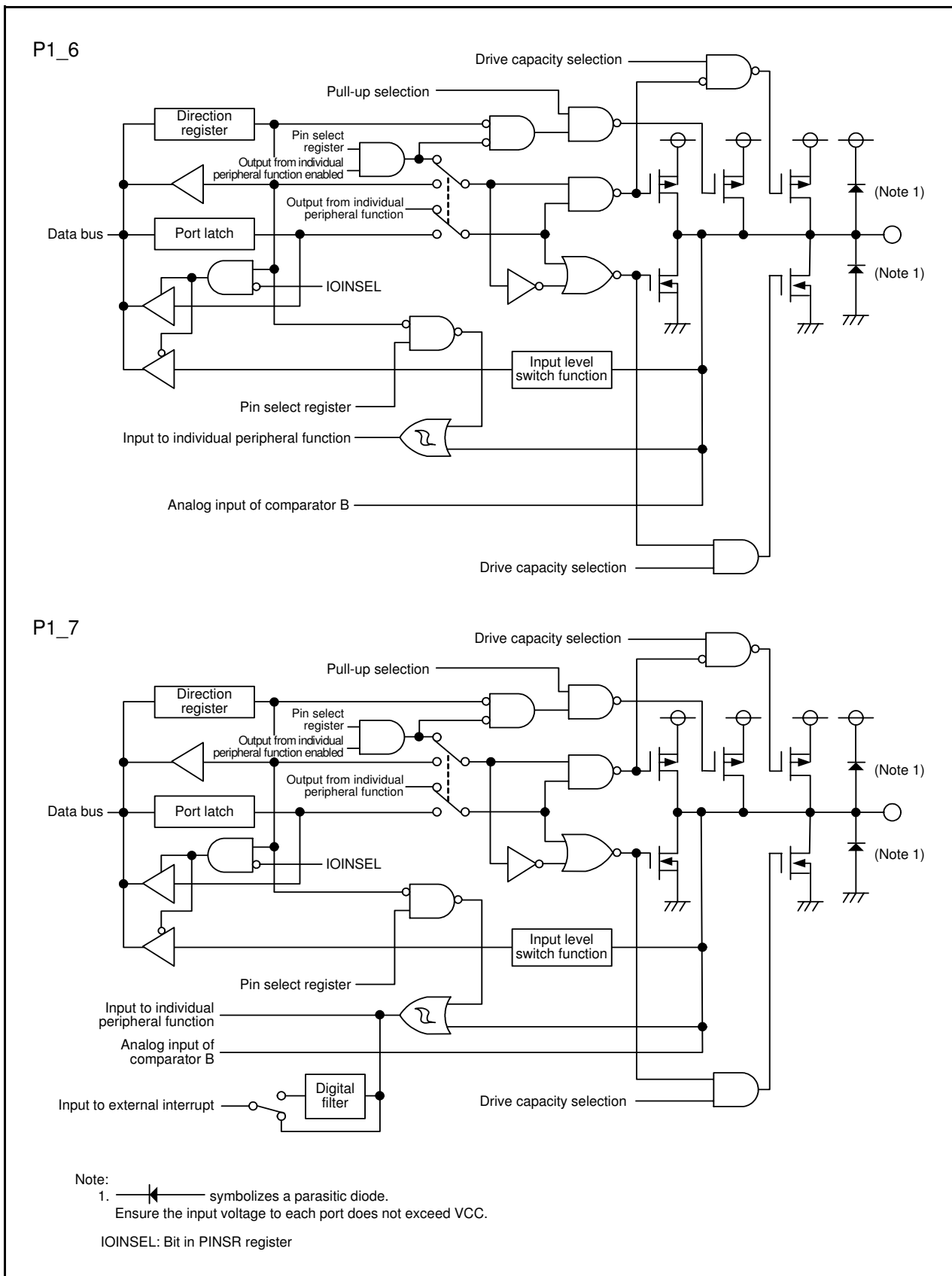


Figure 7.4 Configuration of I/O Ports (4)

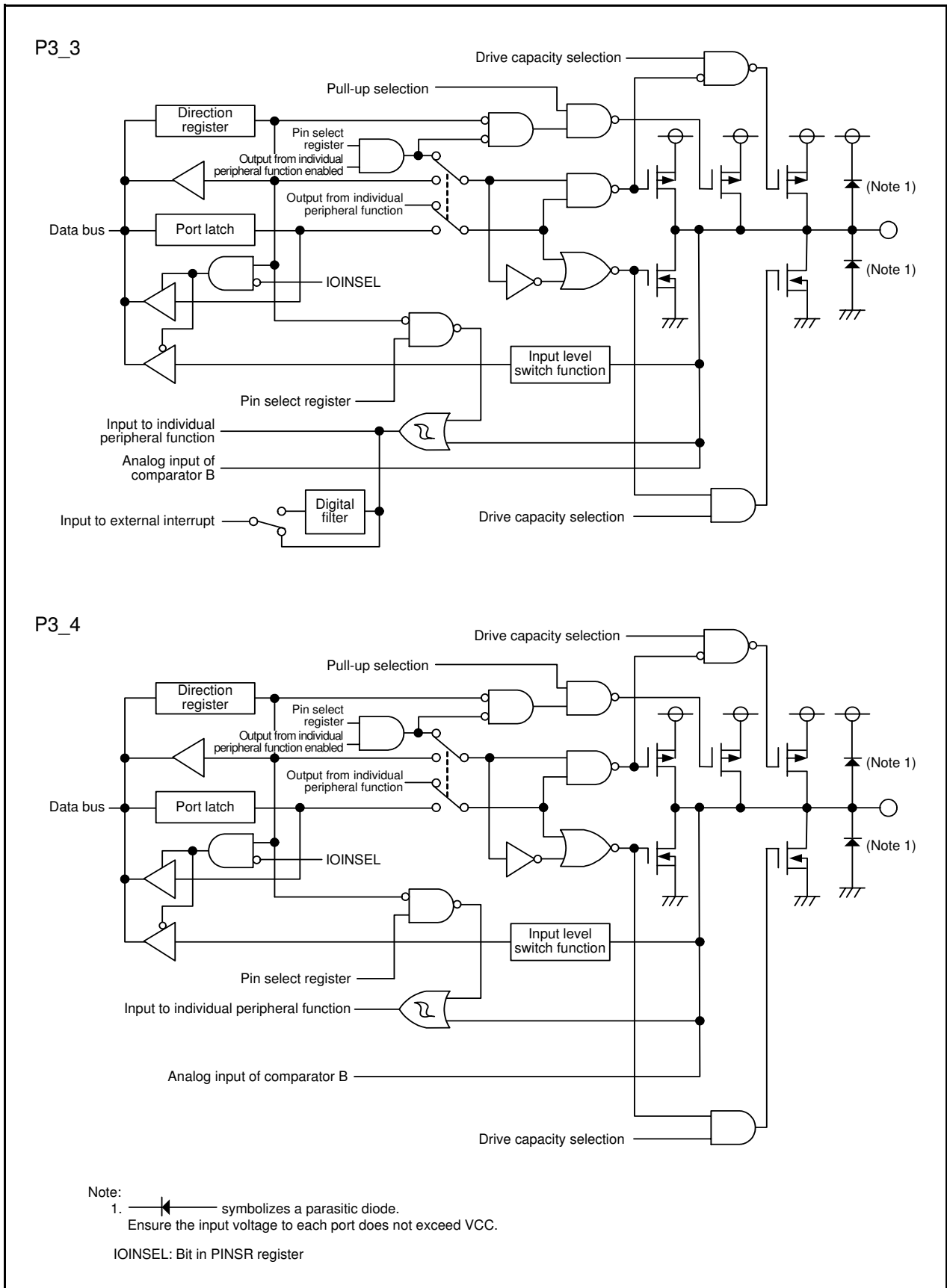


Figure 7.5 Configuration of I/O Ports (5)

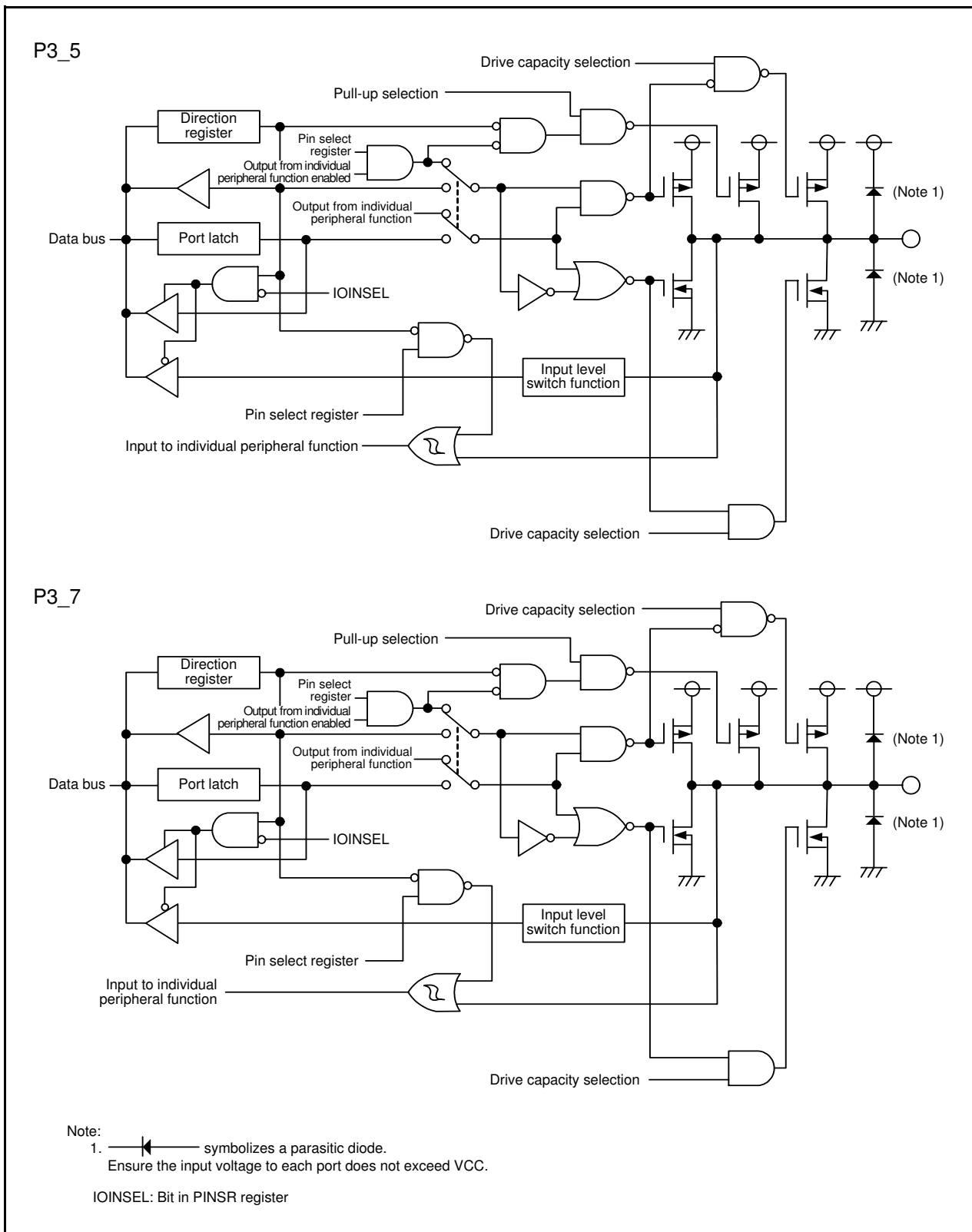
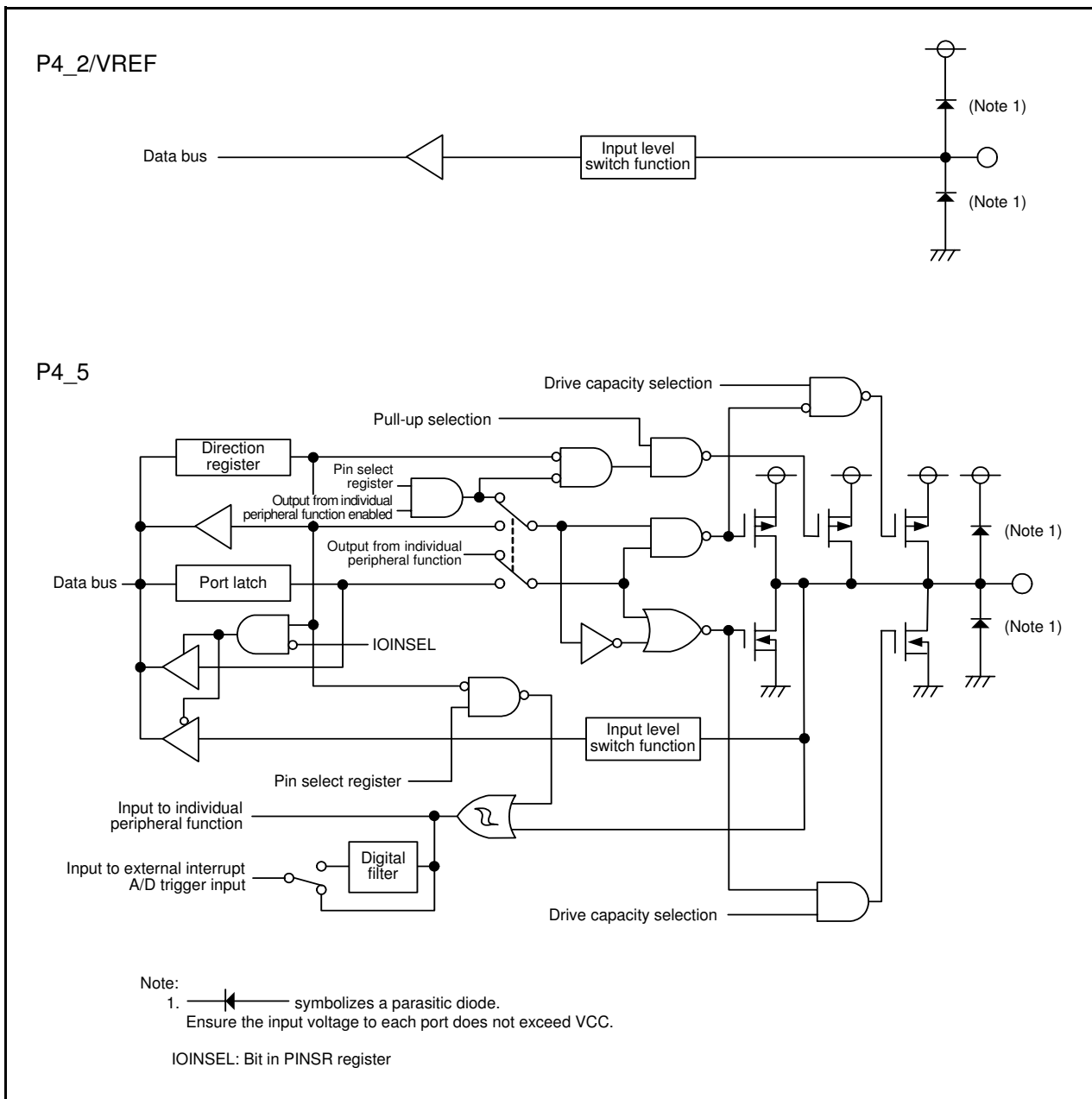


Figure 7.6 Configuration of I/O Ports (6)



**Figure 7.7 Configuration of I/O Ports (7)**

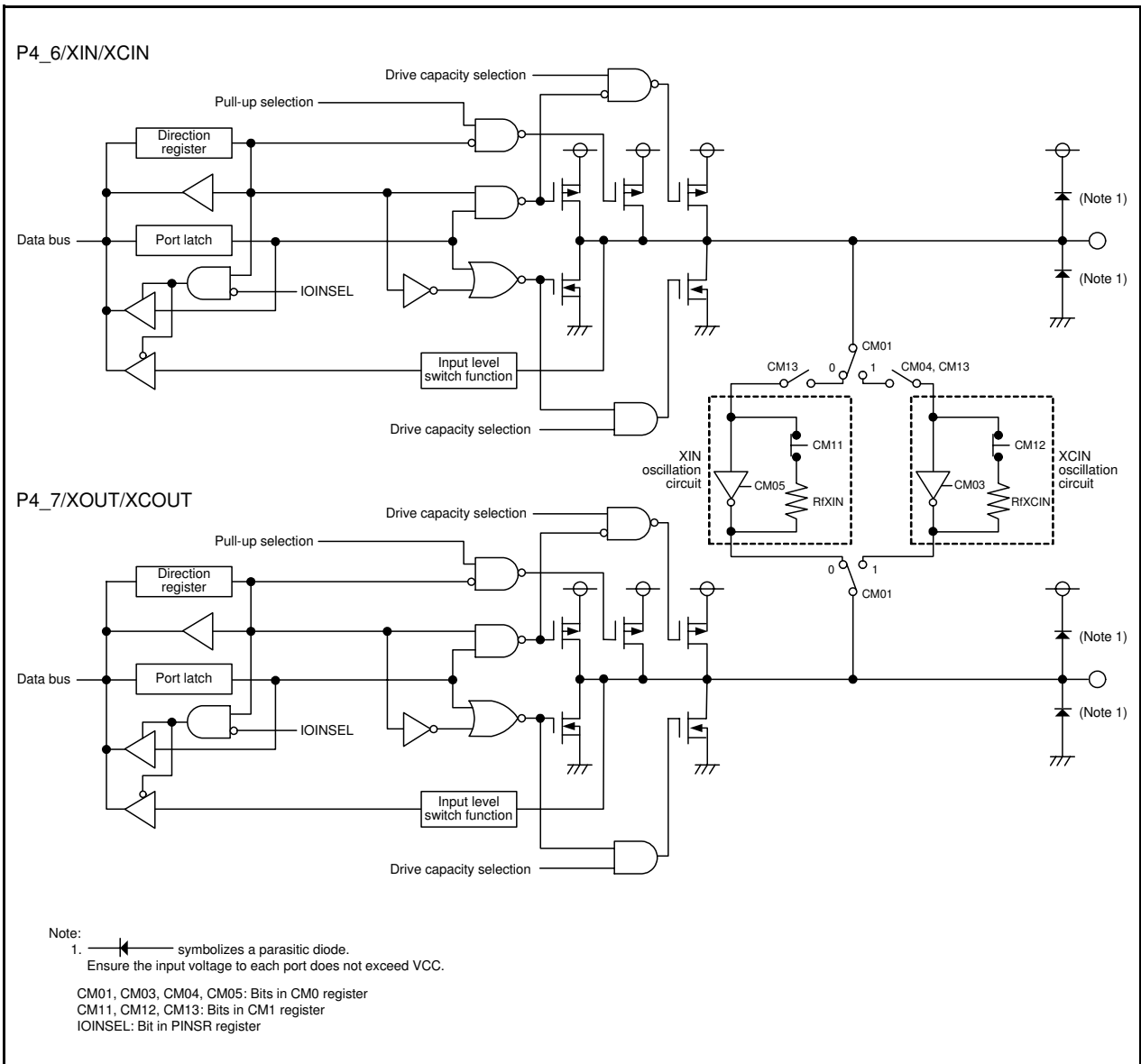


Figure 7.8 Configuration of I/O Ports (8)

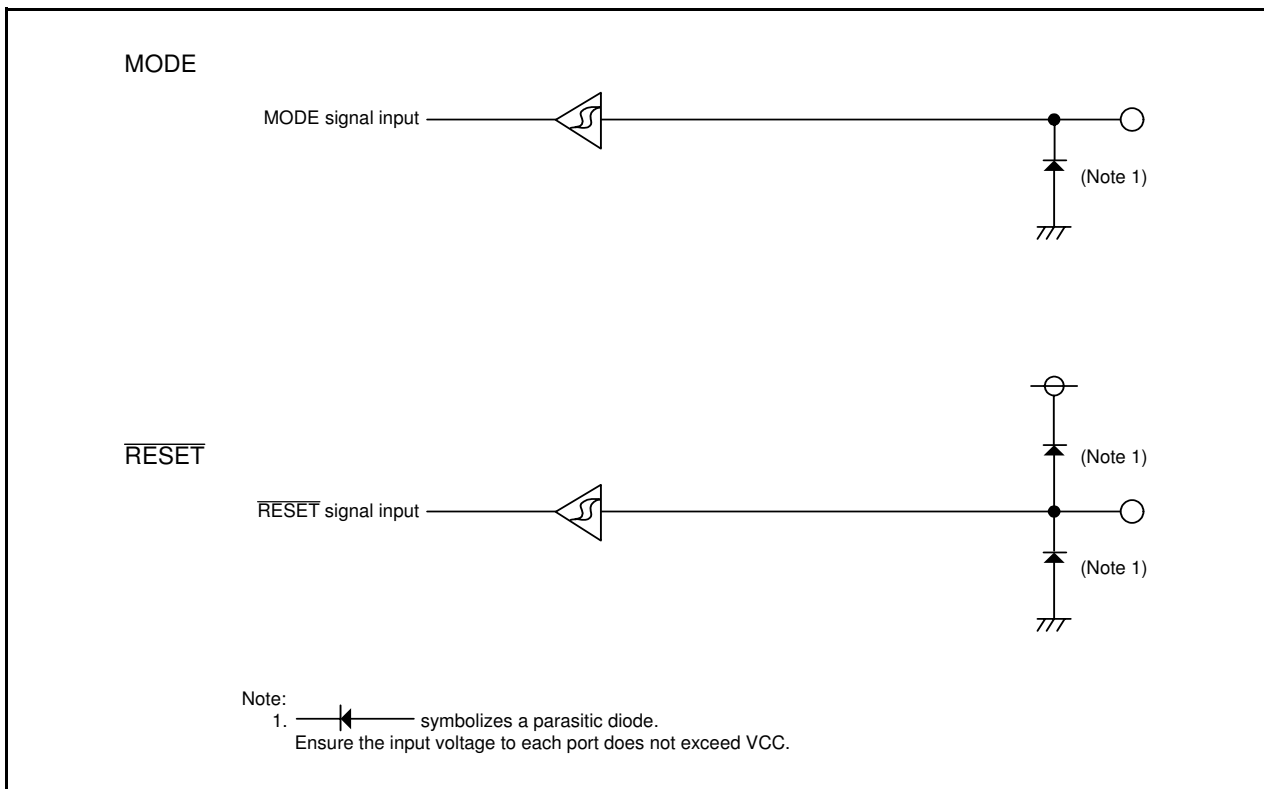


Figure 7.9 Configuration of I/O Pins

## 7.4 Registers

### 7.4.1 Port Pi Direction Register (PDi) (i = 0 to 1, 3 to 4)

Address 00E2h (PD0 <sup>(1)</sup>), 00E3h (PD1), 00E7h (PD3 <sup>(2)</sup>), 00EAh (PD4 <sup>(3)</sup>)

|             |       |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit         | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
| Symbol      | PDi_7 | PDi_6 | PDi_5 | PDi_4 | PDi_3 | PDi_2 | PDi_1 | PDi_0 |
| After Reset | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

| Bit | Symbol | Bit Name                | Function   | R/W |
|-----|--------|-------------------------|--|-----|
| b0  | PDi_0  | Port Pi_0 direction bit | 0: Input mode (functions as an input port)<br>1: Output mode (functions as an output port) | R/W |
| b1  | PDi_1  | Port Pi_1 direction bit |  | R/W |
| b2  | PDi_2  | Port Pi_2 direction bit |  | R/W |
| b3  | PDi_3  | Port Pi_3 direction bit |  | R/W |
| b4  | PDi_4  | Port Pi_4 direction bit |  | R/W |
| b5  | PDi_5  | Port Pi_5 direction bit |  | R/W |
| b6  | PDi_6  | Port Pi_6 direction bit |  | R/W |
| b7  | PDi_7  | Port Pi_7 direction bit |  | R/W |

#### Notes:

- Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).  
Bits PD0\_0 and PD0\_3 to PD0\_5 in the PD0 register are reserved bits. If it is necessary to set bits PD0\_0 and PD0\_3 to PD0\_5, set to 0. When read, the content is 0.
- Bits PD3\_0 to PD3\_2, and PD3\_6 in the PD3 register are reserved bits. If it is necessary to set bits PD3\_0 to PD3\_2 and PD3\_6, set to 0. When read, the content is 0.
- Bits PD4\_0 to PD4\_2 in the PD4 register are unavailable on this MCU. If it is necessary to set bits PD4\_0 to PD4\_2 set to 0. When read, the content is 0. Bits PD4\_3, PD4\_4 are reserved bits. If it is necessary to set bits PD4\_3 and PD4\_4, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

### 7.4.2 Port Pi Register (Pi) (i = 0 to 1, 3 to 4)

Address 00E0h(P0<sup>(1)</sup>), 00E1h(P1), 00E5h(P3<sup>(2)</sup>), 00E8h(P4<sup>(3)</sup>)

|             |      |      |      |      |      |      |      |      |
|-------------|------|------|------|------|------|------|------|------|
| Bit         | b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | Pi_7 | Pi_6 | Pi_5 | Pi_4 | Pi_3 | Pi_2 | Pi_1 | Pi_0 |
| After Reset | X    | X    | X    | X    | X    | X    | X    | X    |

| Bit | Symbol | Bit Name      | Function                     | R/W |
|-----|--------|---------------|------------------------------|-----|
| b0  | Pi_0   | Port Pi_0 bit | 0: "L" level<br>1: "H" level | R/W |
| b1  | Pi_1   | Port Pi_1 bit |                              | R/W |
| b2  | Pi_2   | Port Pi_2 bit |                              | R/W |
| b3  | Pi_3   | Port Pi_3 bit |                              | R/W |
| b4  | Pi_4   | Port Pi_4 bit |                              | R/W |
| b5  | Pi_5   | Port Pi_5 bit |                              | R/W |
| b6  | Pi_6   | Port Pi_6 bit |                              | R/W |
| b7  | Pi_7   | Port Pi_7 bit |                              | R/W |

Notes:

1. Bits P0\_0 and P0\_3 to P0\_5 in the P1 register are reserved bits. If it is necessary to set bits P0\_0 and P0\_3 to P0\_5, set to 0. When read, the content is 0.
2. Bits P3\_0 to P3\_2, and P3\_6 in the P3 register are reserved bits. If it is necessary to set bits P3\_0 to P3\_2 and P3\_6, set to 0. When read, the content is 0.
3. Bits P4\_0 to P4\_1 in the P4 register are unavailable on this MCU. If it is necessary to set bits P4\_0 to P4\_1 set to 0. When read, the content is 0. Bits P4\_3, P4\_4 are reserved bits. If it is necessary to set bits P4\_3 and P4\_4, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

#### Pi\_j Bit (i = 0 to 1, 3 to 4, j = 0 to 7) (Port Pi\_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.



### 7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

|             |    |    |    |    |    |    |            |            |
|-------------|----|----|----|----|----|----|------------|------------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1         | b0         |
| Symbol      | —  | —  | —  | —  | —  | —  | TRAIOSSEL1 | TRAIOSSEL0 |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function  | R/W |
|-----|------------|---|---|-----|
| b0  | TRAIOSSEL0 | TRAI0 pin select bit  | <sup>b1 b0</sup><br>0 0: TRAI0 pin not used<br>0 1: P1_7 assigned<br>1 0: P1_5 assigned<br>1 1: Do not set. | R/W |
| b1  | TRAIOSSEL1 |   |   | R/W |
| b2  | —          | Reserved bits   | Set to 0.   | R/W |
| b3  | —          |   |   |     |
| b4  | —          |   |   |     |
| b5  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b6  | —          |   |   |     |
| b7  | —          |   |   |     |

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.

Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

### 7.4.4 Timer RC Pin Select Register (TRBRCSR)

Address 0181h

|             |    |    |            |            |    |    |    |    |
|-------------|----|----|------------|------------|----|----|----|----|
| Bit         | b7 | b6 | b5         | b4         | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | TRCCLKSEL1 | TRCCLKSEL0 | —  | —  | —  | —  |
| After Reset | 0  | 0  | 0          | 0          | 0  | 0  | 0  | 0  |

| Bit | Symbol     | Bit Name  | Function   | R/W |
|-----|------------|---|--|-----|
| b0  | —          | Reserved bits   | Set to 0.  | R/W |
| b1  | —          |   |  | —   |
| b2  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b3  | —          |   |  |     |
| b4  | TRCCLKSEL0 | TRCCLK pin select bit   | <sup>b5 b4</sup><br>0 0: TRCCLK pin not used<br>0 1: P1_4 assigned<br>1 0: P3_3 assigned<br>1 1: Do not set. | R/W |
| b5  | TRCCLKSEL1 |   |  | R/W |
| b6  | —          | Reserved bit  | Set to 0.  | R/W |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

The TRBRCSR register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set bits TRCCLKSEL0 and TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of bits TRCCLKSEL0 and TRCCLKSEL1 during timer RC operation.

### 7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

| Bit         | b7 | b6 | b5 | b4         | b3 | b2         | b1         | b0         |
|-------------|----|----|----|------------|----|------------|------------|------------|
| Symbol      | —  | —  | —  | TRCIOBSEL0 | —  | TRCIOASEL2 | TRCIOASEL1 | TRCIOASEL0 |
| After Reset | 0  | 0  | 0  | 0          | 0  | 0          | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function   | R/W |
|-----|------------|---|--|-----|
| b0  | TRCIOASEL0 | TRCIOA/TRCTRГ pin select bit  | b2 b1 b0<br>0 0 0: TRCIOA/TRCTRГ pin not used<br>0 0 1: P1_1 assigned<br>0 1 1: P0_1 assigned<br>1 0 0: P0_2 assigned<br>Other than above: Do not set. | R/W |
| b1  | TRCIOASEL1 |   |  | R/W |
| b2  | TRCIOASEL2 |   |  | R/W |
| b3  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | TRCIOBSEL0 | TRCIOB pin select bit   | 0: TRCIOB pin not used<br>1: P1_2 assigned   | R/W |
| b5  | —          | Reserved bits   | Set to 0.  | R/W |
| b6  | —          |   |  |     |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

### 7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

| Bit         | b7 | b6 | b5         | b4         | b3 | b2 | b1         | b0         |
|-------------|----|----|------------|------------|----|----|------------|------------|
| Symbol      | —  | —  | TRCIODSEL1 | TRCIODSEL0 | —  | —  | TRCIOCSEL1 | TRCIOCSEL0 |
| After Reset | 0  | 0  | 0          | 0          | 0  | 0  | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function  | R/W |
|-----|------------|---|---|-----|
| b0  | TRCIOCSEL0 | TRCIOC pin select bit   | b1 b0<br>0 0: TRCIOC pin not used<br>0 1: P1_3 assigned<br>1 0: P3_4 assigned<br>1 1: P0_7 assigned | R/W |
| b1  | TRCIOCSEL1 |   |   | R/W |
| b2  | —          | Reserved bit  | Set to 0.   | R/W |
| b3  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | TRCIODSEL0 | TRCIOD pin select bit   | b5 b4<br>0 0: TRCIOD pin not used<br>0 1: P1_0 assigned<br>1 0: P3_5 assigned<br>1 1: P0_6 assigned | R/W |
| b5  | TRCIODSEL1 |   |   | R/W |
| b6  | —          | Reserved bit  | Set to 0.   | R/W |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

### 7.4.7 UART0 Pin Select Register (U0SR)

Address 0188h

|             |    |    |    |          |    |          |    |          |
|-------------|----|----|----|----------|----|----------|----|----------|
| Bit         | b7 | b6 | b5 | b4       | b3 | b2       | b1 | b0       |
| Symbol      | —  | —  | —  | CLK0SEL0 | —  | RXD0SEL0 | —  | TXD0SEL0 |
| After Reset | 0  | 0  | 0  | 0        | 0  | 0        | 0  | 0        |

| Bit | Symbol   | Bit Name  | Function                                 | R/W |
|-----|----------|---|--|-----|
| b0  | TXD0SEL0 | TXD0 pin select bit   | 0: TXD0 pin not used<br>1: P1_4 assigned | R/W |
| b1  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b2  | RXD0SEL0 | RXD0 pin select bit   | 0: RXD0 pin not used<br>1: P1_5 assigned | R/W |
| b3  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | CLK0SEL0 | CLK0 pin select bit   | 0: CLK0 pin not used<br>1: P1_6 assigned | R/W |
| b5  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b6  | —        |   |  |     |
| b7  | —        |   |  |     |

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.

Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

### 7.4.8 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

| Bit         | b7 | b6 | b5       | b4       | b3 | b2 | b1       | b0       |
|-------------|----|----|----------|----------|----|----|----------|----------|
| Symbol      | —  | —  | RXD2SEL1 | RXD2SEL0 | —  | —  | TXD2SEL1 | TXD2SEL0 |
| After Reset | 0  | 0  | 0        | 0        | 0  | 0  | 0        | 0        |

| Bit | Symbol   | Bit Name  | Function   | R/W |
|-----|----------|---|--|-----|
| b0  | TXD2SEL0 | TXD2/SDA2 pin select bit  | b1 b0<br>0 0: TXD2/SDA2 pin not used<br>0 1: P3_7 assigned<br>1 0: P3_4 assigned<br>1 1: Do not set.   | R/W |
| b1  | TXD2SEL1 |   |  | R/W |
| b2  | —        | Reserved bit  | Set to 0.  | R/W |
| b3  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | RXD2SEL0 | RXD2/SCL2 pin select bit  | b5 b4<br>0 0: RXD2/SCL2 pin not used<br>0 1: P3_4 assigned<br>1 0: P3_7 assigned<br>1 1: P4_5 assigned | R/W |
| b5  | RXD2SEL1 |   |  | R/W |
| b6  | —        | Reserved bit  | Set to 0.  | R/W |
| b7  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.

Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

### 7.4.9 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

| Bit         | b7 | b6 | b5 | b4       | b3 | b2 | b1 | b0       |
|-------------|----|----|----|----------|----|----|----|----------|
| Symbol      | —  | —  | —  | CTS2SEL0 | —  | —  | —  | CLK2SEL0 |
| After Reset | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0        |

| Bit | Symbol   | Bit Name  | Function                                      | R/W |
|-----|----------|---|---|-----|
| b0  | CLK2SEL0 | CLK2 pin select bit   | 0: CLK2 pin not used<br>1: P3_5 assigned      | R/W |
| b1  | —        | Reserved bit  | Set to 0.                                     | R/W |
| b2  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b3  | —        |   |   |     |
| b4  | CTS2SEL0 | CTS2/RTS2 pin select bit  | 0: CTS2/RTS2 pin not used<br>1: P3_3 assigned | R/W |
| b5  | —        | Reserved bit  | Set to 0.                                     | R/W |
| b6  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b7  | —        |   |   |     |

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.

Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

### 7.4.10 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

|             |    |    |    |    |    |    |          |    |
|-------------|----|----|----|----|----|----|----------|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1       | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | INT1SEL0 | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  |

| Bit | Symbol   | Bit Name  | Function                             | R/W |
|-----|----------|---|--------------------------------------|-----|
| b0  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                      | —   |
| b1  | INT1SEL0 | INT1 pin select bit   | 0: P1_7 assigned<br>1: P1_5 assigned | R/W |
| b2  | —        | Reserved bits   | Set to 0.                            | R/W |
| b3  | —        |   |                                      |     |
| b4  | —        |   |                                      |     |
| b5  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                      | —   |
| b6  | —        | Reserved bits   | Set to 0.                            | R/W |
| b7  | —        |   |                                      |     |

The INTSR register selects which pin is assigned to the  $\overline{\text{INT1}}$  input. To use  $\overline{\text{INT1}}$ , set this register. Set the INTSR register before setting the  $\overline{\text{INT1}}$  associated registers. Also, do not change the setting values in this register during  $\overline{\text{INT1}}$  operation.

### 7.4.11 I/O Function Pin Select Register (PINSR)

Address 018Fh

|             |    |    |    |    |         |    |    |    |
|-------------|----|----|----|----|---------|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3      | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | IOINSEL | —  | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 0       | 0  | 0  | 0  |

| Bit | Symbol  | Bit Name  | Function  | R/W |
|-----|---------|---|---|-----|
| b0  | —       | Reserved bits   | Set to 0.   | R/W |
| b1  | —       |   |   |     |
| b2  | —       | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b3  | IOINSEL | I/O port input function select bit  | 0: The I/O port input function depends on the PDi (i = 0, 1, 3 to 4) register.<br>When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read.<br>When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read.<br>1: The I/O port input function reads the pin input level regardless of the PDi register. | R/W |
| b4  | —       | Reserved bits   | Set to 0.   | R/W |
| b5  | —       |   |   |     |
| b6  | —       |   |   |     |
| b7  | —       |   |   |     |

#### IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi\_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3 to 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports except P4\_2.

**Table 7.4 I/O Port Values Read by Using IOINSEL Bit**

| PDi_j bit in PDi register | 0 (input mode) |                 | 1 (output mode)  |                 |   |
|---------------------------|----------------|-----------------|------------------|-----------------|---|
|                           | IOINSEL bit    | 0               | 1                | 0               | 1 |
| I/O port values read      |                | Pin input level | Port latch value | Pin input level |   |

### 7.4.12 Pull-Up Control Register 0 (PUR0)

Address 01E0h

| Bit         | b7   | b6   | b5 | b4 | b3   | b2   | b1   | b0   |
|-------------|------|------|----|----|------|------|------|------|
| Symbol      | PU07 | PU06 | —  | —  | PU03 | PU02 | PU01 | PU00 |
| After Reset | 0    | 0    | 0  | 0  | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                 | Function  | R/W |
|-----|--------|--------------------------|---|-----|
| b0  | PU00   | P0_1, P0_2 pull-up       | 0: Not pulled up<br>1: Pulled up <sup>(1)</sup> | R/W |
| b1  | PU01   | P0_6, P0_7 pull-up       |   | R/W |
| b2  | PU02   | P1_0 to P1_3 pull-up     |   | R/W |
| b3  | PU03   | P1_4 to P1_7 pull-up     |   | R/W |
| b4  | —      | Reserved bits            | Set to 0.                                       | R/W |
| b5  | —      |                          |   |     |
| b6  | PU06   | P3_3 pull-up             | 0: Not pulled up<br>1: Pulled up <sup>(1)</sup> | R/W |
| b7  | PU07   | P3_4, P3_5, P3_7 pull-up |   | R/W |

Note:

- When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For pins used as input, the setting values in the PUR0 register are valid.

### 7.4.13 Pull-Up Control Register 1 (PUR1)

Address 01E1h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1   | b0 |
|-------------|----|----|----|----|----|----|------|----|
| Symbol      | —  | —  | —  | —  | —  | —  | PU11 | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0    | 0  |

| Bit | Symbol | Bit Name             | Function  | R/W       |
|-----|--------|----------------------|---|-----------|
| b0  | —      | Reserved bit         | Set to 0.   | R/W       |
| b1  | PU11   | P4_5 to P4_7 pull-up | 0: Not pulled up<br>1: Pulled up <sup>(1)</sup>                                   | R/W       |
| b2  | —      | Reserved bits        |   | Set to 0. |
| b3  | —      |                      |   |           |
| b4  | —      |                      |   |           |
| b5  | —      |                      |   |           |
| b6  | —      |                      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |           |
| b7  | —      |                      |   |           |

Note:

- When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For pins used as input, the setting values in the PUR1 register are valid.

### 7.4.14 Port P1 Drive Capacity Control Register (P1DRR)

Address 01F0h

|             |        |        |        |        |        |        |        |        |
|-------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit         | b7     | b6     | b5     | b4     | b3     | b2     | b1     | b0     |
| Symbol      | P1DRR7 | P1DRR6 | P1DRR5 | P1DRR4 | P1DRR3 | P1DRR2 | P1DRR1 | P1DRR0 |
| After Reset | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

| Bit | Symbol | Bit Name            | Function                         | R/W |
|-----|--------|---------------------|----------------------------------|-----|
| b0  | P1DRR0 | P1_0 drive capacity | 0: Low<br>1: High <sup>(1)</sup> | R/W |
| b1  | P1DRR1 | P1_1 drive capacity |                                  | R/W |
| b2  | P1DRR2 | P1_2 drive capacity |                                  | R/W |
| b3  | P1DRR3 | P1_3 drive capacity |                                  | R/W |
| b4  | P1DRR4 | P1_4 drive capacity |                                  | R/W |
| b5  | P1DRR5 | P1_5 drive capacity |                                  | R/W |
| b6  | P1DRR6 | P1_6 drive capacity |                                  | R/W |
| b7  | P1DRR7 | P1_7 drive capacity |                                  | R/W |

Note:

- Both "H" and "L" output are set to high drive capacity.

The P1DRR register selects whether the drive capacity of the P1 output transistor is set to low or high.

The P1DRR<sub>i</sub> bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.

For pins used as output, the setting values in the P1DRR register are valid.



### 7.4.15 Drive Capacity Control Register 0 (DRR0)

Address 01F2h

| Bit         | b7    | b6    | b5 | b4 | b3 | b2 | b1    | b0    |
|-------------|-------|-------|----|----|----|----|-------|-------|
| Symbol      | DRR07 | DRR06 | —  | —  | —  | —  | DRR01 | DRR00 |
| After Reset | 0     | 0     | 0  | 0  | 0  | 0  | 0     | 0     |

| Bit | Symbol | Bit Name  | Function               | R/W |
|-----|--------|---|------------------------|-----|
| b0  | DRR00  | P0_1, P0_2 drive capacity   | 0: Low                 | R/W |
| b1  | DRR01  | P0_6, P0_7 drive capacity   | 1: High <sup>(1)</sup> | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                        | —   |
| b3  | —      |   |                        |     |
| b4  | —      |   |                        |     |
| b5  | —      |   |                        |     |
| b6  | DRR06  | P3_3 drive capacity   | 0: Low                 | R/W |
| b7  | DRR07  | P3_4, P3_5, P3_7 drive capacity   | 1: High <sup>(1)</sup> | R/W |

Note:

- Both "H" and "L" output are set to high drive capacity.

For pins used as output, the setting values in the DRR0 register are valid.

#### DRR00 Bit (P0\_1, P0\_2 drive capacity)

The DRR00 bit selects whether the drive capacity of the P0\_1, P0\_2 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

#### DRR01 Bit (P0\_6, P0\_7 drive capacity)

The DRR01 bit selects whether the drive capacity of the P0\_6, P0\_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

#### DRR06 Bit (P3\_3 drive capacity)

The DRR06 bit selects whether the drive capacity of the P3\_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for one pin.

#### DRR07 Bit (P3\_4, P3\_5, P3\_7 drive capacity)

The DRR07 bit selects whether the drive capacity of the P3\_4, P3\_5, P3\_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

### 7.4.16 Drive Capacity Control Register 1 (DRR1)

Address 01F3h

|             |    |    |    |    |    |    |       |    |
|-------------|----|----|----|----|----|----|-------|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1    | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | DRR11 | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0  |

| Bit | Symbol | Bit Name  | Function                         | R/W |
|-----|--------|---|----------------------------------|-----|
| b0  | —      | Reserved bit  | Set to 0.                        | R/W |
| b1  | DRR11  | P4_5 to P4_7 drive capacity   | 0: Low<br>1: High <sup>(1)</sup> | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                  | —   |
| b3  | —      | Reserved bits   | Set to 0.                        | R/W |
| b4  | —      |   |                                  |     |
| b5  | —      |   |                                  |     |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                  | —   |
| b7  | —      |   |                                  |     |

Note:

- Both "H" and "L" output are set to high drive capacity.

For pins used as output, the setting values in the DRR1 register are valid.

#### DRR11 Bit (P4\_5 to P4\_7 drive capacity)

The DRR11 bit selects whether the drive capacity of the P4\_5 to P4\_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

### 7.4.17 Input Threshold Control Register 0 (VLT0)

Address 01F5h

| Bit         | b7    | b6    | b5 | b4 | b3    | b2    | b1    | b0    |
|-------------|-------|-------|----|----|-------|-------|-------|-------|
| Symbol      | VLT07 | VLT06 | —  | —  | VLT03 | VLT02 | VLT01 | VLT00 |
| After Reset | 0     | 0     | 0  | 0  | 0     | 0     | 0     | 0     |

| Bit | Symbol | Bit Name                                      | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | VLT00  | P0_1, P0_2, P0_6, P0_7 input level select bit | <sup>b1 b0</sup><br>0 0: 0.50 × VCC<br>0 1: 0.35 × VCC<br>1 0: 0.70 × VCC<br>1 1: Do not set. | R/W |
| b1  | VLT01  |   |   | R/W |
| b2  | VLT02  | P1 input level select bit                     | <sup>b3 b2</sup><br>0 0: 0.50 × VCC<br>0 1: 0.35 × VCC<br>1 0: 0.70 × VCC<br>1 1: Do not set. | R/W |
| b3  | VLT03  |   |   | R/W |
| b4  | —      | Reserved bits                                 | Set to 0.   | R/W |
| b5  | —      |   |   | R/W |
| b6  | VLT06  | P3_3 to P3_5, P3_7 input level select bit     | <sup>b7 b6</sup><br>0 0: 0.50 × VCC<br>0 1: 0.35 × VCC<br>1 0: 0.70 × VCC<br>1 1: Do not set. | R/W |
| b7  | VLT07  |   |   | R/W |

The VLT0 register selects the voltage level of the input threshold values for ports P0\_1, P0\_2, P0\_6, P0\_7, P1, P3\_3 to P3\_5, and P3\_7. Bits VLT00 to VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

### 7.4.18 Input Threshold Control Register 1 (VLT1)

Address 01F6h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1    | b0    |
|-------------|----|----|----|----|----|----|-------|-------|
| Symbol      | —  | —  | —  | —  | —  | —  | VLT11 | VLT10 |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0     |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | VLT10  | P4_2, P4_5 to P4_7 input level select bit                                 | <sup>b1 b0</sup><br>0 0: 0.50 × VCC<br>0 1: 0.35 × VCC<br>1 0: 0.70 × VCC<br>1 1: Do not set. | R/W |
| b1  | VLT11  |   |   | R/W |
| b2  | —      | Reserved bits   | Set to 0.   | R/W |
| b3  | —      |   |   | R/W |
| b4  | —      |   |   | R/W |
| b5  | —      |   |   | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b7  | —      |   |   | —   |

The VLT1 register selects the voltage level of the input threshold values for ports P4\_2 and P4\_5 to P4\_7. Bits VLT10 to VLT15 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

## 7.5 Port Settings

Tables 7.5 to 7.29 list the port settings.

**Table 7.5 Port P0\_1/AN6/TRCIOA/TRCTRG**

| Register      | PD0   | ADINSEL |   |   |        |   | TRCPSR0         |   |   | Timer RC Setting                              | Function                                 |
|---------------|-------|---------|---|---|--------|---|-----------------|---|---|---|--|
| Bit           | PD0_1 | CH      |   |   | ADGSEL |   | TRCIOASEL       |   |   | —   |  |
|               |       | 2       | 1 | 0 | 1      | 0 | 2               | 1 | 0 |   |  |
| Setting Value | 0     | X       | X | X | X      | X | Other than 011b |   |   | X   | Input port <sup>(1)</sup>                |
|               | 1     | X       | X | X | X      | X | Other than 011b |   |   | X   | Output port <sup>(2)</sup>               |
|               | 0     | 1       | 1 | 0 | 0      | 0 | Other than 011b |   |   | X   | A/D converter input (AN6) <sup>(1)</sup> |
|               | 0     | X       | X | X | X      | X | 0               | 1 | 1 | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> | TRCIOA input <sup>(1)</sup>              |
|               | X     | X       | X | X | X      | X | 0               | 1 | 1 | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> | TRCIOA output <sup>(2)</sup>             |

X: 0 or 1

Notes:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.

**Table 7.6 Port P0\_2/AN5/TRCIOA/TRCTRG**

| Register      | PD0   | ADINSEL |   |   |        |   | TRCPSR0         |   |   | Timer RC Setting                              | Function                                 |
|---------------|-------|---------|---|---|--------|---|-----------------|---|---|---|--|
| Bit           | PD0_2 | CH      |   |   | ADGSEL |   | TRCIOASEL       |   |   | —   |  |
|               |       | 2       | 1 | 0 | 1      | 0 | 2               | 1 | 0 |   |  |
| Setting Value | 0     | X       | X | X | X      | X | Other than 100b |   |   | X   | Input port <sup>(1)</sup>                |
|               | 1     | X       | X | X | X      | X | Other than 100b |   |   | X   | Output port <sup>(2)</sup>               |
|               | 0     | 1       | 0 | 1 | 0      | 0 | Other than 100b |   |   | X   | A/D converter input (AN5) <sup>(1)</sup> |
|               | 0     | X       | X | X | X      | X | 1               | 0 | 0 | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> | TRCIOA input <sup>(1)</sup>              |
|               | X     | X       | X | X | X      | X | 1               | 0 | 0 | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> | TRCIOA output <sup>(2)</sup>             |

X: 0 or 1

Notes:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.

**Table 7.7 Port P0\_6/AN1/TRCIOD**

| Register      | PD0   | ADINSEL |   |   |        |   | TRCPSR1        |   | Timer RC Setting                              | Function                                 |
|---------------|-------|---------|---|---|--------|---|----------------|---|---|--|
| Bit           | PD0_6 | CH      |   |   | ADGSEL |   | TRCIODSEL      |   | —   |  |
|               |       | 2       | 1 | 0 | 1      | 0 | 1              | 0 |   |  |
| Setting Value | 0     | X       | X | X | X      | X | Other than 11b |   | X   | Input port <sup>(1)</sup>                |
|               | 1     | X       | X | X | X      | X | Other than 11b |   | X   | Output port <sup>(2)</sup>               |
|               | 0     | 0       | 0 | 1 | 0      | 0 | Other than 11b |   | X   | A/D converter input (AN1) <sup>(1)</sup> |
|               | 0     | X       | X | X | X      | X | 1              | 1 | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> | TRCIOD input <sup>(1)</sup>              |
|               | X     | X       | X | X | X      | X | 1              | 1 | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> | TRCIOD output <sup>(2)</sup>             |

X: 0 or 1

Notes:

1. Pulled up by setting the PU01 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR01 bit in the DRR0 register to 1.

**Table 7.8 Port P0\_7/AN0/TRCIOC**

| Register      | PD0   | ADINSEL |   |   |        |   | TRCPSR1        |   | Timer RC Setting                              |  | Function                                 |
|---------------|-------|---------|---|---|--------|---|----------------|---|---|--|--|
| Bit           | PD0_7 | CH      |   |   | ADGSEL |   | TRCIOCSEL      |   | —   |  |  |
|               |       | 2       | 1 | 0 | 1      | 0 | 1              | 0 |   |  |  |
| Setting Value | 0     | X       | X | X | X      | X | Other than 11b |   | X   |  | Input port <sup>(1)</sup>                |
|               | 1     | X       | X | X | X      | X | Other than 11b |   | X   |  | Output port <sup>(2)</sup>               |
|               | 0     | 0       | 0 | 0 | 0      | 0 | Other than 11b |   | X   |  | A/D converter input (AN0) <sup>(1)</sup> |
|               | 0     | X       | X | X | X      | X | 1              | 1 | Refer to <b>Table 7.28 TRCIOC Pin Setting</b> |  | TRCIOC input <sup>(1)</sup>              |
|               | X     | X       | X | X | X      | X | 1              | 1 | Refer to <b>Table 7.28 TRCIOC Pin Setting</b> |  | TRCIOC output <sup>(2)</sup>             |

X: 0 or 1

Notes:

1. Pulled up by setting the PU01 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR01 bit in the DRR0 register to 1.

**Table 7.9 Port P1\_0/KI0/AN8/TRCIOD**

| Register      | PD1   | KIEN  | ADINSEL |   |   |        |   | TRCPSR1        |                | Timer RC Setting |   | Function                                     |  |
|---------------|-------|-------|---------|---|---|--------|---|----------------|----------------|------------------|---|--|--|
| Bit           | PD1_0 | KI0EN | CH      |   |   | ADGSEL |   | TRCIODSEL      |                | —                |   |  |  |
|               |       |       | 2       | 1 | 0 | 1      | 0 | 1              | 0              |                  |   |  |  |
| Setting Value | 0     | X     | X       | X | X | X      | X | Other than 01b |                | X                |   | Input port <sup>(1)</sup>                    |  |
|               | 1     | X     | X       | X | X | X      | X | Other than 01b |                | X                |   | Output port <sup>(2)</sup>                   |  |
|               | 0     | 1     | X       | X | X | X      | X | Other than 01b |                | X                |   | $\overline{\text{KI0}}$ input <sup>(1)</sup> |  |
|               | 0     | 0     | 0       | 0 | 0 | 0      | 0 | 1              | Other than 01b |                  | X   |  | A/D converter input (AN8) <sup>(1)</sup> |
|               | 0     | X     | X       | X | X | X      | X | X              | 0              | 1                | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> |  | TRCIOD input <sup>(1)</sup>              |
|               | X     | X     | X       | X | X | X      | X | X              | 0              | 1                | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> |  | TRCIOD output <sup>(2)</sup>             |

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR0 bit in the P1DRR register to 1.

**Table 7.10 Port P1\_1/KI1/AN9/TRCIOA/TRCTR**

| Register      | PD1   | KIEN  | ADINSEL |   |   |        |   | TRCPSR0         |   |   | Timer RC Setting |   | Function                                     |                              |
|---------------|-------|-------|---------|---|---|--------|---|-----------------|---|---|------------------|---|--|------------------------------|
| Bit           | PD1_1 | KI1EN | CH      |   |   | ADGSEL |   | TRCIOASEL       |   |   | —                |   |  |                              |
|               |       |       | 2       | 1 | 0 | 1      | 0 | 2               | 1 | 0 |                  |   |  |                              |
| Setting Value | 0     | X     | X       | X | X | X      | X | Other than 001b |   |   | X                |   | Input port <sup>(1)</sup>                    |                              |
|               | 1     | X     | X       | X | X | X      | X | Other than 001b |   |   | X                |   | Output port <sup>(2)</sup>                   |                              |
|               | 0     | 1     | X       | X | X | X      | X | Other than 001b |   |   | X                |   | $\overline{\text{KI1}}$ input <sup>(1)</sup> |                              |
|               | 0     | 0     | 0       | 0 | 1 | 0      | 1 | Other than 001b |   |   | X                |   | A/D converter input (AN9) <sup>(1)</sup>     |                              |
|               | 0     | X     | X       | X | X | X      | X | X               | 0 | 0 | 1                | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> |  | TRCIOA input <sup>(1)</sup>  |
|               | X     | X     | X       | X | X | X      | X | X               | 0 | 0 | 1                | Refer to <b>Table 7.26 TRCIOA Pin Setting</b> |  | TRCIOA output <sup>(2)</sup> |

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR1 bit in the P1DRR register to 1.

**Table 7.11 Port P1\_2/KI2/AN10/TRCIOB**

| Register      | PD1   | KIEN  | ADINSEL |   |   |        |   | TRCPSR0    | Timer RC Setting                              | Function                                     |                              |
|---------------|-------|-------|---------|---|---|--------|---|------------|---|--|------------------------------|
| Bit           | PD1_2 | KI2EN | CH      |   |   | ADGSEL |   | TRCIOBSEL0 |   |  |                              |
|               |       |       | 2       | 1 | 0 | 1      | 0 | —          |   |  |                              |
| Setting Value | 0     | X     | X       | X | X | X      | X | 0          | X   | Input port <sup>(1)</sup>                    |                              |
|               | 1     | X     | X       | X | X | X      | X | 0          | X   | Output port <sup>(2)</sup>                   |                              |
|               | 0     | 1     | X       | X | X | X      | X | 0          | X   | $\overline{\text{KI2}}$ input <sup>(1)</sup> |                              |
|               | 0     | 0     | 0       | 1 | 0 | 0      | 1 | 0          | X   | A/D converter input (AN10) <sup>(1)</sup>    |                              |
|               | 0     | X     | X       | X | X | X      | X | 1          | Refer to <b>Table 7.27 TRCIOB Pin Setting</b> |  | TRCIOB input <sup>(1)</sup>  |
|               | X     | X     | X       | X | X | X      | X | 1          | Refer to <b>Table 7.27 TRCIOB Pin Setting</b> |  | TRCIOB output <sup>(2)</sup> |

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR2 bit in the P1DRR register to 1.

**Table 7.12 Port P1\_3/KI3/AN11/TRCIOC**

| Register      | PD1   | KIEN  | ADINSEL |   |   |        |   | TRCPSR1   | Timer RB Setting | Timer RC Setting                 | Function                                      |  |
|---------------|-------|-------|---------|---|---|--------|---|-----------|------------------|----------------------------------|---|--|
| Bit           | PD1_3 | KI3EN | CH      |   |   | ADGSEL |   | TRCIOCSEL |                  |                                  |   |  |
|               |       |       | 2       | 1 | 0 | 1      | 0 | 1         | 0                | —                                |   | —  |
| Setting Value | 0     | X     | X       | X | X | X      | X | X         | Other than 01b   | X                                | X   | Input port <sup>(1)</sup>                    |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |
|               | 1     | X     | X       | X | X | X      | X | X         | Other than 01b   | X                                | X   | Output port <sup>(2)</sup>                   |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |
|               | 0     | 1     | X       | X | X | X      | X | X         | Other than 01b   | X                                | X   | $\overline{\text{KI3}}$ input <sup>(1)</sup> |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |
|               | 0     | 0     | 0       | 0 | 1 | 1      | 0 | 1         | Other than 01b   | X                                | X   | A/D converter input (AN11) <sup>(1)</sup>    |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |
| X             | X     | X     | X       | X | X | X      | X | X         | X                | X                                | TRBO output <sup>(2)</sup>                    |  |
| 0             | X     | X     | X       | X | X | X      | X | 0         | 1                | X                                | Refer to <b>Table 7.28 TRCIOC Pin Setting</b> | TRCIOC input <sup>(1)</sup>                  |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |
| X             | X     | X     | X       | X | X | X      | X | 0         | 1                | X                                | Refer to <b>Table 7.28 TRCIOC Pin Setting</b> | TRCIOC output <sup>(2)</sup>                 |
|               |       |       |         |   |   |        |   |           |                  | Other than TRBO usage conditions |   |  |

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR3 bit in the P1DRR register to 1.

**Table 7.13 Port P1\_4/TXD0/TRCCLK**

| Register      | PD1   | U0SR     | U0MR |   |   | TRBRCR    |   | TRCCR1 |   |   | Function                    |                              |
|---------------|-------|----------|------|---|---|-----------|---|--------|---|---|-----------------------------|------------------------------|
| Bit           | PD1_4 | TXD0SEL0 | SMD  |   |   | TRCCLKSEL |   | TCK    |   |   |                             |                              |
|               |       |          | 2    | 1 | 0 | 1         | 0 | 2      | 1 | 0 |                             |                              |
| Setting Value | 0     | 0        | X    | X | X | X         | X | X      | X | X | Input port <sup>(1)</sup>   |                              |
|               | 1     | 0        | X    | X | X | X         | X | X      | X | X | Output port <sup>(2)</sup>  |                              |
|               | X     | 1        | 1    | 0 | 0 | 1         | X | X      | X | X | X                           | TXD0 output <sup>(2,3)</sup> |
|               |       |          |      | 0 |   | 0         |   |        |   |   |                             |                              |
|               |       |          |      | 1 |   | 0         |   |        |   |   |                             |                              |
| 0             | 0     | 0        | X    | X | X | 0         | 1 | 1      | 0 | 1 | TRCCLK input <sup>(1)</sup> |                              |

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR4 bit in the P1DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

**Table 7.14 Port P1\_5/RXD0/TRAIO/ $\overline{\text{INT1}}$** 

| Register      | PD1   | U0SR     | TRASR          |   | TRAIOC | TRAMR                 |   |   | INTSR   |   | INTEN  | INTCMP  | Function   |
|---------------|-------|----------|----------------|---|--------|-----------------------|---|---|---------|---|--------|---------|--|
| Bit           | PD1_5 | RXD0SEL0 | TRAIOSEL       |   | TOPCR  | TMOD                  |   |   | INT1SEL |   | INT1EN | INT1CP0 |  |
|               |       |          | 1              | 0 |        | 2                     | 1 | 0 | 1       | 0 |        |         |  |
| Setting Value | 0     | X        | Other than 10b |   | X      | X                     | X | X | X       | X | X      | X       | Input port <sup>(1)</sup>                            |
|               | 1     | X        | Other than 10b |   | X      | X                     | X | X | X       | X | X      | X       | Output port <sup>(2)</sup>                           |
|               | 0     | 1        | Other than 10b |   | X      | X                     | X | X | X       | X | X      | X       | RXD0 input <sup>(1)</sup>                            |
|               | 0     | X        | 1              | 0 | 0      | Other than 000b, 001b |   |   | X       | X | X      | X       | TRAIO input <sup>(1)</sup>                           |
|               | 0     | X        | Other than 10b |   | X      | X                     | X | X | 0       | 1 | 1      | 0       | $\overline{\text{INT1}}$ input <sup>(1)</sup>        |
|               | 0     | X        | 1              | 0 | 0      | Other than 000b, 001b |   |   | 0       | 1 | 1      | 0       | TRAIO/ $\overline{\text{INT1}}$ input <sup>(1)</sup> |
|               | X     | X        | 1              | 0 | 0      | 0                     | 0 | 1 | X       | X | X      | X       | TRAIO pulse output <sup>(2)</sup>                    |

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR5 bit in the P1DRR register to 1.

**Table 7.15 Port P1\_6/CLK0/IVREF1**

| Register      | PD1   | U0SR     | U0MR |   |   | INTCMP |         | Function                                    |
|---------------|-------|----------|------|---|---|--------|---------|---|
| Bit           | PD1_6 | CLK0SEL0 | SMD  |   |   | CKDIR  | INT1CP0 |   |
|               |       |          | 2    | 1 | 0 |        |         |   |
| Setting Value | 0     | 0        | X    | X | X | X      | X       | Input port <sup>(1)</sup>                   |
|               | 1     | 0        | X    | X | X | X      | X       | Output port <sup>(2)</sup>                  |
|               | 0     | 1        | X    | X | X | 1      | X       | CLK0 (external clock) input <sup>(1)</sup>  |
|               | X     | 1        | 0    | 0 | 1 | 0      | X       | CLK0 (internal clock) output <sup>(2)</sup> |
|               | 0     | 0        | 0    | X | X | X      | X       | 1   |

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR6 bit in the P1DRR register to 1.

**Table 7.16 Port P1\_7/INT1/TRAIO/IVCMP1**

| Register      | PD1   | TRASR          |   | TRAIOC | TRAMR                 |   |   | INTSR   |   | INTEN  | INTCMP  | Function               |
|---------------|-------|----------------|---|--------|-----------------------|---|---|---------|---|--------|---------|------------------------|
| Bit           | PD1_7 | TRAIOSEL       |   | TOPCR  | TMOD                  |   |   | INT1SEL |   | INT1EN | INT1CP0 |                        |
|               |       | 1              | 0 |        | 2                     | 1 | 0 | 1       | 0 |        |         |                        |
| Setting Value | 0     | Other than 01b |   | X      | X                     | X | X | X       | X | X      | X       | Input port (1)         |
|               | 1     | Other than 01b |   | X      | X                     | X | X | X       | X | X      | X       | Output port (2)        |
|               | 0     | 0              | 1 | 0      | Other than 000b, 001b |   |   | X       | X | X      | X       | TRAIO input (1)        |
|               | 0     | Other than 01b |   | X      | X                     | X | X | 0       | 0 | 1      | 0       | INT1 input (1)         |
|               | 0     | 0              | 1 | 0      | Other than 000b, 001b |   |   | 0       | 0 | 1      | 0       | TRAIO/INT1 input (1)   |
|               | X     | 0              | 1 | 0      | 0                     | 0 | 1 | X       | X | X      | X       | TRAIO pulse output (2) |
|               | 0     | Other than 01b |   | X      | X                     | X | X | X       | X | 1      | 1       | 1                      |

X: 0 or 1

Notes:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR7 bit in the P1DRR register to 1.

**Table 7.17 Port P3\_3/INT3/TRCCLK/CTS2/RTS2/IVCMP3**

| Register      | PD3   | INTEN  | TRBRCSR        |   | TRCCR1 |   |   | U2SR1   | U2MR            |   |   | U2CO |     | INTCMP  | Function                     |
|---------------|-------|--------|----------------|---|--------|---|---|---------|-----------------|---|---|------|-----|---------|------------------------------|
| Bit           | PD3_3 | INT3EN | TRCCLKSEL      |   | TCK    |   |   | CTS2SEL | SMD             |   |   | CRS  | CRD | INT3CP0 |                              |
|               |       |        | 1              | 0 | 2      | 1 | 0 |         | 0               | 2 | 1 |      |     |         |                              |
| Setting Value | 0     | X      | X              | X | X      | X | X | 0       | X               | X | X | X    | X   | X       | Input port (1)               |
|               | 1     | X      | X              | X | X      | X | X | 0       | X               | X | X | X    | X   | X       | Output port (2)              |
|               | 0     | 1      | X              | X | X      | X | X | 0       | X               | X | X | X    | X   | 0       | INT3 input (1)               |
|               | 0     | X      | 1              | 0 | 1      | 0 | 1 | 0       | X               | X | X | X    | X   | X       | TRCCLK input (1)             |
|               | 0     | X      | X              | X | X      | X | X | 1       | Other than 000b |   |   | 0    | 0   | X       | CTS2 input (1)               |
|               | X     | X      | X              | X | X      | X | X | 1       | Other than 000b |   |   | 1    | 0   | X       | RTS2 output (2)              |
|               | 0     | 1      | Other than 10b | X | X      | X | X | 0       | X               | X | X | X    | X   | 1       | Comparator B3 input (IVCMP3) |

X: 0 or 1

Notes:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.



**Table 7.18 Port P3\_4/TRCIOCR/RXD2/SCL2/TXD2/SDA2/IVREF3**

| Register      | PD3            | TRCPSR1        |                | U2SR0          |                |                | U2MR |     |   | U2SMR | INTCMP | Timer RC Setting | Function                                       |                          |                    |   |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|------|-----|---|-------|--------|------------------|--|--------------------------|--------------------|---|
| Bit           | PD3_4          | TRCIOCR SEL    |                | RXD2 SEL       |                | TXD2 SEL       |      | SMD |   |       | IICM   | INT3CP0          |  | —                        |                    |   |
|               |                | 1              | 0              | 1              | 0              | 1              | 0    | 2   | 1 | 0     |        |                  |  |                          |                    |   |
| Setting Value | 0              | Other than 10b |                | Other than 01b |                | Other than 10b |      | X   | X | X     | X      | X                | X  | Input port (1)           |                    |   |
|               | 1              | Other than 10b |                | Other than 01b |                | Other than 10b |      | X   | X | X     | X      | X                | X  | Output port (2)          |                    |   |
|               | 0              | 1              | 0              | Other than 01b |                | Other than 10b |      | X   | X | X     | X      | X                | Refer to <b>Table 7.28 TRCIOCR Pin Setting</b> | TRCIOCR input (1)        |                    |   |
|               | X              | 1              | 0              | Other than 01b |                | Other than 10b |      | X   | X | X     | X      | X                | Refer to <b>Table 7.28 TRCIOCR Pin Setting</b> | TRCIOCR output (2)       |                    |   |
|               | 0              | Other than 10b |                | 0              | 1              | Other than 10b |      | X   | X | X     | X      | X                | X  | RXD2 input (1)           |                    |   |
|               | 0              | X              | X              | 0              | 1              | Other than 10b |      | 0   | 1 | 0     | 1      | X                | X  | SCL2 input/output (2, 3) |                    |   |
|               | X              | X              | X              | X              | X              | 1              | 0    | 0   | 0 | 1     | 0      | X                | X  | X                        | TXD2 output (2, 3) |   |
|               |                |                |                |                |                |                | 1    |     |   |       |        |                  |  |                          |                    | 0 |
|               |                |                |                |                |                |                | 1    |     |   |       |        |                  |  |                          |                    | 0 |
| 0             | X              | X              | X              | X              | 1              | 0              | 0    | 1   | 0 | 1     | X      | X                | SDA2 input/output (2, 3)                       |                          |                    |   |
| 0             | Other than 10b |                | Other than 01b |                | Other than 10b |                | X    | X   | X | X     | 1      | X                | Comparator B3 reference voltage input (IVREF3) |                          |                    |   |

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

**Table 7.19 Port P3\_5/TRCIOD/CLK2**

| Register      | PD3   | TRCPSR1        |   | U2SR1    | U2MR |   |   | Timer RC Setting | Function                                      |                    |
|---------------|-------|----------------|---|----------|------|---|---|------------------|---|--------------------|
| Bit           | PD3_5 | TRCIODSEL      |   | CLK2SEL0 | SMD  |   |   | CKDIR            |   | —                  |
|               |       | 1              | 0 |          | 2    | 1 | 0 |                  |   |                    |
| Setting Value | 0     | Other than 10b |   | 0        | X    | X | X | X                | X   | Input port (1)     |
|               | 1     | Other than 10b |   | 0        | X    | X | X | X                | X   | Output port (2)    |
|               | 0     | 1              | 0 | 0        | X    | X | X | X                | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> | TRCIOD input (1)   |
|               | X     | 1              | 0 | 0        | X    | X | X | X                | Refer to <b>Table 7.29 TRCIOD Pin Setting</b> | TRCIOD output (2)  |
|               | 0     | X              | X | 1        | X    | X | X | 1                | X   | CLK2 input (2)     |
|               | X     | X              | X | 1        | 0    | 0 | 1 | 0                | X   | CLK2 output (2, 3) |

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.

**Table 7.20 Port P3\_7/TXD2/SDA2/RXD2/SCL2/TRAO**

| Register      | PD3            | U2SR0          |                |                |   | U2MR |   |   | U2SMR | TRAI0C                     | Function                            |                               |
|---------------|----------------|----------------|----------------|----------------|---|------|---|---|-------|----------------------------|-------------------------------------|-------------------------------|
| Bit           | PD3_7          | RXD2SEL        |                | TXD2SEL        |   | SMD  |   |   | IICM  | TOENA                      |                                     |                               |
|               |                | 1              | 0              | 1              | 0 | 2    | 1 | 0 |       |                            |                                     |                               |
| Setting Value | 0              | Other than 10b |                | Other than 01b |   | X    | X | X | X     | 0                          | Input port <sup>(1)</sup>           |                               |
|               | 1              | Other than 10b |                | Other than 01b |   | X    | X | X | X     | 0                          | Output port <sup>(2)</sup>          |                               |
|               | 0              | 1              | 0              | Other than 01b |   | X    | X | X | X     | 0                          | RXD2 input <sup>(1)</sup>           |                               |
|               | 0              | 1              | 0              | Other than 01b |   | 0    | 1 | 0 | 1     | X                          | SCL2 input/output <sup>(2, 3)</sup> |                               |
|               | X              | X              | X              | 0              | 1 | 1    | 0 | 1 | X     | X                          | X                                   | TXD2 output <sup>(2, 3)</sup> |
|               |                |                |                |                |   |      |   | 0 |       |                            |                                     |                               |
|               |                |                |                |                |   |      |   | 1 |       |                            |                                     |                               |
|               | 0              | X              | X              | 0              | 1 | 0    | 1 | 0 | 1     | X                          | SDA2 input/output <sup>(2, 3)</sup> |                               |
| X             | Other than 10b |                | Other than 01b |                | X | X    | X | X | 1     | TRAO output <sup>(2)</sup> |                                     |                               |

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

**Table 7.21 Port P4\_2/VREF**

| Register      | ADCON1 | Function              |
|---------------|--------|-----------------------|
| Bit           | ADSTBY |                       |
| Setting Value | 0      | Input port            |
|               | 1      | Input port/VREF input |

**Table 7.22 Port P4\_5/INT0/RXD2/SCL2/ADTRG**

| Register      | PD4   | INTEN  | U2SR0          |   | U2MR |   |   | U2SMR | ADM0D |   | Function                 |
|---------------|-------|--------|----------------|---|------|---|---|-------|-------|---|--------------------------|
| Bit           | PD4_5 | INT0EN | RXD2SEL        |   | SMD  |   |   | IICM  | ADCAP |   |                          |
|               |       |        | 1              | 0 | 2    | 1 | 0 |       | 1     | 0 |                          |
| Setting Value | 0     | X      | Other than 11b |   | X    | X | X | X     | X     | X | Input port (1)           |
|               | 1     | X      | Other than 11b |   | X    | X | X | X     | X     | X | Output port (2)          |
|               | 0     | 1      | Other than 11b |   | X    | X | X | X     | X     | X | INT0 input (1)           |
|               | 0     | X      | 1              | 1 | X    | X | X | X     | X     | X | RXD2 input (1)           |
|               | 0     | X      | 1              | 1 | 0    | 1 | 0 | 1     | X     | X | SCL2 input/output (2, 3) |
|               | 0     | 1      | Other than 11b |   | X    | X | X | X     | X     | 1 | 1                        |

X: 0 or 1

Notes:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

**Table 7.23 Port P4\_6/XIN/XCIN**

| Register      | PD4   | CM0  |      |      |      | CM1  |      |      |      | Circuit specifications |                              | Function        |  |  |
|---------------|-------|------|------|------|------|------|------|------|------|------------------------|------------------------------|-----------------|--|--|
| Bit           | PD4_6 | CM01 | CM03 | CM04 | CM05 | CM10 | CM11 | CM12 | CM13 | Oscillation buffer     | Feedback resistor            |                 |  |  |
| Setting Value | 0     | X    | X    | 0    | X    | 0    | X    | X    | 0    | OFF                    | OFF                          | Input port (1)  |  |  |
|               | 1     | X    | X    | 0    | X    | 0    | X    | X    | 0    | OFF                    | OFF                          | Output port (2) |  |  |
|               | X     | X    | 0    | X    | X    | 0    | 0    | 0    | X    | 1                      | ON                           | ON              | XIN-XOUT oscillation (on-chip feedback resistor enabled)       |  |
|               |       |      |      |      |      |      |      | 1    |      |                        | ON                           | OFF             | XIN-XOUT oscillation (on-chip feedback resistor disabled)      |  |
|               |       |      |      |      |      |      |      | 0    |      |                        | OFF                          | ON              | XIN-XOUT oscillation stop (on-chip feedback resistor enabled)  |  |
|               |       |      |      |      |      |      |      | 1    |      |                        | OFF                          | OFF             | XIN-XOUT oscillation stop (on-chip feedback resistor disabled) |  |
|               |       |      | 1    | 0    | 1    | X    | 0    | X    | 0    | X                      | 1                            | ON              | ON   | XCIN-XCOUT oscillation (on-chip feedback resistor enabled)       |
|               |       |      |      |      |      |      |      |      | 1    |                        |                              | ON              | OFF  | XCIN-XCOUT oscillation (on-chip feedback resistor disabled)      |
|               |       |      |      |      |      |      |      |      | 0    |                        |                              | OFF             | ON   | XCIN-XCOUT oscillation stop (on-chip feedback resistor enabled)  |
|               |       |      |      |      |      |      |      |      | 1    |                        |                              | OFF             | OFF  | XCIN-XCOUT oscillation stop (on-chip feedback resistor disabled) |
|               | X     | X    | X    |      |      | 1    | X    | X    | OFF  | OFF                    | Oscillation stop (STOP mode) |                 |  |  |

X: 0 or 1

Notes:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

**Table 7.24 Port P4\_7/XOUT/XCOUT**

| Register      | PD4   | CM0  |      |      |      | CM1  |      |      |      | Circuit specifications |                   | Function                     |  |
|---------------|-------|------|------|------|------|------|------|------|------|------------------------|-------------------|------------------------------|--|
| Bit           | PD4_7 | CM01 | CM03 | CM04 | CM05 | CM10 | CM11 | CM12 | CM13 | Oscillation buffer     | Feedback resistor |                              |  |
| Setting Value | 0     | X    | X    | 0    | X    | 0    | X    | X    | 0    | OFF                    | OFF               | Input port <sup>(1)</sup>    |  |
|               | 1     | X    | X    | 0    | X    | 0    | X    | X    | 0    | OFF                    | OFF               | Output port <sup>(2)</sup>   |  |
|               | X     | X    | 0    | X    | X    | 0    | 0    | 0    | X    | 1                      | ON                | ON                           | XIN-XOUT oscillation (on-chip feedback resistor enabled)                   |
|               |       |      |      |      |      |      |      | 1    |      |                        | ON                | OFF                          | XIN-XOUT oscillation (on-chip feedback resistor disabled)                  |
|               |       |      |      |      |      |      |      | 0    |      |                        | OFF               | ON                           | XIN-XOUT oscillation stop (on-chip feedback resistor enabled)              |
|               |       |      |      |      |      |      |      | 1    |      |                        | OFF               | OFF                          | XIN-XOUT oscillation stop (on-chip feedback resistor disabled)             |
|               |       |      | 1    | 0    | 1    | X    | 0    | X    | 0    | 1                      | ON                | ON                           | XCIN-XCOUT oscillation (on-chip feedback resistor enabled) <sup>(3)</sup>  |
|               |       |      |      |      |      |      |      |      | 1    |                        | ON                | OFF                          | XCIN-XCOUT oscillation (on-chip feedback resistor disabled) <sup>(3)</sup> |
|               |       |      |      |      |      |      |      |      | 0    |                        | OFF               | ON                           | XCIN-XCOUT oscillation stop (on-chip feedback resistor enabled)            |
|               |       |      |      |      |      |      |      |      | 1    |                        | OFF               | OFF                          | XCIN-XCOUT oscillation stop (on-chip feedback resistor disabled)           |
|               | X     | X    | X    |      |      | 1    |      | X    | X    | OFF                    | OFF               | Oscillation stop (STOP mode) |  |

X: 0 or 1

Notes:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.
3. Since the XCIN-XCOUT oscillation buffer operates with internal step-down power, the XCOUT output level cannot be used as the CMOS level signal directly.

**Table 7.25 TRBO Pin Setting**

| Register      | TRBIOC | TRBMR |       | Function  |
|---------------|--------|-------|-------|---|
| Bit           | TOCNT  | TMOD1 | TMOD0 |   |
| Setting Value | 0      | 0     | 1     | Programmable waveform generation mode (pulse output)        |
|               | 1      | 0     | 1     | Programmable waveform generation mode (programmable output) |
|               | 0      | 1     | 0     | Programmable one-shot generation mode                       |
|               | 0      | 1     | 1     | Programmable wait one-shot generation mode                  |

**Table 7.26 TRCIOA Pin Setting**

| Register      | TRCOER | TRCMR | TRCIOR0 |      |      | TRCCR2 |                         | Function  |
|---------------|--------|-------|---------|------|------|--------|-------------------------|---|
| Bit           | EA     | PWM2  | IOA2    | IOA1 | IOA0 | TCEG1  | TCEG0                   |   |
| Setting Value | 0      | 1     | 0       | 0    | 1    | X      | X                       | Timer waveform output (output compare function) |
|               |        |       |         | 1    | X    |        |                         |   |
|               | 1      | 0     | X       | X    | X    | X      | X                       | Timer mode (input capture function)             |
|               |        |       |         |      |      |        |                         |   |
| 1             | 0      | X     | X       | X    | 0    | 1      | PWM2 mode TRCTRIG input |   |
|               |        |       |         |      | 1    | X      |                         |   |

X: 0 or 1

**Table 7.27 TRCIOB Pin Setting**

| Register      | TRCOER | TRCMR |      | TRCIOR0 |      |      | Function  |                                     |
|---------------|--------|-------|------|---------|------|------|---|-------------------------------------|
| Bit           | EB     | PWM2  | PWMB | IOB2    | IOB1 | IOB0 |   |                                     |
| Setting Value | 0      | 0     | X    | X       | X    | X    | PWM2 mode waveform output                       |                                     |
|               |        |       |      |         |      |      |   | 1                                   |
|               | 0      | 1     | 0    | 0       | 0    | 1    | Timer waveform output (output compare function) |                                     |
|               |        |       |      |         | 1    | X    |   |                                     |
|               | 1      | 0     | 1    | 0       | 1    | X    | X   | Timer mode (input capture function) |
|               |        |       |      |         |      |      |   |                                     |

X: 0 or 1

**Table 7.28 TRCIOC Pin Setting**

| Register      | TRCOER | TRCMR |      | TRCIOR1 |      |      | Function                 |
|---------------|--------|-------|------|---------|------|------|--------------------------|
| Bit           | EC     | PWM2  | PWMC | IOC2    | IOC1 | IOC0 |                          |
| Setting Value | 0      | 1     | 1    | X       | X    | X    | PWM mode waveform output |
|               |        |       |      |         |      |      |                          |
|               | 1      | X     |      |         |      |      |                          |
|               | 1      | 0     | 1    | 0       | 1    | X    | X                        |
| 1             |        |       |      |         |      |      |                          |

X: 0 or 1

**Table 7.29 TRCIOD Pin Setting**

| Register      | TRCOER | TRCMR |      | TRCIOR1 |      |      | Function                 |
|---------------|--------|-------|------|---------|------|------|--------------------------|
| Bit           | ED     | PWM2  | PWMD | IOD2    | IOD1 | IOD0 |                          |
| Setting Value | 0      | 1     | 1    | X       | X    | X    | PWM mode waveform output |
|               |        |       |      |         |      |      |                          |
|               | 1      | X     |      |         |      |      |                          |
|               | 1      | 0     | 1    | 0       | 1    | X    | X                        |
| 1             |        |       |      |         |      |      |                          |

X: 0 or 1

## 7.6 Unassigned Pin Handling

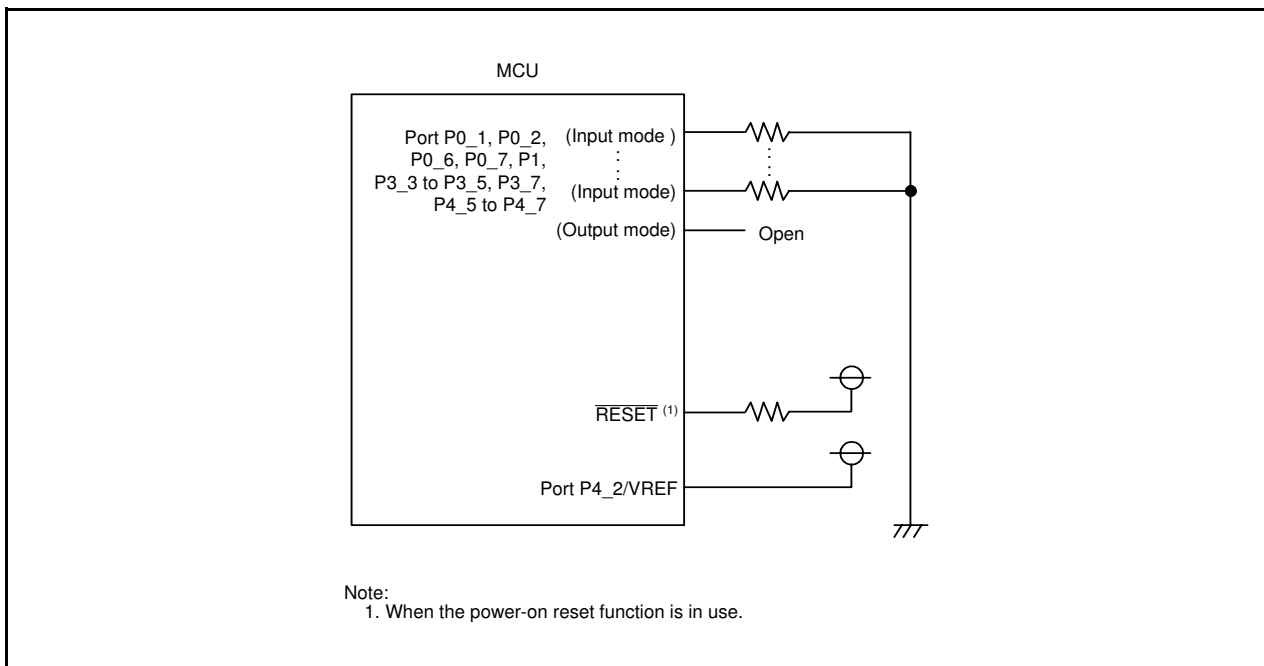
Table 7.30 lists Unassigned Pin Handling. Figure 7.10 shows the Unassigned Pin Handling.

**Table 7.30 Unassigned Pin Handling**

| Pin Name   | Connection  |
|--|---|
| Ports P0_1, P0_2, P0_6, P0_7, P1, P3_3 to P3_5, P3_7, P4_5 to P4_7 | <ul style="list-style-type: none"> <li>• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2)</li> <li>• After setting to output mode, leave these pins open. (1, 2)</li> </ul> |
| Port P4_2/VREF   | Connect to VCC  |
| RESET (3)  | Connect to VCC via a pull-up resistor (2)   |

Notes:

1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode. The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.



**Figure 7.10 Unassigned Pin Handling**

## 8. Bus

The bus cycles differ when accessing ROM/RAM and when accessing SFR.

Table 8.1 lists Bus Cycles by Access Area of R8C/3GD Group.


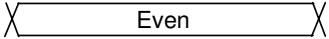
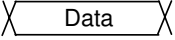

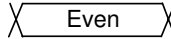
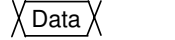

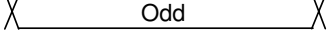


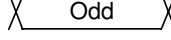
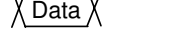

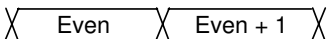


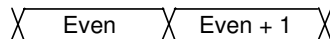


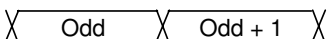


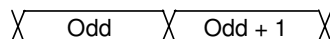

ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.

Table 8.2 shows Access Units and Bus Operations.

**Table 8.1 Bus Cycles by Access Area of R8C/3GD Group**

| Access Area     | Bus Cycle             |
|-----------------|-----------------------|
| SFR             | 2 cycles of CPU clock |
| Program ROM/RAM | 1 cycle of CPU clock  |

**Table 8.2 Access Units and Bus Operations**

| Area                        | SFR  | ROM (program ROM), RAM   |
|-----------------------------|--|--|
| Even address<br>Byte access | CPU clock <br>Address <br>Data        | CPU clock <br>Address <br>Data        |
| Odd address<br>Byte access  | CPU clock <br>Address <br>Data   | CPU clock <br>Address <br>Data   |
| Even address<br>Word access | CPU clock <br>Address <br>Data  | CPU clock <br>Address <br>Data  |
| Odd address<br>Word access  | CPU clock <br>Address <br>Data  | CPU clock <br>Address <br>Data  |

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register

Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD

UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR

A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1

Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.



## 9. Clock Generation Circuit

The following five circuits are incorporated in the clock generation circuit:

- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for watchdog timer

### 9.1 Overview

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows a Clock Generation Circuit (With XIN and XCIN Pins Shared). Figure 9.2 shows a Peripheral Function Clock and Figure 9.3 shows a Procedure for Reducing Internal Power Consumption Using VCA20 bit.

**Table 9.1 Specification Overview of Clock Generation Circuit**

| Item                               | XIN Clock Oscillation Circuit  | XCIN Clock Oscillation Circuit  | On-Chip Oscillator  |   | Low-Speed On-Chip Oscillator for Watchdog Timer                                 |
|------------------------------------|--|---|---|---|---|
|                                    |  |   | High-Speed On-Chip Oscillator   | Low-Speed On-Chip Oscillator  |   |
| Applications                       | <ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> </ul> | <ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> </ul>  | <ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> <li>• CPU and peripheral function clock source when XIN clock stops oscillating</li> </ul> | <ul style="list-style-type: none"> <li>• CPU clock source</li> <li>• Peripheral function clock source</li> <li>• CPU and peripheral function clock source when XIN clock stops oscillating</li> </ul> | <ul style="list-style-type: none"> <li>• Watchdog timer clock source</li> </ul> |
| Clock frequency                    | 0 to 20 MHz  | 32.768 kHz  | Approx. 40 MHz <sup>(3)</sup>   | Approx. 125 kHz   | Approx. 125 kHz   |
| Connectable oscillator             | <ul style="list-style-type: none"> <li>• Ceramic resonator</li> <li>• Crystal oscillator</li> </ul>              | <ul style="list-style-type: none"> <li>• Crystal oscillator</li> </ul>  | –   | –   | –   |
| Oscillator connect pins            | XIN, XOUT <sup>(1)</sup>   | XCIN, XCOU <sup>(1)</sup>   | – <sup>(1)</sup>  | – <sup>(1)</sup>  | –   |
| Oscillation stop, restart function | Usable   | Usable  | Usable  | Usable  | Usable  |
| Oscillator status after reset      | Stop   | Stop  | Stop  | Oscillate   | Stop <sup>(4)</sup><br>Oscillate <sup>(5)</sup>                                 |
| Others                             | Externally generated clock can be input <sup>(2)</sup>   | <ul style="list-style-type: none"> <li>• Externally generated clock can be input</li> <li>• On-chip feedback resistor R<sub>f</sub> (connected/not connected selectable)</li> </ul> | –   | –   | –   |

Notes:

1. These pins can be used as P4\_6 or P4\_7 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit and the XCIN clock oscillation circuit are not used.
2. To input an external clock, set the CM05 bit in the CM0 register to 1 (XIN clock stops), the CM11 bit in the CM1 register to 1 (internal feedback resistor disabled), and the CM13 bit to 1 (XIN-XOUT pin).
3. The clock frequency is automatically set to up to 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.
4. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

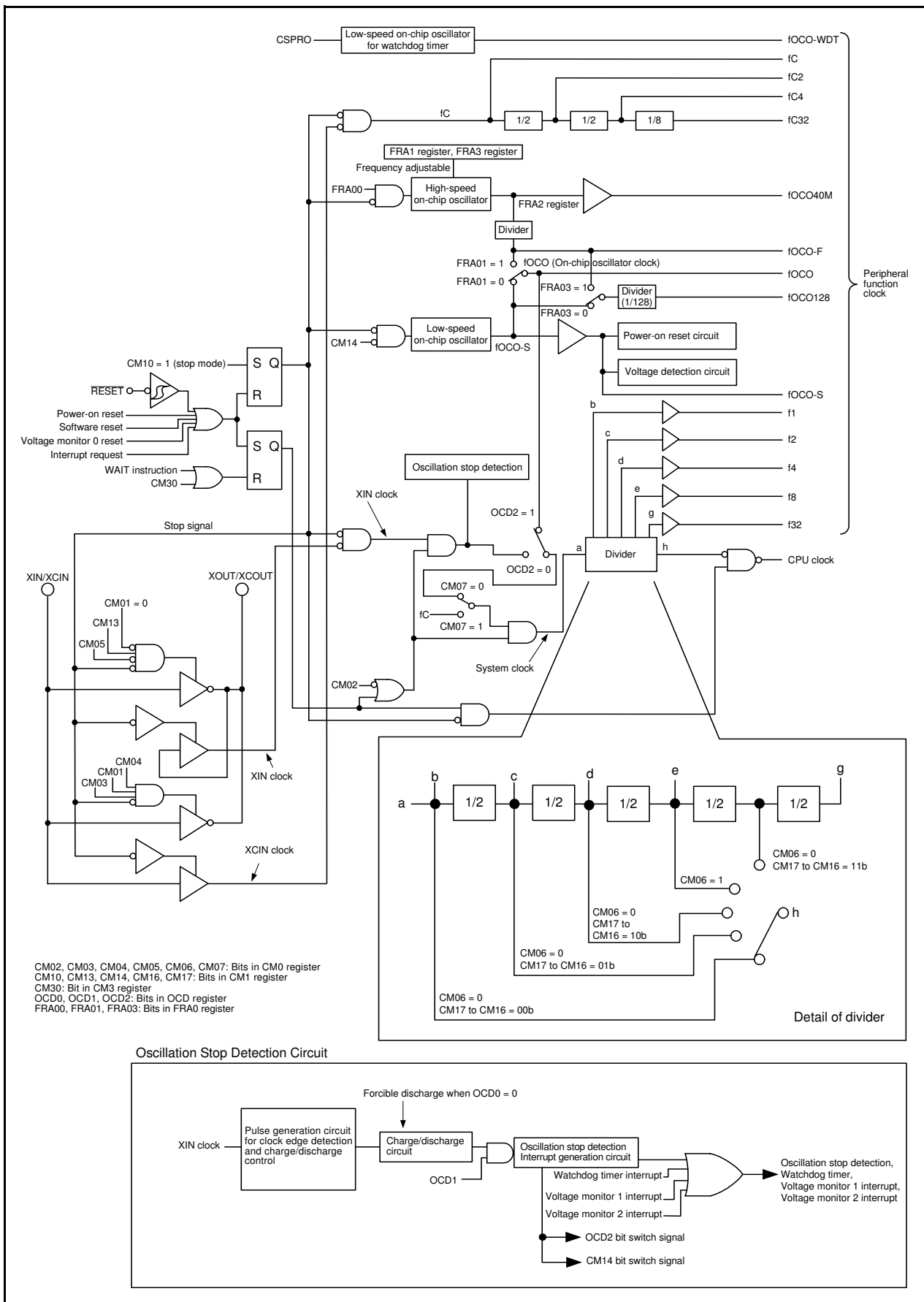


Figure 9.1 Clock Generation Circuit (With XIN and XCIN Pins Shared)

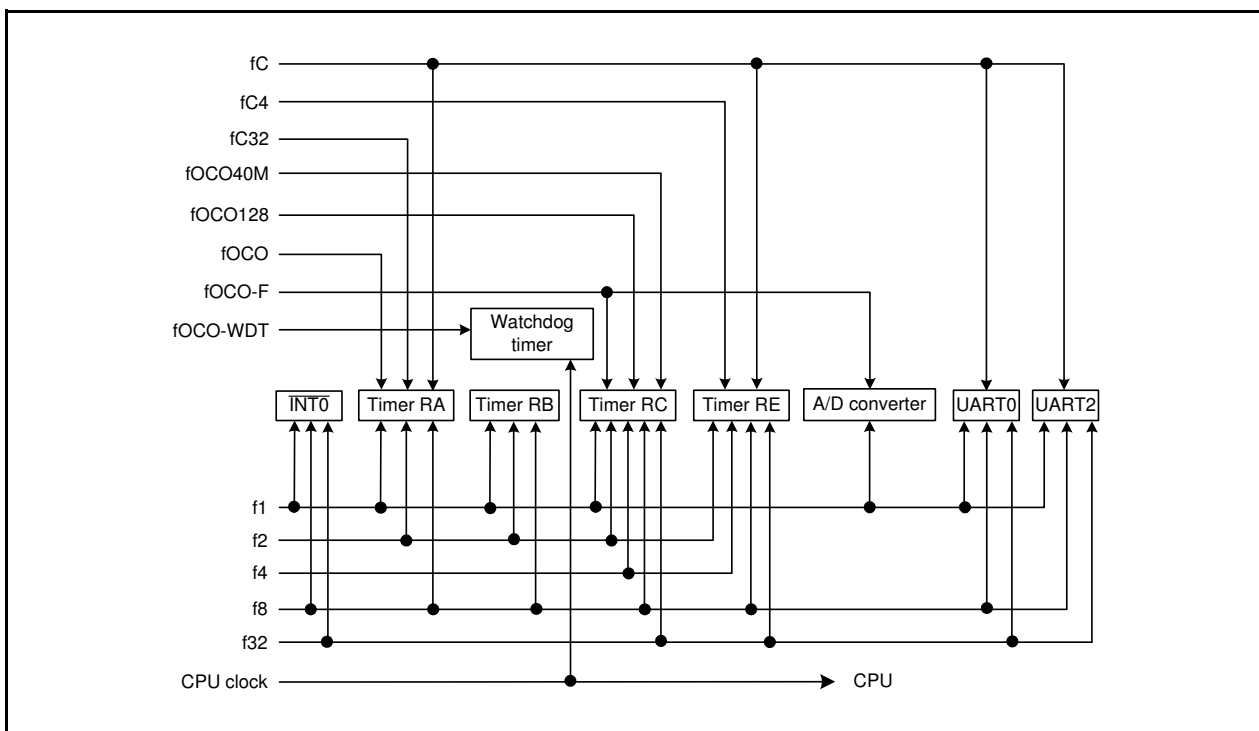


Figure 9.2 Peripheral Function Clock

## 9.2 Registers

### 9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

|             |      |      |      |      |      |      |      |    |
|-------------|------|------|------|------|------|------|------|----|
| Bit         | b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0 |
| Symbol      | CM07 | CM06 | CM05 | CM04 | CM03 | CM02 | CM01 | —  |
| After Reset | 0    | 0    | 1    | 0    | 1    | 0    | 0    | 0  |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | —      | Reserved bit                                    | Set to 0.  | R/W |
| b1  | CM01   | XIN-XCIN switch bit                             | 0: P4_6 and P4_7 set as XIN-XOUT pin<br>1: P4_6 and P4_7 set as XCIN-XCOUT pin                             | R/W |
| b2  | CM02   | Wait mode peripheral function clock stop bit    | 0: Peripheral function clock does not stop in wait mode<br>1: Peripheral function clock stops in wait mode | R/W |
| b3  | CM03   | XCIN clock stop bit                             | 0: XCIN clock oscillates<br>1: XCIN clock stops  | R/W |
| b4  | CM04   | Port/XCIN-XCOUT switch bit <sup>(5)</sup>       | 0: I/O ports P4_6 and P4_7<br>1: XCIN-XCOUT pin <sup>(6)</sup>   | R/W |
| b5  | CM05   | XIN clock (XIN-XOUT) stop bit <sup>(1, 3)</sup> | 0: XIN clock oscillates<br>1: XIN clock stops <sup>(2)</sup>   | R/W |
| b6  | CM06   | CPU clock division select bit 0 <sup>(4)</sup>  | 0: Bits CM16 and CM17 in CM1 register enabled<br>1: Divide-by-8 mode                                       | R/W |
| b7  | CM07   | XIN, XCIN clock select bit <sup>(7)</sup>       | 0: XIN clock<br>1: XCIN clock  | R/W |

Notes:

- The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
  - Set bits OCD1 to OCD0 in the OCD register to 00b.
  - Set the OCD2 bit to 1 (on-chip oscillator clock selected).
- During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
- Only when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4\_6 and P4\_7), P4\_6 and P4\_7 can be used as I/O ports.
- When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
- The CM04 bit can be set to 1 by a program but cannot be set to 0.
- To use the XCIN clock, set the CM04 bit to 1.
- Set the CM07 bit to 1 (XCIN clock) from 0 after setting the CM04 bit to 1 (XCIN-XCOUT pin) and allowing XCIN clock oscillation to stabilize.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

## 9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

|             |      |      |    |      |      |      |      |      |
|-------------|------|------|----|------|------|------|------|------|
| Bit         | b7   | b6   | b5 | b4   | b3   | b2   | b1   | b0   |
| Symbol      | CM17 | CM16 | —  | CM14 | CM13 | CM12 | CM11 | CM10 |
| After Reset | 0    | 0    | 1  | 0    | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | CM10   | All clock stop control bit <sup>(2, 6)</sup>            | 0: Clock oscillates<br>1: All clocks stop (stop mode)   | R/W |
| b1  | CM11   | XIN-XOUT on-chip feedback resistor select bit           | 0: On-chip feedback resistor enabled<br>1: On-chip feedback resistor disabled   | R/W |
| b2  | CM12   | XCIN-XCOUT on-chip feedback resistor select bit         | 0: On-chip feedback resistor enabled<br>1: On-chip feedback resistor disabled   | R/W |
| b3  | CM13   | Port/XIN-XOUT switch bit <sup>(5)</sup>                 | 0: I/O ports P4_6 and P4_7<br>1: XIN-XOUT pin   | R/W |
| b4  | CM14   | Low-speed on-chip oscillator stop bit <sup>(3, 4)</sup> | 0: Low-speed on-chip oscillator on<br>1: Low-speed on-chip oscillator off   | R/W |
| b5  | —      | Reserved bit  | Set to 1.   | R/W |
| b6  | CM16   | CPU clock division select bit 1 <sup>(1)</sup>          | <sup>b7 b6</sup><br>0 0: No division mode<br>0 1: Divide-by-2 mode<br>1 0: Divide-by-4 mode<br>1 1: Divide-by-16 mode | R/W |
| b7  | CM17   |   |   | R/W |

## Notes:

- When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
- If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
- When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
- To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
- Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
- Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

### 9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

| Bit         | b7   | b6   | b5   | b4 | b3 | b2 | b1 | b0   |
|-------------|------|------|------|----|----|----|----|------|
| Symbol      | CM37 | CM36 | CM35 | —  | —  | —  | —  | CM30 |
| After Reset | 0    | 0    | 0    | 0  | 0  | 0  | 0  | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | CM30   | Wait control bit <sup>(1)</sup>   | 0: Other than wait mode<br>1: MCU enters wait mode   | R/W |
| b1  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b2  | —      |   |  |     |
| b3  | —      | Reserved bits   | Set to 0.  | R/W |
| b4  | —      |   |  |     |
| b5  | CM35   | CPU clock division when exiting wait mode select bit <sup>(2)</sup>       | 0: Following settings are enabled:<br>CM06 bit in CM0 register<br>Bits CM16 and CM17 in CM1 register<br>1: No division   | R/W |
| b6  | CM36   | System clock when exiting wait mode or stop mode select bit               | <sup>b7 b6</sup><br>0 0: MCU exits with the CPU clock immediately before entering wait or stop mode.<br>0 1: Do not set.<br>1 0: High-speed on-chip oscillator clock selected <sup>(3)</sup><br>1 1: XIN clock selected <sup>(4)</sup> | R/W |
| b7  | CM37   |   |  | R/W |

Notes:

- When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
- Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
- When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
  - OCD2 bit in OCD register = 1 (on-chip oscillator selected)
  - FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
  - FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
- When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
  - OM05 bit in OM0 register = 1 (XIN clock oscillates)
  - OM13 bit in OM1 register = 1 (XIN-XOUT pin)
  - OCD2 bit in OCD register = 0 (XIN clock selected)
 When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.  
 However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

#### CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock, XCIN clock, and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

### 9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

|             |    |    |    |    |      |      |      |      |
|-------------|----|----|----|----|------|------|------|------|
| Bit         | b7 | b6 | b5 | b4 | b3   | b2   | b1   | b0   |
| Symbol      | —  | —  | —  | —  | OCD3 | OCD2 | OCD1 | OCD0 |
| After Reset | 0  | 0  | 0  | 0  | 0    | 1    | 0    | 0    |

| Bit | Symbol | Bit Name   | Function   | R/W |
|-----|--------|--|--|-----|
| b0  | OCD0   | Oscillation stop detection enable bit <sup>(6)</sup> | 0: Oscillation stop detection function disabled <sup>(1)</sup><br>1: Oscillation stop detection function enabled | R/W |
| b1  | OCD1   | Oscillation stop detection interrupt enable bit      | 0: Disabled <sup>(1)</sup><br>1: Enabled   | R/W |
| b2  | OCD2   | System clock select bit <sup>(3)</sup>               | 0: XIN clock selected <sup>(6)</sup><br>1: On-chip oscillator clock selected <sup>(2)</sup>                      | R/W |
| b3  | OCD3   | Clock monitor bit <sup>(4, 5)</sup>                  | 0: XIN clock oscillates<br>1: XIN clock stops  | R   |
| b4  | —      | Reserved bits  | Set to 0.  | R/W |
| b5  | —      |  |  |     |
| b6  | —      |  |  |     |
| b7  | —      |  |  |     |

Notes:

- Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
- If the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
- The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
- The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
- The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
- Refer to **Figure 9.10 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock** for the switching procedure when the XIN clock re-oscillates after detecting oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

### 9.2.5 High-Speed On-Chip Oscillator Control Register 7 (FRA7)

Address 0015h

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function   | R/W |
|-------|--|-----|
| b7-b0 | 32 MHz frequency correction data is stored.<br>The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA6 register to the FRA1 register. | R   |

### 9.2.6 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

|             |    |    |    |    |       |    |       |       |
|-------------|----|----|----|----|-------|----|-------|-------|
| Bit         | b7 | b6 | b5 | b4 | b3    | b2 | b1    | b0    |
| Symbol      | —  | —  | —  | —  | FRA03 | —  | FRA01 | FRA00 |
| After Reset | 0  | 0  | 0  | 0  | 0     | 0  | 0     | 0     |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | FRA00  | High-speed on-chip oscillator enable bit                                  | 0: High-speed on-chip oscillator off<br>1: High-speed on-chip oscillator on                          | R/W |
| b1  | FRA01  | High-speed on-chip oscillator select bit <sup>(1)</sup>                   | 0: Low-speed on-chip oscillator selected <sup>(2)</sup><br>1: High-speed on-chip oscillator selected | R/W |
| b2  | —      | Reserved bit  | Set to 0.  | R/W |
| b3  | FRA03  | fOCO128 clock select bit  | 0: fOCO-S divided by 128 selected<br>1: fOCO-F divided by 128 selected                               | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Notes:

- Change the FRA01 bit in the following conditions.
  - FRA00 = 1 (high-speed on-chip oscillator on)
  - The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
  - Bits FRA22 to FRA20 in the FRA2 register:
    - All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
    - Divide ratio of 8 or more when VCC = 1.8 V to 5.5 V 110b to 111b (divide-by-8 or more)
- When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

### 9.2.7 High-Speed On-Chip Oscillator Control Register 1 (FRA1)

Address 0024h

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function  | R/W |
|-------|---|-----|
| b7-b0 | The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows:<br>40 MHz: FRA1 = value after reset, FRA3 = value after reset<br>36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register.<br>32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register. | R/W |

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA1 register.

Also, rewrite the FRA1 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).



### 9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

|             |    |    |    |    |    |       |       |       |
|-------------|----|----|----|----|----|-------|-------|-------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1    | b0    |
| Symbol      | —  | —  | —  | —  | —  | FRA22 | FRA21 | FRA20 |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | FRA20  | High-speed on-chip oscillator frequency switching bit | Division selection<br>These bits select the division ratio for the high-speed on-chip oscillator clock.<br>b2 b1 b0<br>0 0 0: Divide-by-2 mode<br>0 0 1: Divide-by-3 mode<br>0 1 0: Divide-by-4 mode<br>0 1 1: Divide-by-5 mode<br>1 0 0: Divide-by-6 mode<br>1 0 1: Divide-by-7 mode<br>1 1 0: Divide-by-8 mode<br>1 1 1: Divide-by-9 mode | R/W |
| b1  | FRA21  |   |   | R/W |
| b2  | FRA22  |   |   | R/W |
| b3  | —      | Reserved bits   | Set to 0.   | R/W |
| b4  | —      |   |   |     |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      |   |   |     |

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

### 9.2.9 Clock Prescaler Reset Flag (CPSRF)

Address 0028h

|             |      |    |    |    |    |    |    |    |
|-------------|------|----|----|----|----|----|----|----|
| Bit         | b7   | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | CPSR | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

| Bit | Symbol | Bit Name                   | Function  | R/W |
|-----|--------|----------------------------|---|-----|
| b0  | —      | Reserved bits              | Set to 0.   | R/W |
| b1  | —      |                            |   |     |
| b2  | —      |                            |   |     |
| b3  | —      |                            |   |     |
| b4  | —      |                            |   |     |
| b5  | —      |                            |   |     |
| b6  | —      | Clock prescaler reset flag | Setting this bit to 1 initializes the clock prescaler.<br>(When read, the content is 0) | R/W |
| b7  | CPSR   |                            |   |     |

### 9.2.10 High-Speed On-Chip Oscillator Control Register 4 (FRA4)

Address 0029h

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function   | R/W |
|-------|--|-----|
| b7-b0 | 36.864 MHz frequency correction data is stored.<br>The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA5 register to the FRA3 register. | R   |

### 9.2.11 High-Speed On-Chip Oscillator Control Register 5 (FRA5)

Address 002Ah

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function   | R/W |
|-------|--|-----|
| b7-b0 | 36.864 MHz frequency correction data is stored.<br>The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA4 register to the FRA1 register. | R   |

### 9.2.12 High-Speed On-Chip Oscillator Control Register 6 (FRA6)

Address 002Bh

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function   | R/W |
|-------|--|-----|
| b7-b0 | 32 MHz frequency correction data is stored.<br>The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA7 register to the FRA3 register. | R   |

### 9.2.13 High-Speed On-Chip Oscillator Control Register 3 (FRA3)

Address 002Fh

|             |               |    |    |    |    |    |    |    |
|-------------|---------------|----|----|----|----|----|----|----|
| Bit         | b7            | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —             | —  | —  | —  | —  | —  | —  | —  |
| After Reset | When shipping |    |    |    |    |    |    |    |

| Bit   | Function  | R/W |
|-------|---|-----|
| b7-b0 | The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows:<br>40 MHz: FRA1 = value after reset, FRA3 = value after reset<br>36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register.<br>32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register. | R/W |

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA3 register.

Also, rewrite the FRA3 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

### 9.2.14 Voltage Detect Register 2 (VCA2)

Address 0034h

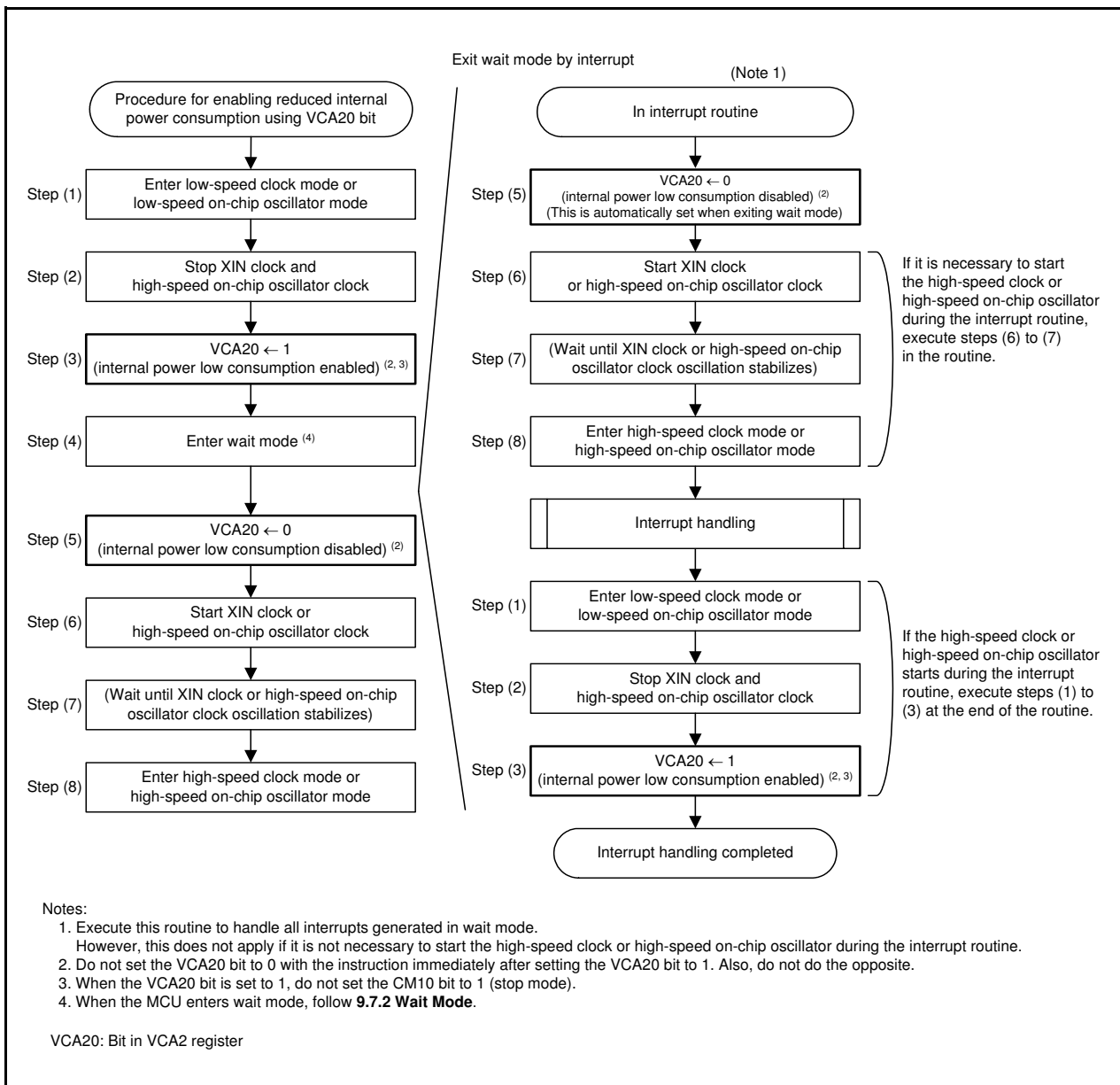
| Bit         | b7  | b6    | b5    | b4 | b3 | b2 | b1 | b0    |
|-------------|---|-------|-------|----|----|----|----|-------|
| Symbol      | VCA27   | VCA26 | VCA25 | —  | —  | —  | —  | VCA20 |
| After Reset | 0   | 0     | 0     | 0  | 0  | 0  | 0  | 0     |
|             | The above applies when the LVDAS bit in the OFS register is set to 1. |       |       |    |    |    |    |       |
| After Reset | 0   | 0     | 1     | 0  | 0  | 0  | 0  | 0     |
|             | The above applies when the LVDAS bit in the OFS register is set to 0. |       |       |    |    |    |    |       |

| Bit | Symbol | Bit Name   | Function  | R/W |
|-----|--------|--|---|-----|
| b0  | VCA20  | Internal power low consumption enable bit <sup>(1)</sup> | 0: Low consumption disabled<br>1: Low consumption enabled <sup>(2)</sup>          | R/W |
| b1  | —      | Reserved bits  | Set to 0.   | R/W |
| b2  | —      |  |   |     |
| b3  | —      |  |   |     |
| b4  | —      |  |   |     |
| b5  | VCA25  | Voltage detection 0 enable bit <sup>(3)</sup>            | 0: Voltage detection 0 circuit disabled<br>1: Voltage detection 0 circuit enabled | R/W |
| b6  | VCA26  | Voltage detection 1 enable bit <sup>(4)</sup>            | 0: Voltage detection 1 circuit disabled<br>1: Voltage detection 1 circuit enabled | R/W |
| b7  | VCA27  | Voltage detection 2 enable bit <sup>(5)</sup>            | 0: Voltage detection 2 circuit disabled<br>1: Voltage detection 2 circuit enabled | R/W |

Notes:

1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.



**Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**

The clocks generated by the clock generation circuits are described below.

### 9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XOUT pin.

Figure 9.4 shows Examples of XIN Clock Connection Circuit.

During and after a reset, the XIN clock stops.

After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates). After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source when the OCD2 bit in the OCD register is set to 0 (XIN clock selected).

The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).

When an externally generated clock is input to the XOUT pin, the XIN clock does not stop even if the CM05 bit is set to 1. If necessary, use an external circuit to stop the clock.

In stop mode, all clocks including the XIN clock stop. Refer to **9.7 Power Control** for details.

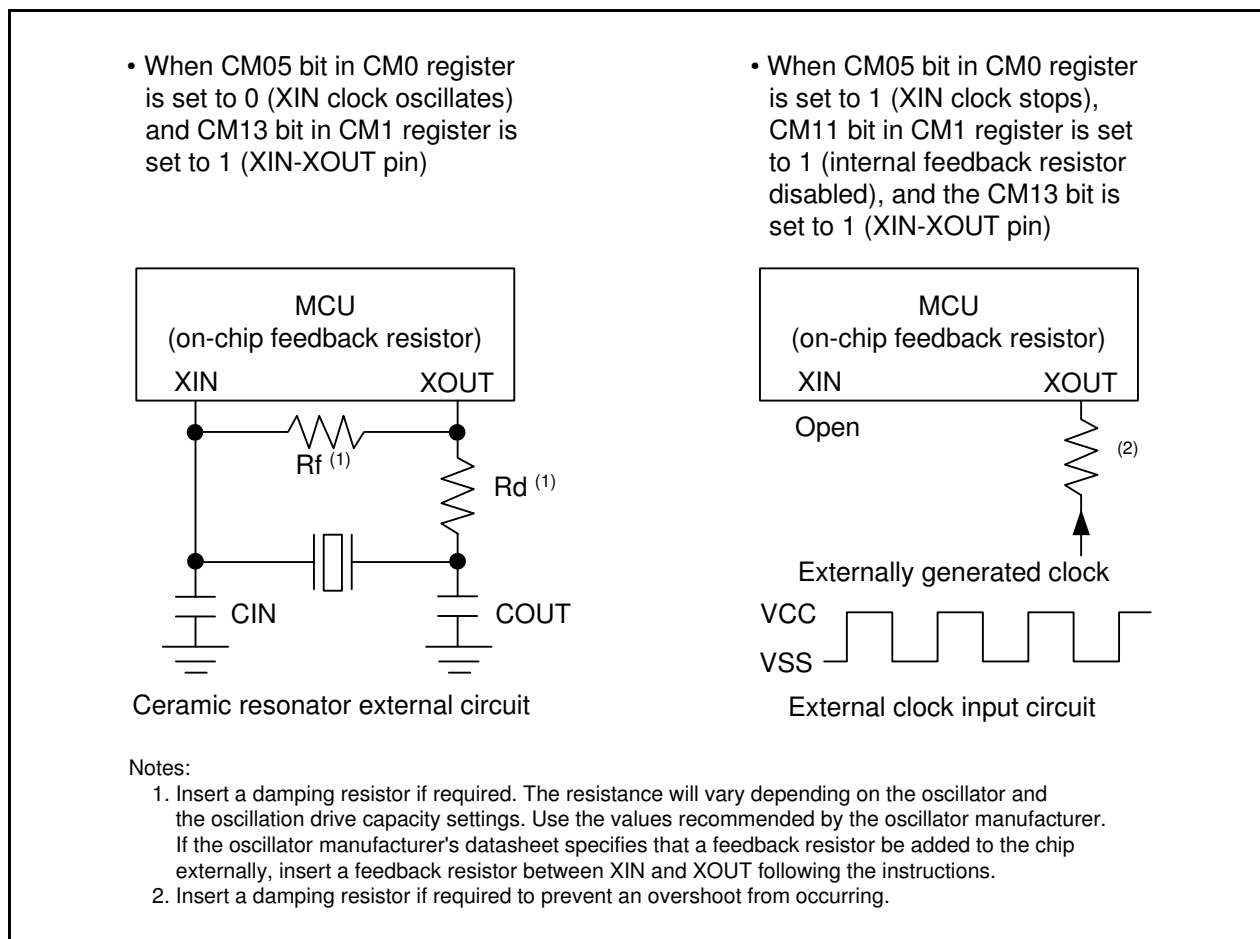


Figure 9.4 Examples of XIN Clock Connection Circuit

## 9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

### 9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-S, and fOCO128.

After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.

If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.

The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

### 9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F, fOCO40M, and fOCO128.

To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All division mode can be set when VCC = 2.7 V to 5.5 V      000b to 111b
- Divide ratio of 8 or more when VCC = 1.8 V to 5.5 V      110b to 111b (divide by 8 or more)

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FRA4 to FRA7.

To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, first transfer the correction value in the FRA4 register to the FRA1 register and the correction value in the FRA5 register to the FRA3 register before using the values. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode (refer to **Table 20.8** and **Table 21.8 Bit Rate Setting Example in UART Mode**).

To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, first transfer the correction value in the FRA6 register to the FRA1 register and the correction value in the FRA7 register to the FRA3 register before using the values.

## 9.5 XCIN Clock

The XCIN clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XCIN clock oscillation circuit is configured by connecting a resonator between the XCIN and XCOUT pins. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XCIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.

Figure 9.5 shows Examples of XCIN Clock Connection Circuits.

During and after a reset, the XCIN clock stops.

After setting the CM04 bit in the CM0 register to 1 (XCIN-XCOUT pin), the XCIN clock starts oscillating when the CM03 bit in the CM0 register is set to 0 (XCIN clock oscillates). After the XCIN clock oscillation stabilizes, the XCIN clock is used as the CPU clock source when the CM07 bit in the CM0 register is set to 1 (XCIN clock). To input an externally generated clock to the XCIN pin, also set the CM04 bit in the CM0 register to 1 (XCIN-XCOUT pin). Leave the XCOUT pin open at this time.

This MCU has an on-chip feedback resistor, which can be disabled/enabled by the CM12 bit in the CM1 register. In stop mode, all clocks including the XCIN clock stop. Refer to **9.7 Power Control** for details.

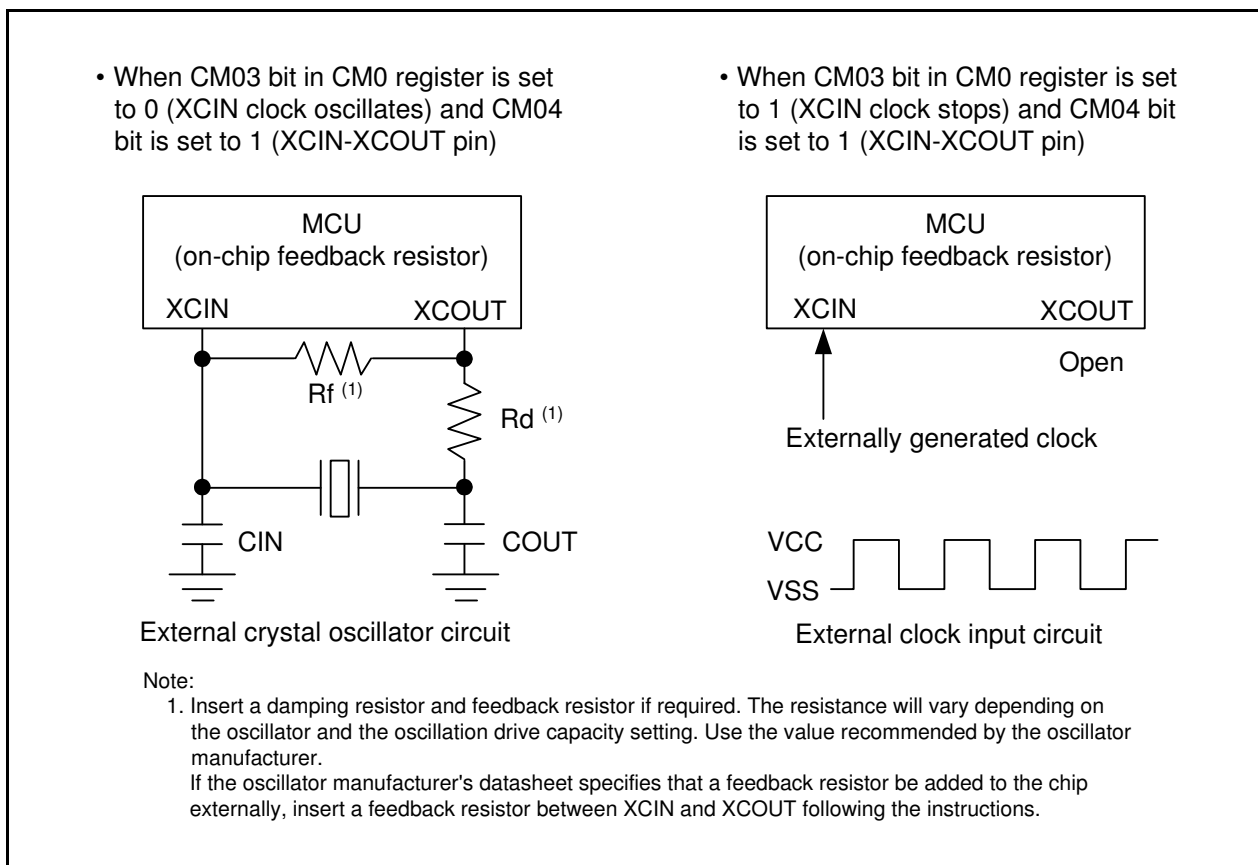


Figure 9.5 Examples of XCIN Clock Connection Circuits

## 9.6 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 9.1 Clock Generation Circuit (With XIN and XCIN Pins Shared)**.

### 9.6.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock, the XCIN clock, or the on-chip oscillator clock can be selected.

### 9.6.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.

The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register to select the value of the division.

Also, use the XCIN clock while the XCIN clock oscillation stabilizes.

After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.

When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

### 9.6.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.

The  $f_i$  ( $i = 1, 2, 4, 8, \text{ and } 32$ ) clock is generated by the system clock divided by  $i$ . It is used for timers RA, RB, RC, RE, the serial interface, and the A/D converter.

If the MCU enters wait mode after the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode), the  $f_i$  clock stops.

### 9.6.4 fOCO

fOCO is an operating clock for the peripheral functions.

This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA.

In wait mode, the fOCO clock does not stop.

### 9.6.5 fOCO40M

fOCO40M is used as the count source for timer RC.

This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.

In wait mode, the fOCO40M clock does not stop.

This clock can be used with supply voltage  $V_{CC} = 2.7$  to 5.5 V.

### 9.6.6 fOCO-F

fOCO-F is used as the count source for timer RC and the A/D converter.

fOCO-F is a clock generated by the high-speed on-chip oscillator and divided by  $i$  ( $i = 2, 3, 4, 5, 6, 7, 8, \text{ and } 9$ ; divide ratio selected by the FRA2 register). This clock is supplied by setting the FRA00 bit to 1.

In wait mode, the fOCO-F clock does not stop.



### 9.6.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.

This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).

In wait mode, the fOCO-S clock does not stop.

### 9.6.8 fOCO128

fOCO128 is a clock generated by dividing fOCO-S or fOCO-F by 128. When the FRA03 bit is set to 0, fOCO-S divided by 128 is selected. When this bit is set to 1, fOCO-F divided by 128 is selected.

fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

### 9.6.9 fC, fC2, fC4, and fC32

fC, fC2, fC4, and fC32 are used for timers RA, RE, and the serial interface.

Use these clocks while the XCIN clock oscillation stabilizes.

### 9.6.10 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.

This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protect mode enabled).

In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

## 9.7 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

### 9.7.1 Standard Operating Mode

Standard operating mode is further separated into four modes.

In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

**Table 9.2 Settings and Modes of Clock Associated Bits**

| Modes                              |              | OCD Register | CM1 Register |      |      | CM0 Register |      |      |      |      | FRA0 Register |       |
|------------------------------------|--------------|--------------|--------------|------|------|--------------|------|------|------|------|---------------|-------|
|                                    |              | OCD2         | CM17, CM16   | CM14 | CM13 | CM07         | CM06 | CM05 | CM04 | CM03 | FRA01         | FRA00 |
| High-speed clock mode              | No division  | 0            | 00b          | –    | 1    | 0            | 0    | 0    | –    | –    | –             | –     |
|                                    | Divide-by-2  | 0            | 01b          | –    | 1    | 0            | 0    | 0    | –    | –    | –             | –     |
|                                    | Divide-by-4  | 0            | 10b          | –    | 1    | 0            | 0    | 0    | –    | –    | –             | –     |
|                                    | Divide-by-8  | 0            | –            | –    | 1    | 0            | 1    | 0    | –    | –    | –             | –     |
|                                    | Divide-by-16 | 0            | 11b          | –    | 1    | 0            | 0    | 0    | –    | –    | –             | –     |
| Low-speed clock mode               | No division  | –            | 00b          | –    | –    | 1            | 0    | –    | 1    | 0    | –             | –     |
|                                    | Divide-by-2  | –            | 01b          | –    | –    | 1            | 0    | –    | 1    | 0    | –             | –     |
|                                    | Divide-by-4  | –            | 10b          | –    | –    | 1            | 0    | –    | 1    | 0    | –             | –     |
|                                    | Divide-by-8  | –            | –            | –    | –    | 1            | 1    | –    | 1    | 0    | –             | –     |
|                                    | Divide-by-16 | –            | 11b          | –    | –    | 1            | 0    | –    | 1    | 0    | –             | –     |
| High-speed on-chip oscillator mode | No division  | 1            | 00b          | –    | –    | 0            | 0    | –    | –    | –    | 1             | 1     |
|                                    | Divide-by-2  | 1            | 01b          | –    | –    | 0            | 0    | –    | –    | –    | 1             | 1     |
|                                    | Divide-by-4  | 1            | 10b          | –    | –    | 0            | 0    | –    | –    | –    | 1             | 1     |
|                                    | Divide-by-8  | 1            | –            | –    | –    | 0            | 1    | –    | –    | –    | 1             | 1     |
|                                    | Divide-by-16 | 1            | 11b          | –    | –    | 0            | 0    | –    | –    | –    | 1             | 1     |
| Low-speed on-chip oscillator mode  | No division  | 1            | 00b          | 0    | –    | 0            | 0    | –    | –    | –    | 0             | –     |
|                                    | Divide-by-2  | 1            | 01b          | 0    | –    | 0            | 0    | –    | –    | –    | 0             | –     |
|                                    | Divide-by-4  | 1            | 10b          | 0    | –    | 0            | 0    | –    | –    | –    | 0             | –     |
|                                    | Divide-by-8  | 1            | –            | 0    | –    | 0            | 1    | –    | –    | –    | 0             | –     |
|                                    | Divide-by-16 | 1            | 11b          | 0    | –    | 0            | 0    | –    | –    | –    | 0             | –     |

–: Indicates that either 0 or 1 can be set.

### 9.7.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RA.

Also, if the FRA00 bit is set to 1, fOCO40M can be used for timer RC.

If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

### 9.7.1.2 Low-Speed Clock Mode

The XCIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock.

In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8, low-current-consumption read mode can be used. However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Also, if the FRA00 bit is set to 1, fOCO40M can be used for timer RC.

If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).

To reduce the power consumption, refer to **25. Reducing Power Consumption**.

### 9.7.1.3 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.

Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

### 9.7.1.4 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.

Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).

To reduce the power consumption, refer to **25. Reducing Power Consumption**.

## 9.7.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operating with the CPU clock and the watchdog timer when count source protection mode is disabled stop. Since the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.

### 9.7.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

### 9.7.2.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).

If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

Enter wait mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

### 9.7.2.3 Pin Status in Wait Mode

The I/O port retains the status immediately before the MCU enters wait mode.

### 9.7.2.4 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt.

The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), the peripheral function interrupts other than A/D conversion interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop and the peripheral functions operating with external signals or the on-chip oscillator clock can be used to exit wait mode.

Table 9.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

**Table 9.3 Interrupts to Exit Wait Mode and Usage Conditions**

| Interrupt                            | CM02 = 0  | CM02 = 1  |
|--------------------------------------|---|---|
| Serial interface interrupt           | Usable when operating with internal or external clock | Usable when operating with external clock   |
| Key input interrupt                  | Usable  | Usable  |
| A/D conversion interrupt             | (Do not use)  | (Do not use)  |
| Timer RA interrupt                   | Usable in all modes                                   | Usable if there is no filter in event counter mode.<br>Usable by selecting fOCO, fC, or fC32 as count source.               |
| Timer RB interrupt                   | Usable in all modes                                   | (Do not use)  |
| Timer RC interrupt                   | Usable in all modes                                   | (Do not use)  |
| Timer RE interrupt                   | Usable in all modes                                   | Usable when operating in real time clock mode   |
| $\overline{\text{INT}}$ interrupt    | Usable  | Usable ( $\overline{\text{INT0}}$ , $\overline{\text{INT1}}$ , $\overline{\text{INT3}}$ can be used if there is no filter.) |
| Voltage monitor 1 interrupt          | Usable  | Usable  |
| Voltage monitor 2 interrupt          | Usable  | Usable  |
| Oscillation stop detection interrupt | Usable  | (Do not use)  |

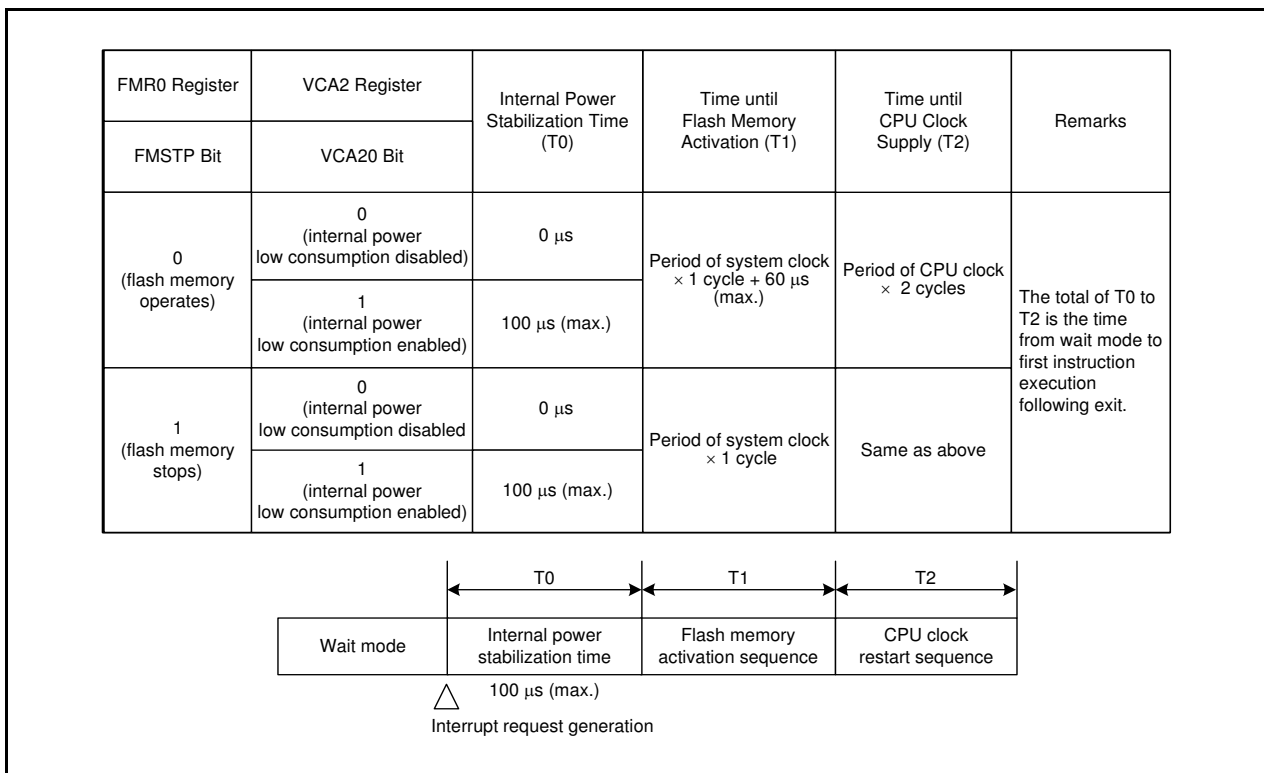
Figure 9.6 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).

To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.

- (1) Set the I flag to 0 (maskable interrupt disabled).
- (2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
- (3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.6.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.



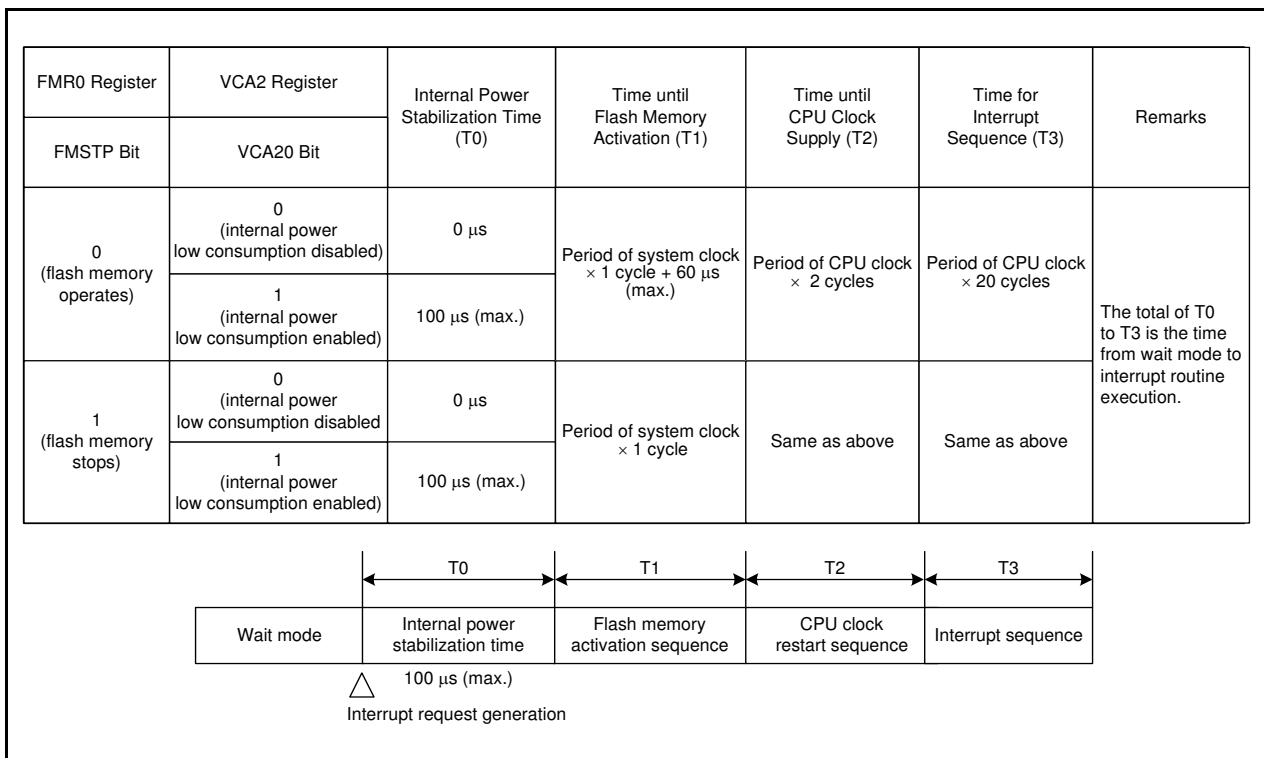
**Figure 9.6 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)**

Figure 9.7 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed. To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

- (1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
- (2) Set the I flag to 1.
- (3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.7.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.



**Figure 9.7 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed**

### 9.7.3 Stop Mode

Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is V<sub>RAM</sub> or more, the contents of internal RAM is retained.

The peripheral functions clocked by external signals continue operating.

Table 9.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

**Table 9.4 Interrupts to Exit Stop Mode and Usage Conditions**

| Interrupt  | Usage Conditions  |
|--|---|
| Key input interrupt  | Usable  |
| $\overline{\text{INT0}}$ , $\overline{\text{INT1}}$ , $\overline{\text{INT3}}$ interrupt | Usable if there is no filter  |
| Timer RA interrupt   | Usable if there is no filter when external pulse is counted in event counter mode |
| Serial interface interrupt   | When external clock selected  |
| Voltage monitor 1 interrupt  | Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)   |
| Voltage monitor 2 interrupt  | Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)   |

#### 9.7.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).

To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

#### 9.7.3.2 Pin Status in Stop Mode

The I/O port retains the status before the MCU enters stop mode.

However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT(P4\_7) pin is held "H". When the CM13 bit is set to 0 (input ports P4\_6 and P4\_7), the P4\_7(XOUT pin) is held in an input status.



### 9.7.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.

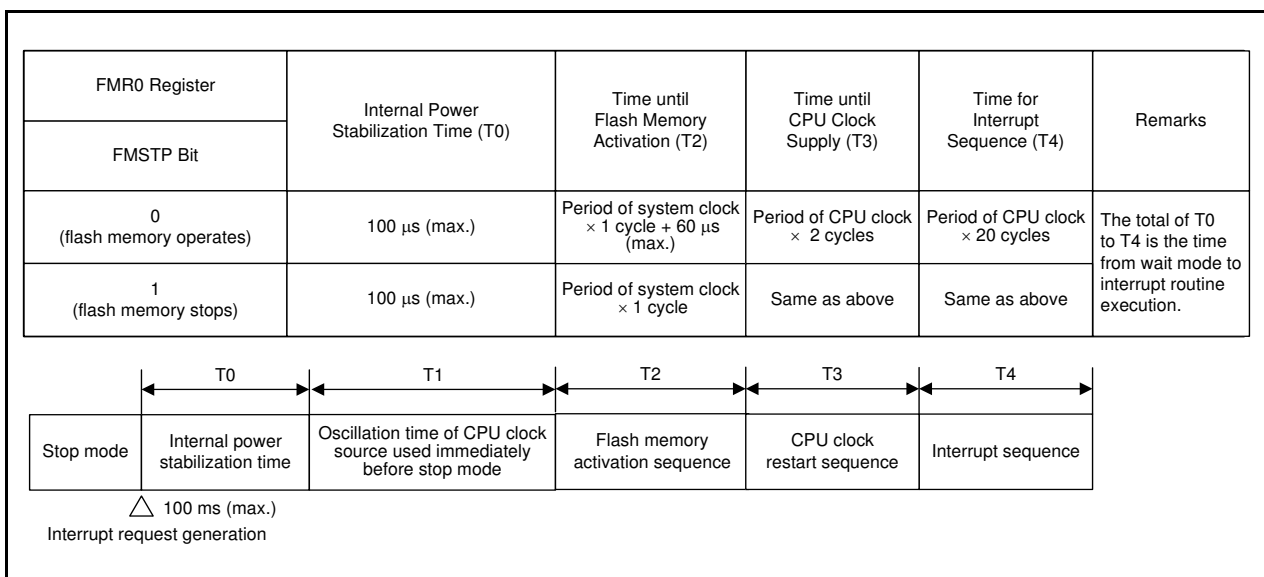
Figure 9.8 shows the Time from Stop Mode to Interrupt Routine Execution.

To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

- (1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
- (2) Set the I flag to 1.
- (3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)



**Figure 9.8 Time from Stop Mode to Interrupt Routine Execution**

Figure 9.9 shows the State Transitions in Power Control Mode.

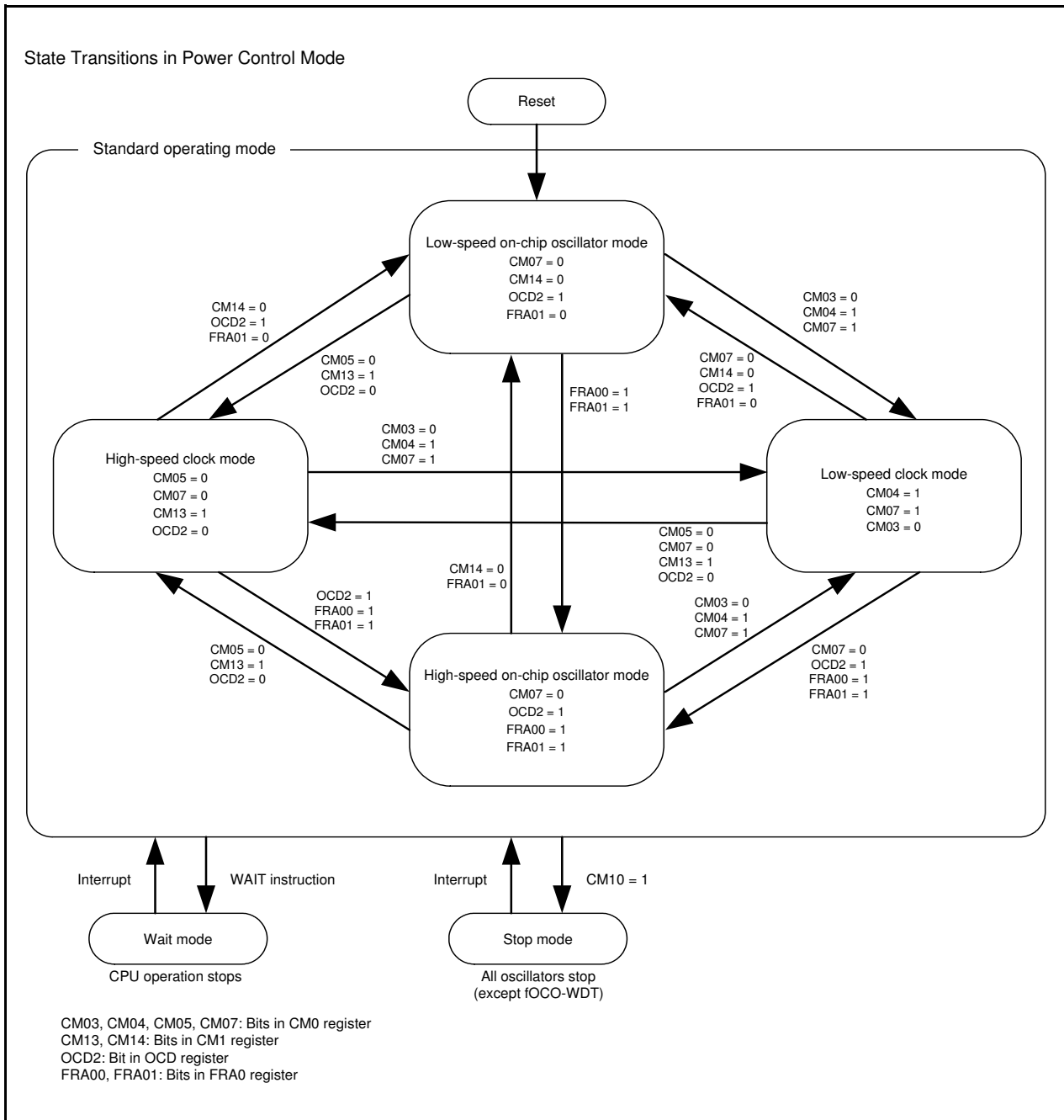


Figure 9.9 State Transitions in Power Control Mode

## 9.8 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.

The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.

Table 9.5 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

**Table 9.5 Specifications of Oscillation Stop Detection Function**

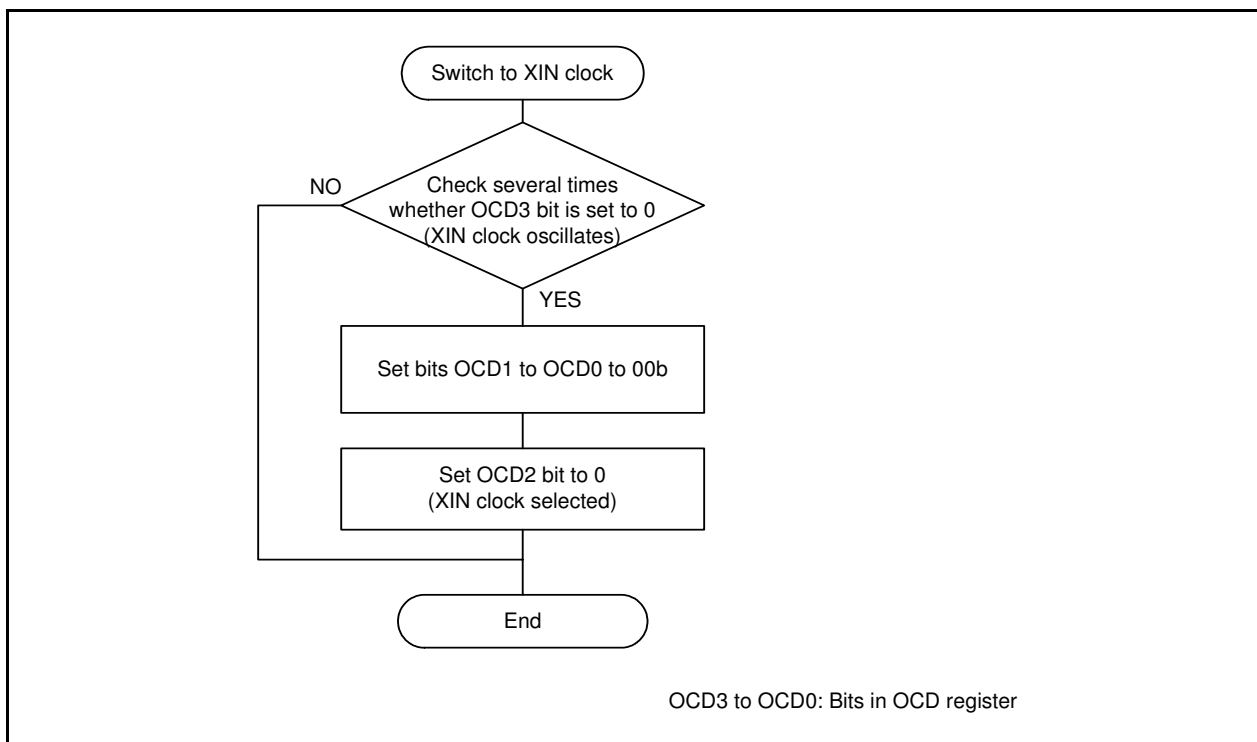
| Item  | Specification                                  |
|---|--|
| Oscillation stop detection clock and frequency bandwidth  | $f(\text{XIN}) \geq 2 \text{ MHz}$             |
| Enabled condition for oscillation stop detection function | Bits OCD1 to OCD0 set to 11b                   |
| Operation at oscillation stop detection                   | Oscillation stop detection interrupt generated |

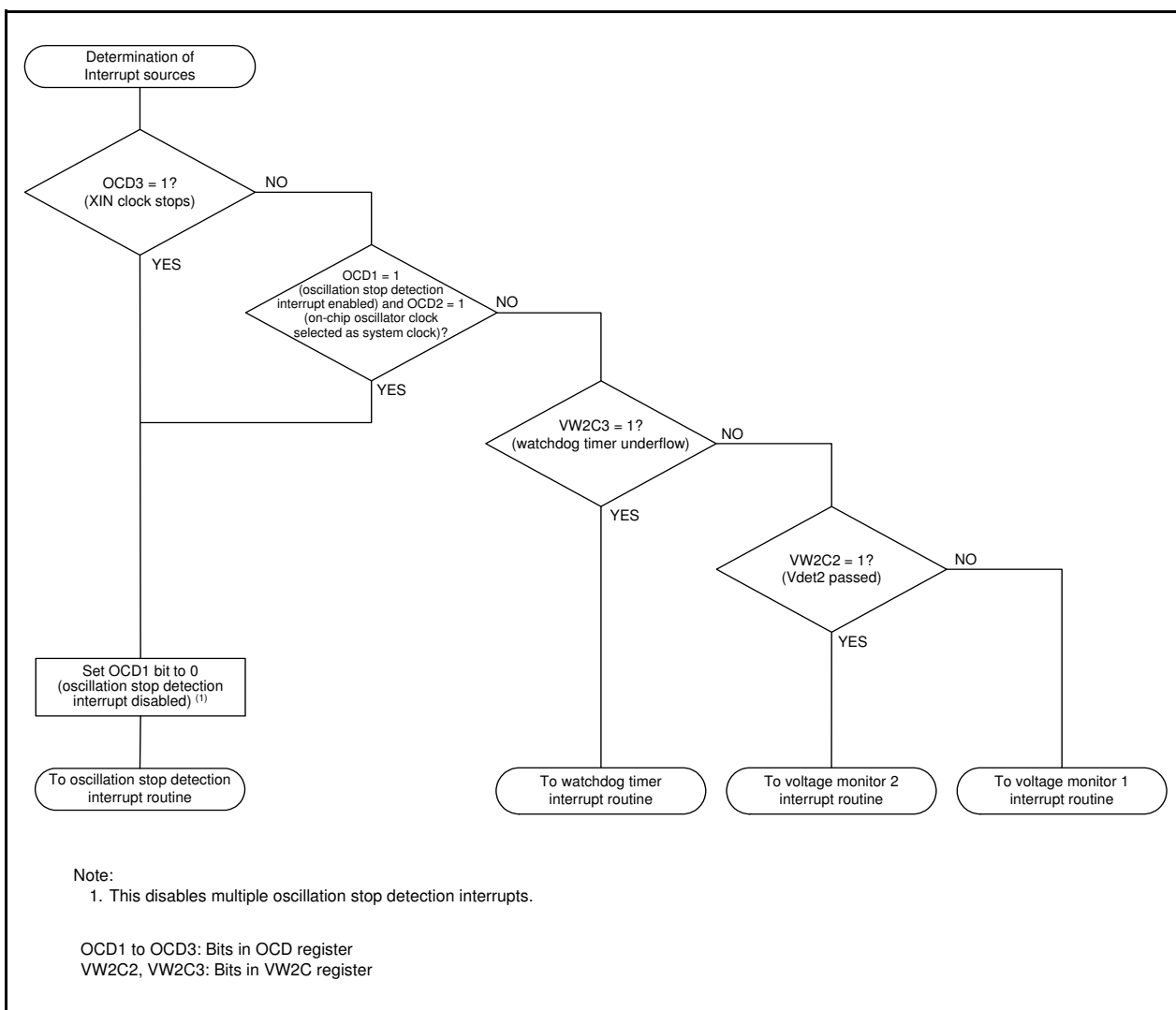
### 9.8.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.  
Table 9.6 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.11 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.  
Figure 9.10 shows the Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while the oscillation stop detection function is used, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and bits OCD1 to OCD0 to 11b.  
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator oscillates) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

**Table 9.6 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt**

| Generated Interrupt Source                 | Bit Indicating Interrupt Source                              |
|--|--|
| Oscillation stop detection<br>((a) or (b)) | (a) OCD3 bit in OCD register = 1                             |
|  | (b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1 |
| Watchdog timer                             | VW2C3 bit in VW2C register = 1                               |
| Voltage monitor 1                          | VW1C2 bit in VW1C register = 1                               |
| Voltage monitor 2                          | VW2C2 bit in VW2C register = 1                               |

**Figure 9.10 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock**



**Figure 9.11 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt**

## 9.9 Notes on Clock Generation Circuit

### 9.9.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.

Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```

BCLR    1, FMR0    ; CPU rewrite mode disabled
BCLR    7, FMR2    ; Low-current-consumption read mode disabled
BSET    0, PRCR    ; Writing to CM1 register enabled
FSET    I         ; Enable interrupt
BSET    0, CM1     ; Stop mode
JMP.B   LABEL_001
LABEL_001:
NOP
NOP
NOP
NOP

```

### 9.9.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.

To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```

BCLR    1, FMR0    ; CPU rewrite mode disabled
BCLR    7, FMR2    ; Low-current-consumption read mode disabled
FSET    I         ; Enable interrupt
WAIT    ; Wait mode
NOP
NOP
NOP
NOP

```

- Program example to execute the instruction to set the CM30 bit to 1

```

BCLR    1, FMR0    ; CPU rewrite mode disabled
BCLR    7, FMR2    ; Low-current-consumption read mode disabled
BSET    0, PRCR    ; Writing to CM3 register enabled
FCLR    I         ; Interrupt disabled
BSET    0, CM3     ; Wait mode
NOP
NOP
NOP
NOP
BCLR    0, PRCR    ; Writing to CM3 register disabled
FSET    I         ; Enable interrupt

```

### 9.9.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

### 9.9.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system. To use the MCU with supply voltage below  $VCC = 2.7$  V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled) and connect the feedback resistor to the chip externally.



## 10. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control.

The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C

### 10.1 Register

#### 10.1.1 Protect Register (PRCR)

Address 000Ah

| Bit         | b7 | b6 | b5 | b4 | b3   | b2   | b1   | b0   |
|-------------|----|----|----|----|------|------|------|------|
| Symbol      | —  | —  | —  | —  | PRC3 | PRC2 | PRC1 | PRC0 |
| After Reset | 0  | 0  | 0  | 0  | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | PRC0   | Protect bit 0   | Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.<br>0: Write disabled<br>1: Write enabled <sup>(2)</sup> | R/W |
| b1  | PRC1   | Protect bit 1   | Enables writing to registers PM0 and PM1.<br>0: Write disabled<br>1: Write enabled <sup>(2)</sup>                                    | R/W |
| b2  | PRC2   | Protect bit 2   | Enables writing to the PD0 register.<br>0: Write disabled<br>1: Write enabled <sup>(1)</sup>   | R/W |
| b3  | PRC3   | Protect bit 3   | Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.<br>0: Write disabled<br>1: Write enabled <sup>(2)</sup>    | R/W |
| b4  | —      | Reserved bits   | Set to 0.  | R/W |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

Notes:

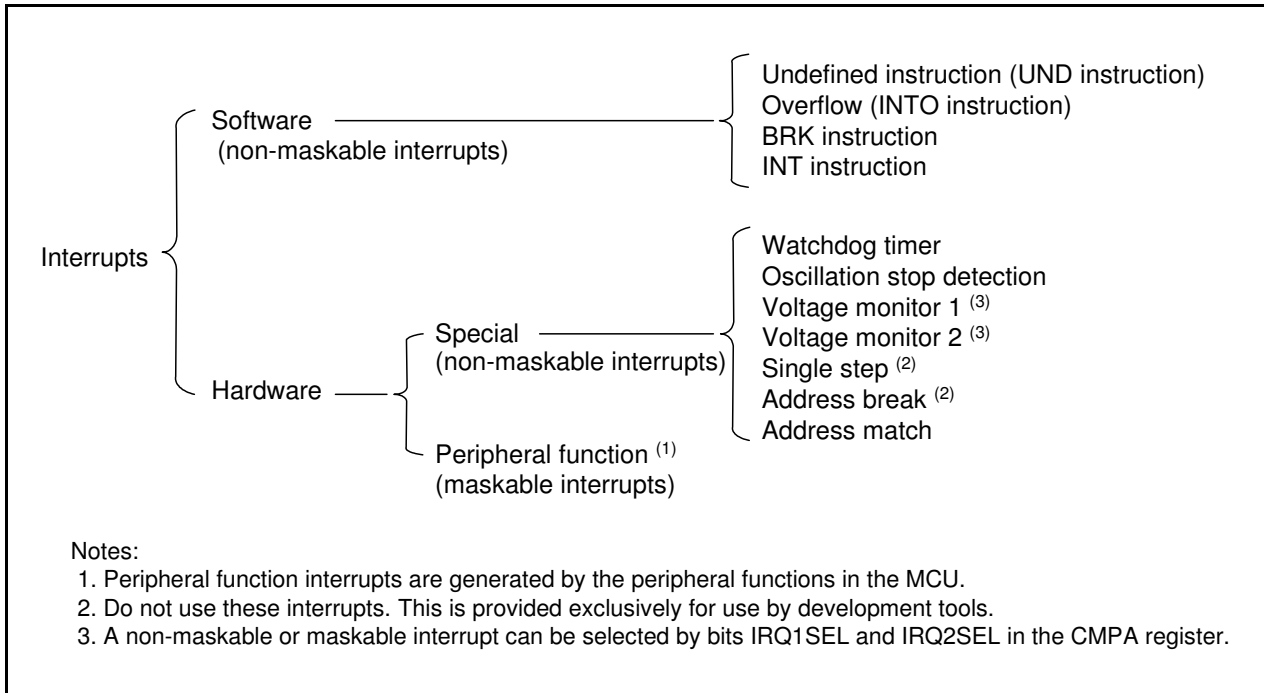
1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

## 11. Interrupts

### 11.1 Overview

#### 11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.



**Figure 11.1** Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

## 11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

### 11.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

### 11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

### 11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

### 11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because some software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.

For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

### 11.1.3 Special Interrupts

Special interrupts are non-maskable.

#### 11.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **14. Watchdog Timer**.

#### 11.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

#### 11.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

#### 11.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

#### 11.1.3.5 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

#### 11.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER0 bit in the AIER register or the AIER1 bit is set to 1 (address match interrupt enabled).

For details of the address match interrupt, refer to **11.6 Address Match Interrupt**.

### 11.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 11.2 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

### 11.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

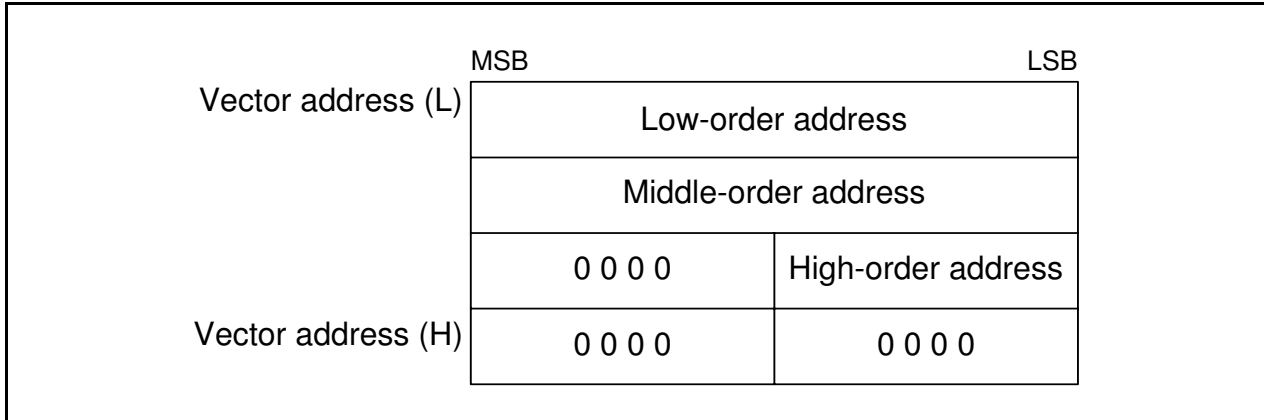


Figure 11.2 Interrupt Vector

#### 11.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.

Table 11.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **24.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 11.1 Fixed Vector Tables

| Interrupt Source   | Vector Addresses Address (L) to (H) | Remarks   | Reference   |
|--|-------------------------------------|---|---|
| Undefined instruction  | 0FFDCh to 0FFDFh                    | Interrupt with UND instruction  | R8C/Tiny Series Software Manual   |
| Overflow   | 0FFE0h to 0FFE3h                    | Interrupt with INTO instruction   |   |
| BRK instruction  | 0FFE4h to 0FFE7h                    | If the content of address 0FFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table. |   |
| Address match  | 0FFE8h to 0FFEBh                    |   | 11.6 Address Match Interrupt  |
| Single step <sup>(1)</sup>   | 0FFECh to 0FEFh                     |   |   |
| Watchdog timer, Oscillation stop detection, Voltage monitor 1, Voltage monitor 2 | 0FFF0h to 0FFF3h                    |   | 14. Watchdog Timer<br>9. Clock Generation Circuit<br>6. Voltage Detection Circuit |
| Address break <sup>(1)</sup>   | 0FFF4h to 0FFF7h                    |   |   |
| (Reserved)   | 0FFF8h to 0FFFBh                    |   |   |
| Reset  | 0FFFCh to 0FFFFh                    |   | 5. Resets   |

Note:

1. Do not use these interrupts. They are provided exclusively for use by development tools.

### 11.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 11.2 lists the Relocatable Vector Tables.

**Table 11.2 Relocatable Vector Tables**

| Interrupt Source               | Vector Addresses <sup>(1)</sup><br>Address (L) to Address (H)     | Software<br>Interrupt<br>Number | Interrupt Control<br>Register | Reference                          |
|--------------------------------|---|---------------------------------|-------------------------------|------------------------------------|
| BRK instruction <sup>(2)</sup> | +0 to +3 (0000h to 0003h)   | 0                               | –                             | R8C/Tiny Series<br>Software Manual |
| Flash memory ready             | +4 to +7 (0004h to 0007h)   | 1                               | FMRDYIC                       | 24. Flash Memory                   |
| (Reserved)                     |   | 2 to 5                          | –                             | –                                  |
| (Reserved)                     | +24 to +27 (0018h to 001Bh)                                       | 6                               | –                             | –                                  |
| Timer RC                       | +28 to +31 (001Ch to 001Fh)                                       | 7                               | TRCIC                         | 18. Timer RC                       |
| (Reserved)                     | +32 to +35 (0020h to 0023h)                                       | 8                               | –                             | –                                  |
| (Reserved)                     | +36 to +39 (0024h to 0027h)                                       | 9                               | –                             | –                                  |
| Timer RE                       | +40 to +43 (0028h to 002Bh)                                       | 10                              | TREIC                         | 19. Timer RE                       |
| UART2 transmit/NACK2           | +44 to +47 (002Ch to 002Fh)                                       | 11                              | S2TIC                         | 21. Serial Interface<br>(UART2)    |
| UART2 receive/ACK2             | +48 to +51 (0030h to 0033h)                                       | 12                              | S2RIC                         |                                    |
| Key input                      | +52 to +55 (0034h to 0037h)                                       | 13                              | KUPIC                         | 11.5 Key Input Interrupt           |
| A/D conversion                 | +56 to +59 (0038h to 003Bh)                                       | 14                              | ADIC                          | 22. A/D Converter                  |
| (Reserved)                     |   | 15                              | –                             | –                                  |
| (Reserved)                     |   | 16                              | –                             | –                                  |
| UART0 transmit                 | +68 to +71 (0044h to 0047h)                                       | 17                              | S0TIC                         | 20. Serial Interface<br>(UART0)    |
| UART0 receive                  | +72 to +75 (0048h to 004Bh)                                       | 18                              | S0RIC                         |                                    |
| (Reserved)                     |   | 19                              | –                             | –                                  |
| (Reserved)                     |   | 20                              | –                             | –                                  |
| (Reserved)                     |   | 21                              | –                             | –                                  |
| Timer RA                       | +88 to +91 (0058h to 005Bh)                                       | 22                              | TRAIC                         | 16. Timer RA                       |
| (Reserved)                     |   | 23                              | –                             | –                                  |
| Timer RB                       | +96 to +99 (0060h to 0063h)                                       | 24                              | TRBIC                         | 17. Timer RB                       |
| INT1                           | +100 to +103 (0064h to 0067h)                                     | 25                              | INT1IC                        | 11.4 INT Interrupt                 |
| INT3                           | +104 to +107 (0068h to 006Bh)                                     | 26                              | INT3IC                        |                                    |
| (Reserved)                     |   | 27                              | –                             | –                                  |
| (Reserved)                     |   | 28                              | –                             | –                                  |
| INT0                           | +116 to +119 (0074h to 0077h)                                     | 29                              | INT0IC                        | 11.4 INT Interrupt                 |
| UART2 bus collision detection  | +120 to +123 (0078h to 007Bh)                                     | 30                              | U2BCNIC                       | 21. Serial Interface<br>(UART2)    |
| (Reserved)                     |   | 31                              | –                             | –                                  |
| Software <sup>(2)</sup>        | +128 to +131 (0080h to 0083h) to<br>+164 to +167 (00A4h to 00A7h) | 32 to 41                        | –                             | R8C/Tiny Series<br>Software Manual |
| (Reserved)                     |   | 42 to 49                        | –                             | –                                  |
| Voltage monitor 1              | +200 to +203 (00C8h to 00CBh)                                     | 50                              | VCMP1IC                       | 6. Voltage Detection<br>Circuit    |
| Voltage monitor 2              | +204 to +207 (00CCh to 00CFh)                                     | 51                              | VCMP2IC                       |                                    |
| (Reserved)                     |   | 52 to 55                        | –                             | –                                  |
| Software <sup>(2)</sup>        | +224 to +227 (00E0h to 00E3h) to<br>+252 to +255 (00FCh to 00FFh) | 56 to 63                        | –                             | R8C/Tiny Series<br>Software Manual |

Notes:

1. These addresses are relative to those in the INTB register.
2. These interrupts are not disabled by the I flag.

## 11.2 Registers

### 11.2.1 Interrupt Control Register (TREIC, S2TIC, S2RIC, KUPIC, ADIC, S0TIC, S0RIC, TRAIC, TRBIC, U2BCNIC, VCMP1IC, VCMP2IC)

Address 004Ah (TREIC), 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC),  
0051h (S0TIC), 0052h (S0RIC), 0056h (TRAIC), 0058h (TRBIC), 005Eh (U2BCNIC),  
0072h (VCMP1IC), 0073h (VCMP2IC),

|             |    |    |    |    |    |       |       |       |
|-------------|----|----|----|----|----|-------|-------|-------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1    | b0    |
| Symbol      | —  | —  | —  | —  | IR | ILVL2 | ILVL1 | ILVL0 |
| After Reset | X  | X  | X  | X  | X  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name   | Function   | R/W        |
|-----|--------|--|--|------------|
| b0  | ILVL0  | Interrupt priority level select bit  | <sup>b2 b1 b0</sup><br>0 0 0: Level 0 (interrupt disabled)<br>0 0 1: Level 1<br>0 1 0: Level 2<br>0 1 1: Level 3<br>1 0 0: Level 4<br>1 0 1: Level 5<br>1 1 0: Level 6<br>1 1 1: Level 7 | R/W        |
| b1  | ILVL1  |  |  | R/W        |
| b2  | ILVL2  |  |  | R/W        |
|     |        |  |  |            |
| b3  | IR     | Interrupt request bit  | 0: No interrupt requested<br>1: Interrupt requested  | R/W<br>(1) |
| b4  | —      | Nothing is assigned. If necessary, set to 0.<br>When read, the content is undefined. |  | —          |
| b5  | —      |  |  |            |
| b6  | —      |  |  |            |
| b7  | —      |  |  |            |

Note:

- Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated.  
Refer to **11.8.5 Rewriting Interrupt Control Register**.

### 11.2.2 Interrupt Control Register (FMRDYIC, TRCIC)

Address 0041h (FMRDYIC), 0047h (TRCIC)

|             |    |    |    |    |    |       |       |       |
|-------------|----|----|----|----|----|-------|-------|-------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1    | b0    |
| Symbol      | —  | —  | —  | —  | IR | ILVL2 | ILVL1 | ILVL0 |
| After Reset | X  | X  | X  | X  | X  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name   | Function   | R/W                   |
|-----|--------|--|--|-----------------------|
| b0  | ILVL0  | Interrupt priority level select bit  | $b_2 b_1 b_0$<br>0 0 0: Level 0 (interrupt disabled)<br>0 0 1: Level 1<br>0 1 0: Level 2<br>0 1 1: Level 3<br>1 0 0: Level 4<br>1 0 1: Level 5<br>1 1 0: Level 6<br>1 1 1: Level 7 | R/W                   |
| b1  | ILVL1  |  |  | R/W                   |
| b2  | ILVL2  |  |  | R/W                   |
| b3  | IR     |  |  | Interrupt request bit |
| b4  | —      | Nothing is assigned. If necessary, set to 0.<br>When read, the content is undefined. |  | —                     |
| b5  | —      |  |  |                       |
| b6  | —      |  |  |                       |
| b7  | —      |  |  |                       |

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.



### 11.2.3 INT<sub>i</sub> Interrupt Control Register (INT<sub>i</sub>IC) (i = 0, 1, 3)

Address 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

|             |    |    |    |     |    |       |       |       |
|-------------|----|----|----|-----|----|-------|-------|-------|
| Bit         | b7 | b6 | b5 | b4  | b3 | b2    | b1    | b0    |
| Symbol      | —  | —  | —  | POL | IR | ILVL2 | ILVL1 | ILVL0 |
| After Reset | X  | X  | 0  | 0   | X  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name                                     | Function   | R/W                   |
|-----|--------|--|--|-----------------------|
| b0  | ILVL0  | Interrupt priority level select bit          | <sup>b2 b1 b0</sup><br>0 0 0: Level 0 (interrupt disabled)<br>0 0 1: Level 1<br>0 1 0: Level 2<br>0 1 1: Level 3<br>1 0 0: Level 4<br>1 0 1: Level 5<br>1 1 0: Level 6<br>1 1 1: Level 7 | R/W                   |
| b1  | ILVL1  |  |  | R/W                   |
| b2  | ILVL2  |  |  | R/W                   |
| b3  | IR     |  |  | Interrupt request bit |
| b4  | POL    | Polarity switch bit <sup>(3)</sup>           | 0: Falling edge selected<br>1: Rising edge selected <sup>(2)</sup>   | R/W                   |
| b5  | —      | Reserved bit                                 | Set to 0.  | R/W                   |
| b6  | —      | Nothing is assigned. If necessary, set to 0. |  | —                     |
| b7  | —      | When read, the content is undefined.         |  | —                     |

Notes:

- Only 0 can be written to the IR bit. Do not write 1 to this bit.
- If the INT<sub>i</sub>PL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
- The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

### 11.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.

Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

#### 11.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

#### 11.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).

The IR bit can be set to 0 by a program. Do not write 1 to this bit.

However, the IR bit operations of the timer RC interrupt, and the flash memory interrupt are different. Refer to **11.7 Timer RC Interrupt and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

#### 11.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.


Table 11.3 lists the Settings of Interrupt Priority Levels and Table 11.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

**Table 11.3 Settings of Interrupt Priority Levels**

| Bits ILVL2 to ILVL0 | Interrupt Priority Level     | Priority   |
|---------------------|------------------------------|--|
| 000b                | Level 0 (interrupt disabled) | —  |
| 001b                | Level 1                      | Low<br><br>High |
| 010b                | Level 2                      |  |
| 011b                | Level 3                      |  |
| 100b                | Level 4                      |  |
| 101b                | Level 5                      |  |
| 110b                | Level 6                      |  |
| 111b                | Level 7                      |  |

**Table 11.4 Interrupt Priority Levels Enabled by IPL**

| IPL  | Enabled Interrupt Priority Level     |
|------|--------------------------------------|
| 000b | Interrupt level 1 and above          |
| 001b | Interrupt level 2 and above          |
| 010b | Interrupt level 3 and above          |
| 011b | Interrupt level 4 and above          |
| 100b | Interrupt level 5 and above          |
| 101b | Interrupt level 6 and above          |
| 110b | Interrupt level 7 and above          |
| 111b | All maskable interrupts are disabled |

### 11.3.4 Interrupt Sequence

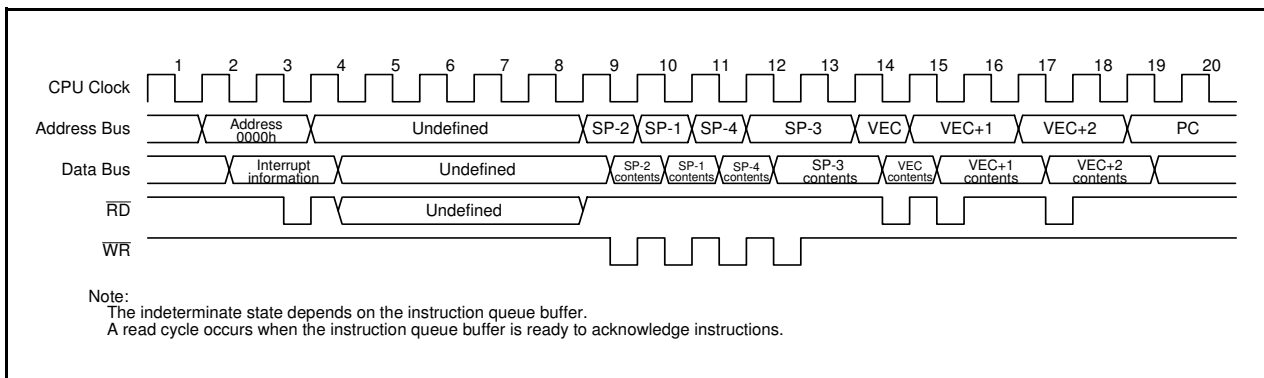
The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.

When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.

Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

- (1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). <sup>(2)</sup>
- (2) The FLG register is saved to a temporary register <sup>(1)</sup> in the CPU immediately before entering the interrupt sequence.
- (3) The I, D and U flags in the FLG register are set as follows:  
 The I flag is set to 0 (interrupts disabled).  
 The D flag is set to 0 (single-step interrupt disabled).  
 The U flag is set to 0 (ISP selected).  
 However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
- (4) The CPU internal temporary register <sup>(1)</sup> is saved on the stack.
- (5) The PC is saved on the stack.
- (6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
- (7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.



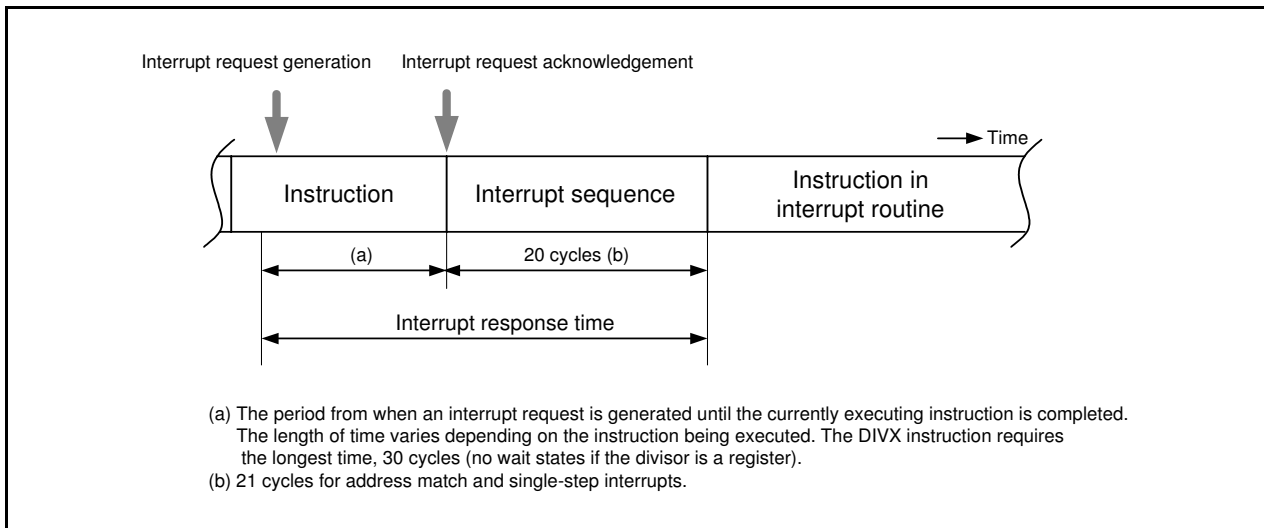
**Figure 11.3 Time Required for Executing Interrupts Sequence**

Notes:

1. These registers cannot be accessed by the user.
2. Refer to **11.7 Timer RC Interrupt and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RC Interrupt.

### 11.3.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 11.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 11.4).



**Figure 11.4** Interrupt Response Time

### 11.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.

When a software interrupt or special interrupt request is acknowledged, the level listed in Table 11.5 is set in the IPL.

Table 11.5 lists the IPL Value When Software or Special Interrupt is Acknowledged.

**Table 11.5** IPL Value When Software or Special Interrupt is Acknowledged

| Interrupt Source without Interrupt Priority Level   | Value Set in IPL |
|---|------------------|
| Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break | 7                |
| Software, address match, single-step  | Not changed      |

### 11.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.

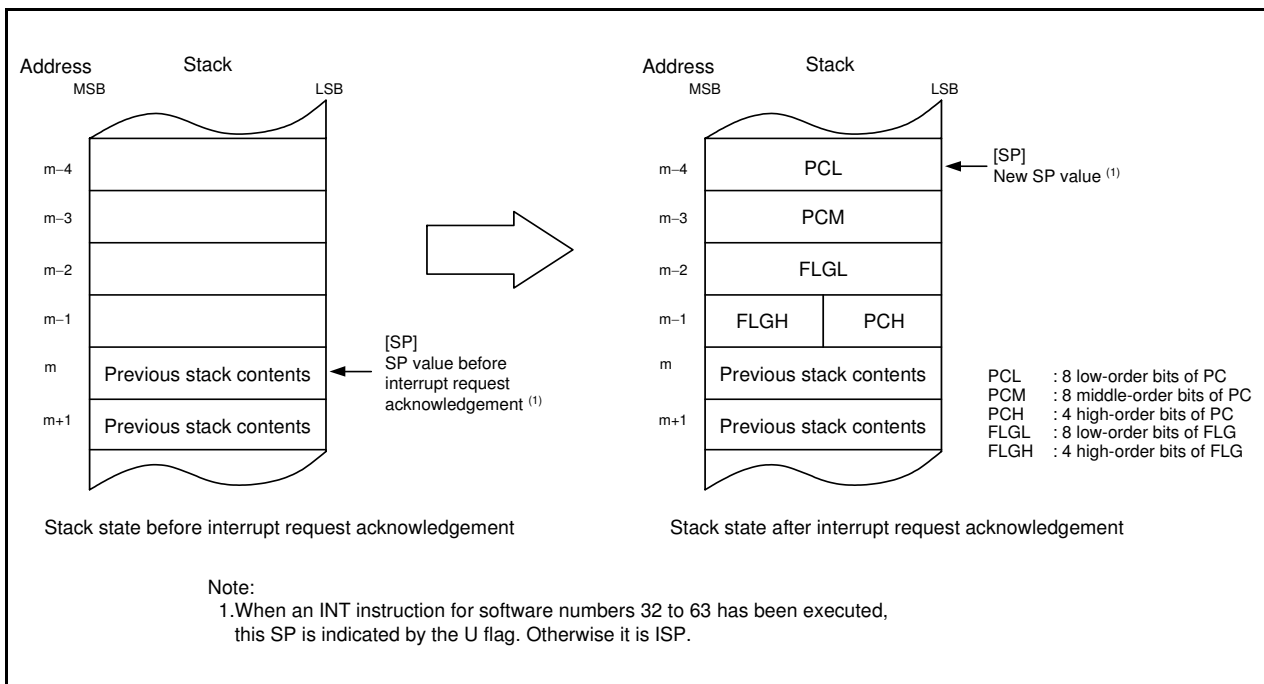
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.

Figure 11.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.

The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used <sup>(1)</sup> with a single instruction.

Note:

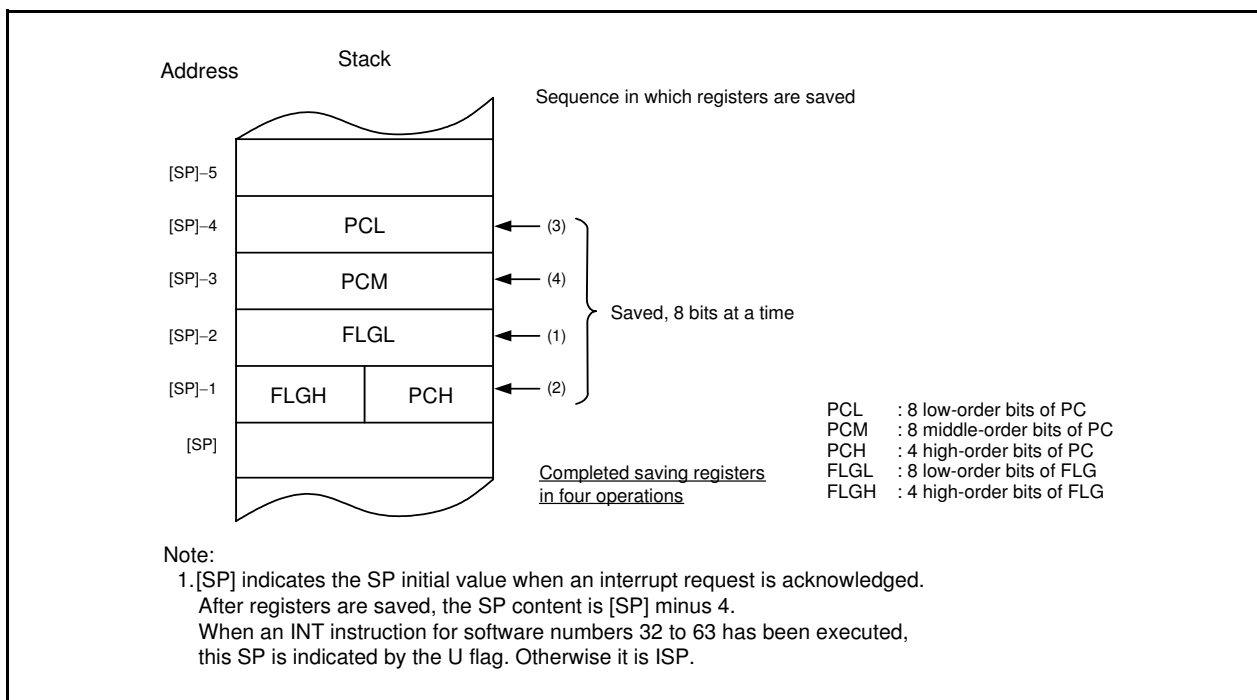
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.



**Figure 11.5 Stack State Before and After Acknowledgement of Interrupt Request**

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.

Figure 11.6 shows the Register Saving Operation.



**Figure 11.6 Register Saving Operation**

### 11.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

### 11.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of watchdog timer and other special interrupts is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, the MCU executes the interrupt routine.

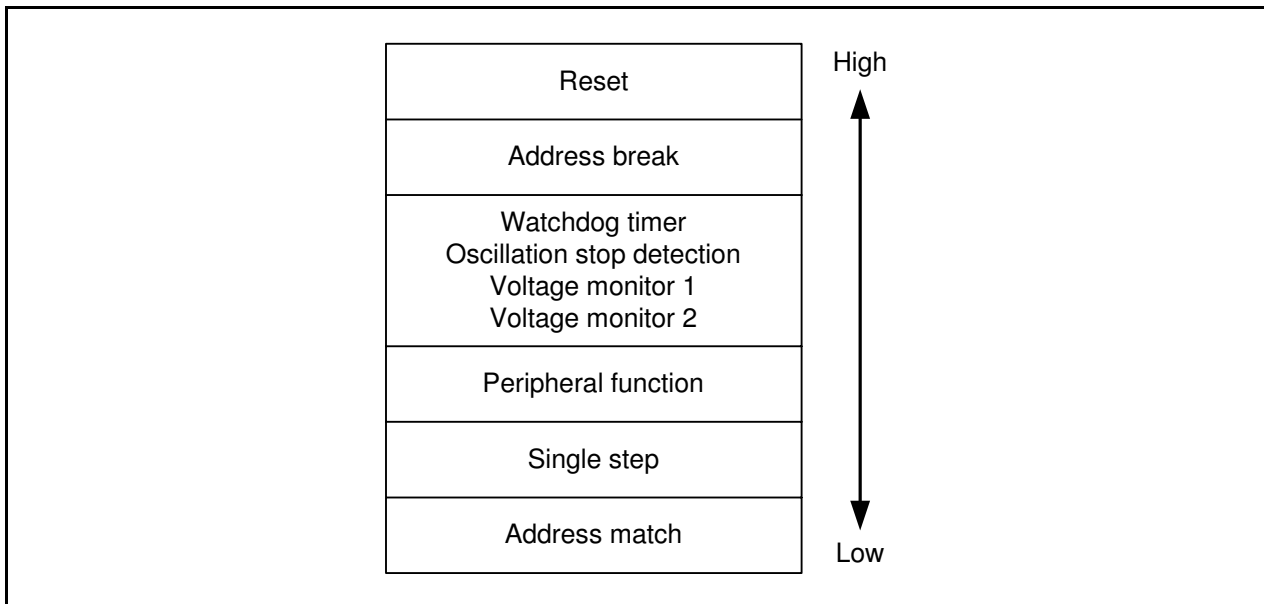


Figure 11.7 Hardware Interrupt Priority

### 11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

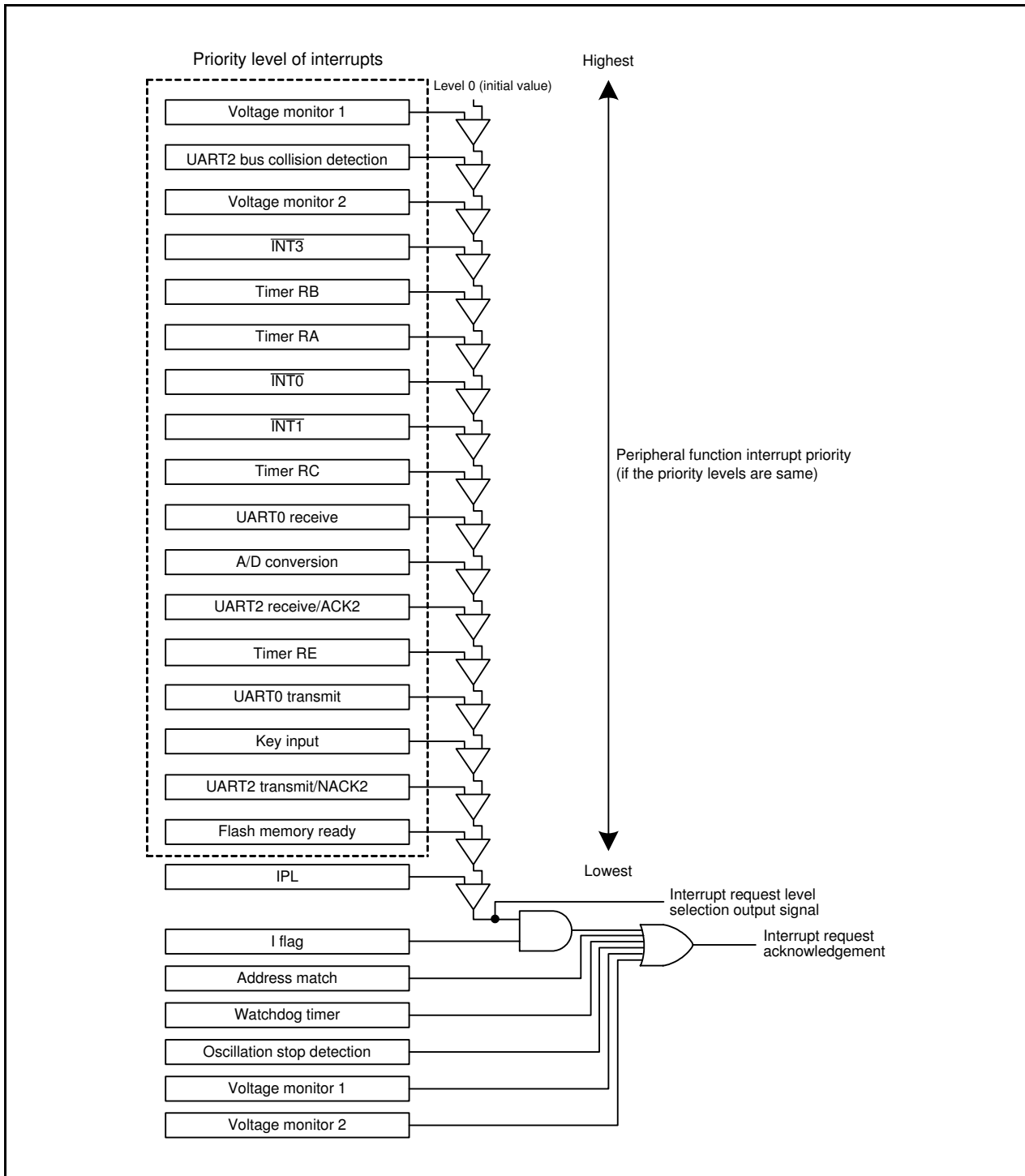


Figure 11.8 Interrupt Priority Level Selection Circuit



## 11.4 $\overline{\text{INT}}$ Interrupt

### 11.4.1 $\overline{\text{INT}}_i$ Interrupt (i = 0, 1, 3)

The  $\overline{\text{INT}}_i$  interrupt is generated by an  $\overline{\text{INT}}_i$  input. To use the  $\overline{\text{INT}}_i$  interrupt, set the  $\text{INT}_i\text{EN}$  bit in the  $\text{INTEN}$  register is to 1 (enabled). The edge polarity is selected using the  $\text{INT}_i\text{PL}$  bit in the  $\text{INTEN}$  register and the  $\text{POL}$  bit in the  $\text{INT}_i\text{IC}$  register. The input pins used as the  $\overline{\text{INT}}_i$  input can be selected.

Also, inputs can be passed through a digital filter with three different sampling clocks.

The  $\overline{\text{INT}}_0$  pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB.

Table 11.6 lists the Pin Configuration of  $\overline{\text{INT}}$  Interrupt.

**Table 11.6 Pin Configuration of  $\overline{\text{INT}}$  Interrupt**

| Pin Name                  | Assigned Pin | I/O   | Function  |
|---------------------------|--------------|-------|---|
| $\overline{\text{INT}}_0$ | P4_5         | Input | $\overline{\text{INT}}_0$ interrupt input, timer RB external trigger input, timer RC pulse output forced cutoff input |
| $\overline{\text{INT}}_1$ | P1_5 or P1_7 | Input | $\overline{\text{INT}}_1$ interrupt input   |
| $\overline{\text{INT}}_3$ | P3_3         | Input | $\overline{\text{INT}}_3$ interrupt input   |

### 11.4.2 $\overline{\text{INT}}$ Interrupt Input Pin Select Register (INTSR)

Address 018Eh

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1       | b0 |
|-------------|----|----|----|----|----|----|----------|----|
| Symbol      | —  | —  | —  | —  | —  | —  | INT1SELO | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0        | 0  |

| Bit | Symbol   | Bit Name  | Function                             | R/W |
|-----|----------|---|--------------------------------------|-----|
| b0  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                      | —   |
| b1  | INT1SELO | $\overline{\text{INT}}_1$ pin select bit                                  | 0: P1_7 assigned<br>1: P1_5 assigned | R/W |
| b2  | —        | Reserved bits   | Set to 0.                            | R/W |
| b3  | —        |   |                                      |     |
| b4  | —        |   |                                      |     |
| b5  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                      | —   |
| b6  | —        | Reserved bits   | Set to 0.                            | R/W |
| b7  | —        |   |                                      |     |

The INTSR register selects which pin is assigned to the  $\overline{\text{INT}}_1$  input. To use  $\overline{\text{INT}}_1$ , set this register.

Set the INTSR register before setting the  $\overline{\text{INT}}_1$  associated registers. Also, do not change the setting values in this register during  $\overline{\text{INT}}_1$  operation.

### 11.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

| Bit         | b7     | b6     | b5 | b4 | b3     | b2     | b1     | b0     |
|-------------|--------|--------|----|----|--------|--------|--------|--------|
| Symbol      | INT3PL | INT3EN | —  | —  | INT1PL | INT1EN | INT0PL | INT0EN |
| After Reset | 0      | 0      | 0  | 0  | 0      | 0      | 0      | 0      |

| Bit | Symbol | Bit Name  | Function                     | R/W |
|-----|--------|---|------------------------------|-----|
| b0  | INT0EN | $\overline{\text{INT0}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b1  | INT0PL | $\overline{\text{INT0}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |
| b2  | INT1EN | $\overline{\text{INT1}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b3  | INT1PL | $\overline{\text{INT1}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |
| b4  | —      | Reserved bits   | Set to 0.                    | R/W |
| b5  | —      |   |                              |     |
| b6  | INT3EN | $\overline{\text{INT3}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b7  | INT3PL | $\overline{\text{INT3}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |

Notes:

1. To set the INT<sub>i</sub>PL bit (i = 0, 1, 3) to 1 (both edges), set the POL bit in the INT<sub>i</sub>IC register to 0 (falling edge selected).
2. The IR bit in the INT<sub>i</sub>IC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

### 11.4.4 INT Input Filter Select Register 0 (INTF)

Address 01FCh

| Bit         | b7     | b6     | b5 | b4 | b3     | b2     | b1     | b0     |
|-------------|--------|--------|----|----|--------|--------|--------|--------|
| Symbol      | INT3F1 | INT3F0 | —  | —  | INT1F1 | INT1F0 | INT0F1 | INT0F0 |
| After Reset | 0      | 0      | 0  | 0  | 0      | 0      | 0      | 0      |

| Bit | Symbol | Bit Name   | Function   | R/W |
|-----|--------|--|--|-----|
| b0  | INT0F0 | $\overline{\text{INT0}}$ input filter select bit | b1 b0<br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b1  | INT0F1 |  |  | R/W |
| b2  | INT1F0 | $\overline{\text{INT1}}$ input filter select bit | b3 b2<br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b3  | INT1F1 |  |  | R/W |
| b4  | —      | Reserved bits                                    | Set to 0.  | R/W |
| b5  | —      |  |  |     |
| b6  | INT3F0 | $\overline{\text{INT3}}$ input filter select bit | b7 b6<br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b7  | INT3F1 |  |  | R/W |

### 11.4.5 $\overline{\text{INT}}_i$ Input Filter (i = 0, 1, 3)

The  $\overline{\text{INT}}_i$  input contains a digital filter. The sampling clock is selected using bits  $\text{INTiF1}$  and  $\text{INTiF0}$  in the  $\text{INTF}$  register. The  $\overline{\text{INT}}_i$  level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the  $\text{INTiIC}$  register is set to 1 (interrupt requested).

Figure 11.9 shows the  $\overline{\text{INT}}_i$  Input Filter Configuration. Figure 11.10 shows an Operating Example of  $\overline{\text{INT}}_i$  Input Filter.

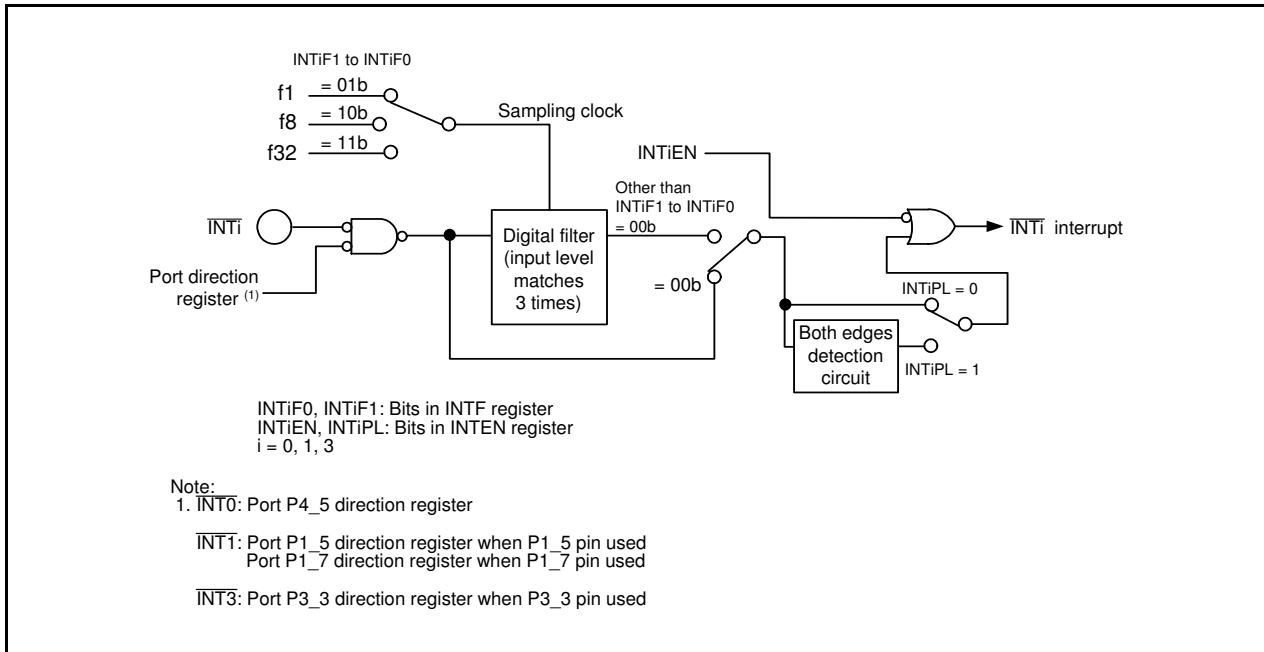


Figure 11.9  $\overline{\text{INT}}_i$  Input Filter Configuration

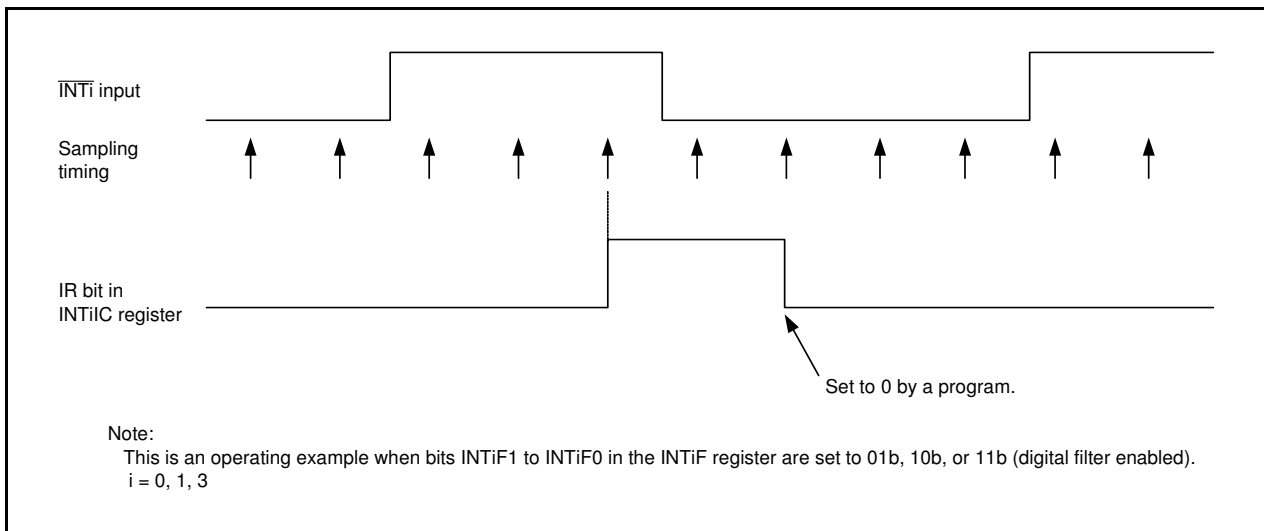


Figure 11.10 Operating Example of  $\overline{\text{INT}}_i$  Input Filter

## 11.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins  $\overline{K10}$  to  $\overline{K13}$ . The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The  $KIiEN$  ( $i = 0$  to  $3$ ) bit in the  $KIEN$  register is used to select whether or not the pins are used as the  $\overline{KIi}$  input. The  $KIiPL$  bit in the  $KIEN$  register is also used to select the input polarity.

When inputting “L” to the  $\overline{KIi}$  pin, which sets the  $KIiPL$  bit to 0 (falling edge), the input to the other pins  $\overline{K10}$  to  $\overline{K13}$  is not detected as interrupts. When inputting “H” to the  $\overline{KIi}$  pin, which sets the  $KIiPL$  bit to 1 (rising edge), the input to the other pins  $\overline{K10}$  to  $\overline{K13}$  is not also detected as interrupts.

Figure 11.11 shows a Block Diagram of Key Input Interrupt. Table 11.7 lists the Pin Configuration of Key Input Interrupt.

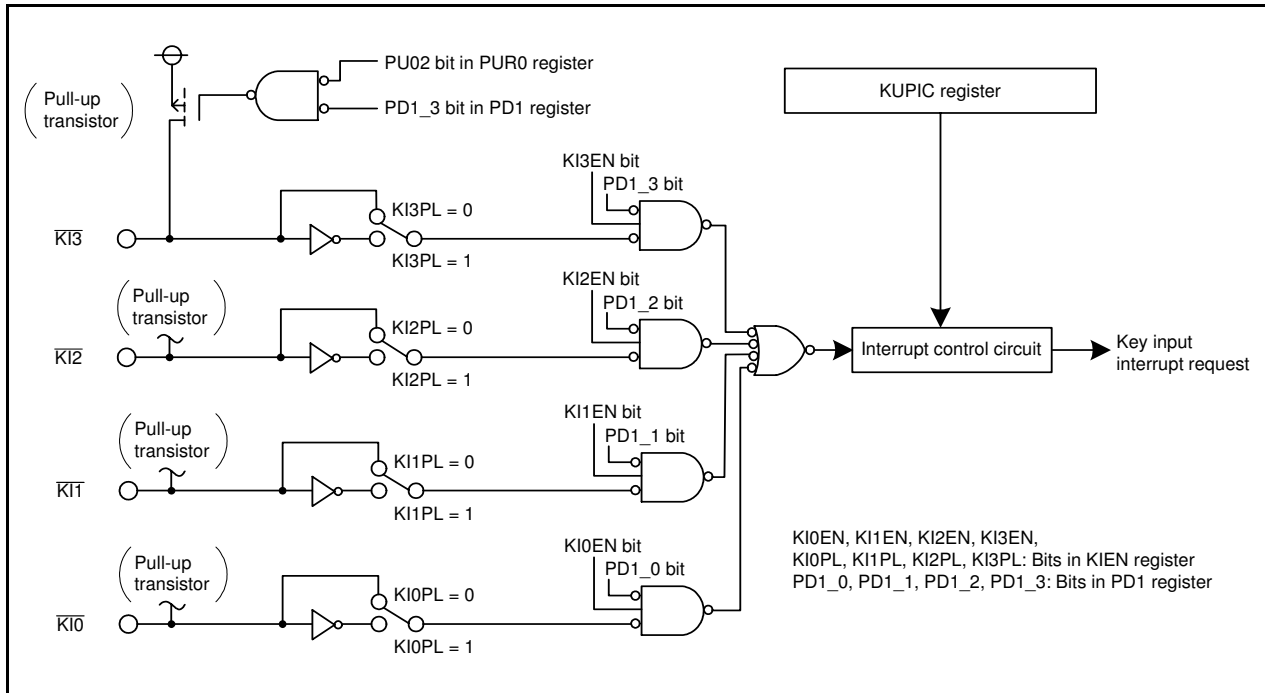


Figure 11.11 Block Diagram of Key Input Interrupt

Table 11.7 Pin Configuration of Key Input Interrupt

| Pin Name         | I/O   | Function                         |
|------------------|-------|----------------------------------|
| $\overline{K10}$ | Input | $\overline{K10}$ interrupt input |
| $\overline{K11}$ | Input | $\overline{K11}$ interrupt input |
| $\overline{K12}$ | Input | $\overline{K12}$ interrupt input |
| $\overline{K13}$ | Input | $\overline{K13}$ interrupt input |

### 11.5.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

|             |       |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit         | b7    | b6    | b5    | b4    | b3    | b2    | b1    | b0    |
| Symbol      | KI3PL | KI3EN | KI2PL | KI2EN | KI1PL | KI1EN | KI0PL | KI0EN |
| After Reset | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

| Bit | Symbol | Bit Name                      | Function                          | R/W |
|-----|--------|-------------------------------|-----------------------------------|-----|
| b0  | KI0EN  | KI0 input enable bit          | 0: Disabled<br>1: Enabled         | R/W |
| b1  | KI0PL  | KI0 input polarity select bit | 0: Falling edge<br>1: Rising edge | R/W |
| b2  | KI1EN  | KI1 input enable bit          | 0: Disabled<br>1: Enabled         | R/W |
| b3  | KI1PL  | KI1 input polarity select bit | 0: Falling edge<br>1: Rising edge | R/W |
| b4  | KI2EN  | KI2 input enable bit          | 0: Disabled<br>1: Enabled         | R/W |
| b5  | KI2PL  | KI2 input polarity select bit | 0: Falling edge<br>1: Rising edge | R/W |
| b6  | KI3EN  | KI3 input enable bit          | 0: Disabled<br>1: Enabled         | R/W |
| b7  | KI3PL  | KI3 input polarity select bit | 0: Falling edge<br>1: Rising edge | R/W |

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

## 11.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi register (i = 0 or 1). Bits AIER0 and AIER1 in the AIER register can be used to select enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (Refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.8 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged and Table 11.9 lists the Correspondence Between Address Match Interrupt Sources and Associated Registers.

**Table 11.8 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged**

| Address Indicated by RMADi Register (i = 0 or 1)   | PC Value Saved <sup>(1)</sup>           |
|--|---|
| <ul style="list-style-type: none"> <li>• Instruction with 2-byte operation code <sup>(2)</sup></li> <li>• Instruction with 1-byte operation code <sup>(2)</sup></li> </ul> ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest<br>OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest<br>STNZ #IMM8,dest STZX #IMM81,#IMM82,dest<br>CMP.B:S #IMM8,dest PUSHM src POPM dest<br>JMPS #IMM8 JSRS #IMM8<br>MOV.B:S #IMM,dest (however, dest = A0 or A1) | Address indicated by RMADi register + 2 |
| Instructions other than above  | Address indicated by RMADi register + 1 |

Notes:

1. Refer to the **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual (REJ09B0001)**.

**Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

**Table 11.9 Correspondence Between Address Match Interrupt Sources and Associated Registers**

| Address Match Interrupt Source | Address Match Interrupt Enable Bit | Address Match Interrupt Register |
|--------------------------------|------------------------------------|----------------------------------|
| Address match interrupt 0      | AIER0                              | RMAD0                            |
| Address match interrupt 1      | AIER1                              | RMAD1                            |

### 11.6.1 Address Match Interrupt Enable Register (AIER)

Address 01C3h (AIER)

|             |    |    |    |    |    |    |       |       |               |
|-------------|----|----|----|----|----|----|-------|-------|---------------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1    | b0    |               |
| Symbol      | —  | —  | —  | —  | —  | —  | AIER1 | AIER0 | AIER register |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0     |               |

| Bit | Symbol | Bit Name  | Function                  | R/W |
|-----|--------|---|---------------------------|-----|
| b0  | AIER0  | Address match interrupt 0 enable bit                                      | 0: Disabled<br>1: Enabled | R/W |
| b1  | AIER1  | Address match interrupt 1 enable bit                                      | 0: Disabled<br>1: Enabled | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                           | —   |
| b3  | —      |   |                           |     |
| b4  | —      |   |                           |     |
| b5  | —      |   |                           |     |
| b6  | —      |   |                           |     |
| b7  | —      |   |                           |     |

### 11.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

|             |     |     |     |     |     |     |    |    |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | —  |
| After Reset | X   | X   | X   | X   | X   | X   | X  | X  |

|             |     |     |     |     |     |     |     |     |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit         | b23 | b22 | b21 | b20 | b19 | b18 | b17 | b16 |
| Symbol      | —   | —   | —   | —   | —   | —   | —   | —   |
| After Reset | 0   | 0   | 0   | 0   | X   | X   | X   | X   |

| Bit       | Symbol | Function  | Setting Range    | R/W |
|-----------|--------|---|------------------|-----|
| b19 to b0 | —      | Address setting register for address match interrupt                      | 00000h to FFFFFh | R/W |
| b20       | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                  | —   |
| b21       | —      |   |                  |     |
| b22       | —      |   |                  |     |
| b23       | —      |   |                  |     |

## 11.7 Timer RC Interrupt and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RC interrupt and flash memory interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 11.10 lists the Registers Associated with Timer RC Interrupt and Flash Memory Interrupt.

**Table 11.10 Registers Associated with Timer RC Interrupt and Flash Memory Interrupt**

| Peripheral Function Name | Status Register of Interrupt Request Source | Enable Register of Interrupt Request Source | Interrupt Control Register |
|--------------------------|---|---|----------------------------|
| Timer RC                 | TRCSR                                       | TRCIER                                      | TRCIC                      |
| Flash memory             | RDYSTI                                      | RDYSTIE                                     | FMRDYIC                    |
|                          | BSYAEI                                      | BSYAEIE                                     |                            |
|                          |   | CMDERIE                                     |                            |



As with other maskable interrupts, the timer RC interrupt and flash memory interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).  
That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.  
Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.  
The IR bit is also not automatically set to 0 when the interrupt is acknowledged.  
Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**18. Timer RC** and **24. Flash Memory**) for the status register and enable register.

For the interrupt control register, refer to **11.3 Interrupt Control**.

## 11.8 Notes on Interrupts

### 11.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

### 11.8.2 SP Setting

Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

### 11.8.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins  $\overline{\text{INT0}}$ ,  $\overline{\text{INT1}}$ ,  $\overline{\text{INT3}}$  and pins  $\overline{\text{KI0}}$  to  $\overline{\text{KI3}}$ , regardless of the CPU clock.

For details, refer to **Table 26.18** (VCC = 5V), **Table 26.24** (VCC = 3V), **Table 26.30** (VCC = 2.2V) **External Interrupt INT<sub>i</sub> (i = 0, 1, 3) Input, Key Input Interrupt KI<sub>i</sub> (i = 0 to 3)**.

### 11.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources. Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts. Figure 11.12 shows a Procedure Example for Changing Interrupt Sources.

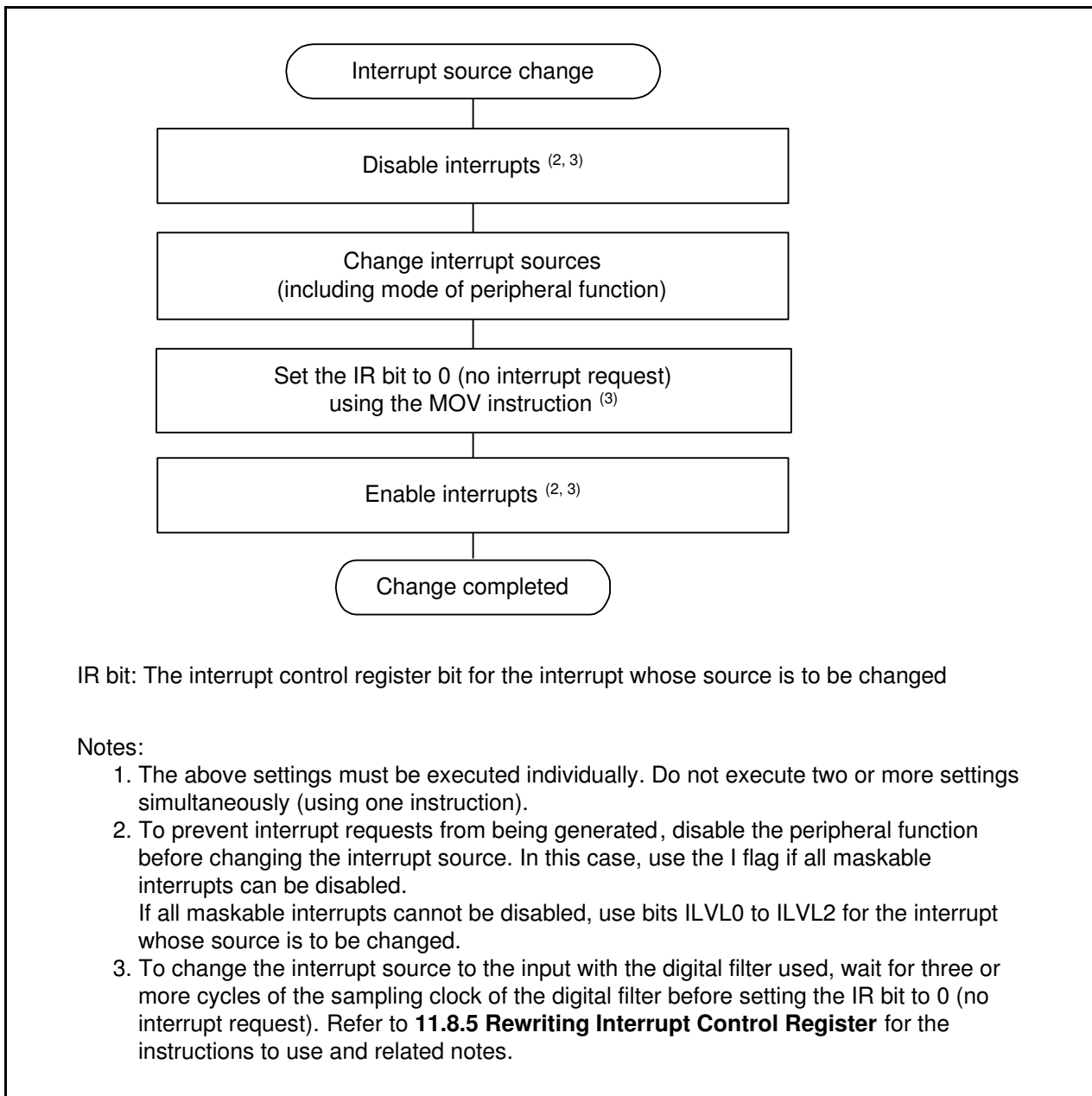


Figure 11.12 Procedure Example for Changing Interrupt Sources

### 11.8.5 Rewriting Interrupt Control Register

- (a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.
- (b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.

#### Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

#### Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

- (c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

#### Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  NOP                    ;
  NOP                    ;
  FSET   I           ; Enable interrupts
```

#### Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  MOV.W  MEM,R0      ; Dummy read
  FSET   I           ; Enable interrupts
```

#### Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC  FLG
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  POPC   FLG        ; Enable interrupts
```

## 12. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

### 12.1 Overview

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEb, 0FFEf, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 12.1 shows the ID Code Areas.

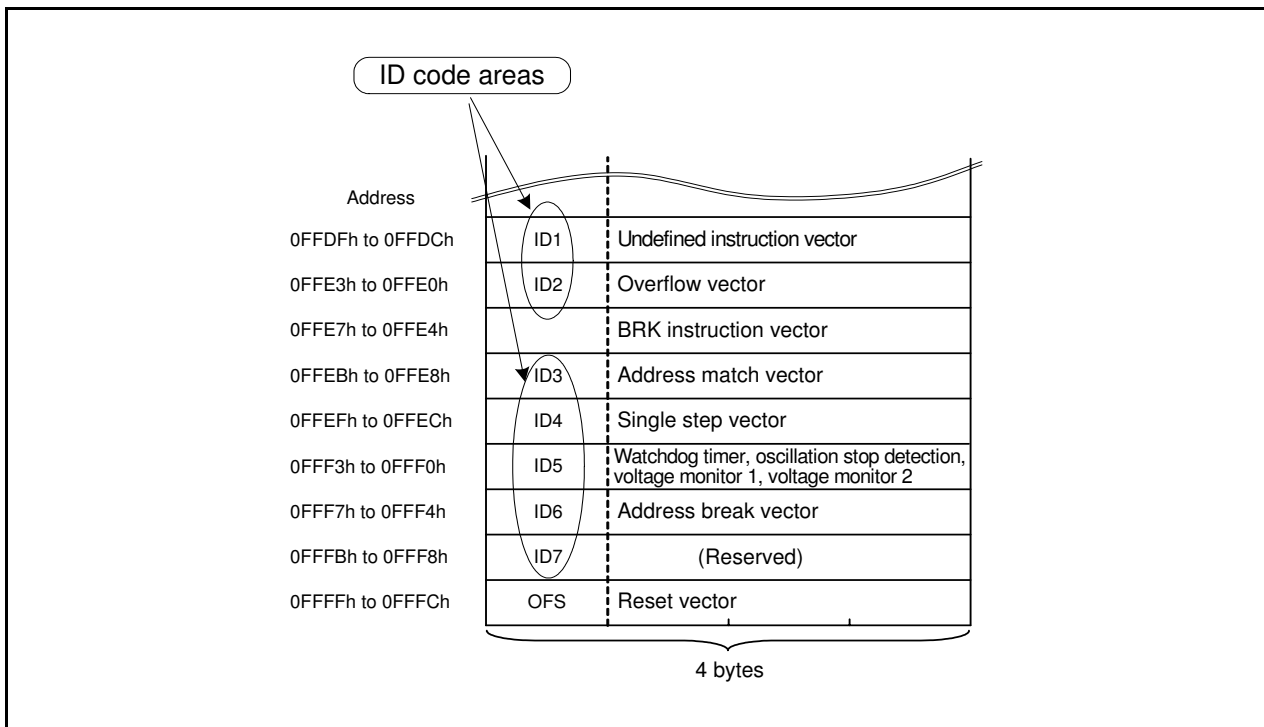


Figure 12.1 ID Code Areas

## 12.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.

If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes "ALeRASE" is the reserved word used for the forced erase function. The character sequence of the ASCII codes "Protect" is the reserved word used for the standard serial I/O mode disabled function. Table 12.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

**Table 12.1 ID Code Reserved Word**

| ID Code Storage Address |     | ID Code Reserved Word (ASCII) <sup>(1)</sup> |                      |
|-------------------------|-----|--|----------------------|
|                         |     | ALeRASE                                      | Protect              |
| 0FFDFh                  | ID1 | 41h (upper-case "A")                         | 50h (upper-case "P") |
| 0FFE3h                  | ID2 | 4Ch (upper-case "L")                         | 72h (lower-case "r") |
| 0FFEbH                  | ID3 | 65h (lower-case "e")                         | 6Fh (lower-case "o") |
| 0FFEFh                  | ID4 | 52h (upper-case "R")                         | 74h (lower-case "t") |
| 0FFF3h                  | ID5 | 41h (upper-case "A")                         | 65h (lower-case "e") |
| 0FFF7h                  | ID6 | 53h (upper-case "S")                         | 63h (lower-case "c") |
| 0FFFBh                  | ID7 | 45h (upper-case "E")                         | 74h (lower-case "t") |

Note:

1. Reserve word: A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1.

### 12.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 12.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 12.2 lists the Conditions and Operations of Forced Erase Function.

Also, when the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

**Table 12.2 Conditions and Operations of Forced Erase Function**

| Condition  |                                    |  | Operation   |
|--|------------------------------------|--|---|
| ID code from serial programmer or the on-chip debugging emulator | ID code in ID code storage address | Bits ROMCP1 and ROMCR in OFS register      |   |
| ALeRASE  | ALeRASE                            | –  | All erasure of user ROM area (forced erase function)      |
|  | Other than ALeRASE (1)             | Other than 01b (ROM code protect disabled) |   |
|  |                                    | 01b (ROM code protect enabled)             | ID code check (ID code check function)                    |
| Other than ALeRASE   | ALeRASE                            | –  | ID code check (ID code check function. No ID code match.) |
|  | Other than ALeRASE (1)             | –  | ID code check (ID code check function)                    |

Note:

1. For “Protect”, refer to **12.4 Standard Serial I/O Mode Disabled Function**.

### 12.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 12.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.

Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or parallel programmer.

## 12.5 Notes on ID Code Areas

### 12.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH  
.lword dummy l (55000000h) ; UND  
.lword dummy l (55000000h) ; INTO  
.lword dummy ; BREAK  
.lword dummy l (55000000h) ; ADDRESS MATCH  
.lword dummy l (55000000h) ; SET SINGLE STEP  
.lword dummy l (55000000h) ; WDT  
.lword dummy l (55000000h) ; ADDRESS BREAK  
.lword dummy l (55000000h) ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)



## 13. Option Function Select Area

### 13.1 Overview

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-address, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 13.1 shows the Option Function Select Area.

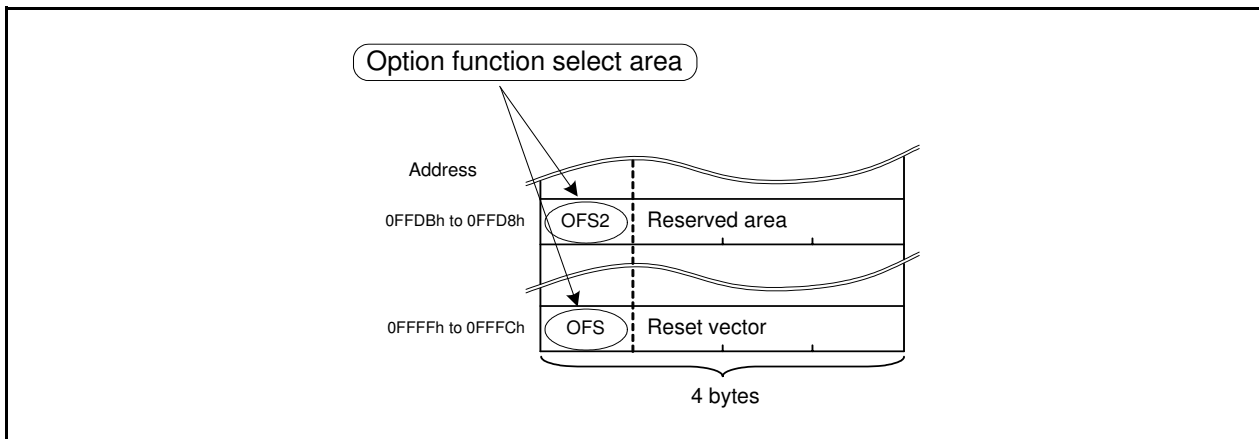


Figure 13.1 Option Function Select Area

## 13.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

### 13.2.1 Option Function Select Register (OFS)

|                |                                   |       |        |        |        |       |    |       |
|----------------|-----------------------------------|-------|--------|--------|--------|-------|----|-------|
| Address 0FFFFh |                                   |       |        |        |        |       |    |       |
| Bit            | b7                                | b6    | b5     | b4     | b3     | b2    | b1 | b0    |
| Symbol         | CSPROINI                          | LVDAS | VDSEL1 | VDSEL0 | ROMCP1 | ROMCR | —  | WDTON |
| After Reset    | User Setting Value <sup>(1)</sup> |       |        |        |        |       |    |       |

| Bit | Symbol   | Bit Name   | Function  | R/W |
|-----|----------|--|---|-----|
| b0  | WDTON    | Watchdog timer start select bit                      | 0: Watchdog timer automatically starts after reset.<br>1: Watchdog timer is stopped after reset.  | R/W |
| b1  | —        | Reserved bit   | Set to 1.   | R/W |
| b2  | ROMCR    | ROM code protect disable bit                         | 0: ROM code protect disabled<br>1: ROMCP1 bit enabled   | R/W |
| b3  | ROMCP1   | ROM code protect bit                                 | 0: ROM code protect enabled<br>1: ROM code protect disabled   | R/W |
| b4  | VDSEL0   | Voltage detection 0 level select bit <sup>(2)</sup>  | b5 b4<br>0 0: 3.80 V selected (Vdet0_3)<br>0 1: 2.85 V selected (Vdet0_2)<br>1 0: 2.35 V selected (Vdet0_1)<br>1 1: 1.90 V selected (Vdet0_0) | R/W |
| b5  | VDSEL1   |  |   | R/W |
| b6  | LVDAS    | Voltage detection 0 circuit start bit <sup>(3)</sup> | 0: Voltage monitor 0 reset enabled after reset<br>1: Voltage monitor 0 reset disabled after reset   | R/W |
| b7  | CSPROINI | Count source protection mode after reset select bit  | 0: Count source protect mode enabled after reset<br>1: Count source protect mode disabled after reset   | R/W |

#### Notes:

- The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.  
When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
- The same level of the voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both functions of voltage monitor 0 reset and power-on reset.
- To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

### LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

### 13.2.2 Option Function Select Register 2 (OFS2)

|                |                                   |    |    |    |         |         |         |         |
|----------------|-----------------------------------|----|----|----|---------|---------|---------|---------|
| Address 0FFDBh |                                   |    |    |    |         |         |         |         |
| Bit            | b7                                | b6 | b5 | b4 | b3      | b2      | b1      | b0      |
| Symbol         | —                                 | —  | —  | —  | WDTRCS1 | WDTRCS0 | WDTUFS1 | WDTUFS0 |
| After Reset    | User Setting Value <sup>(1)</sup> |    |    |    |         |         |         |         |

| Bit | Symbol  | Bit Name  | Function   | R/W |
|-----|---------|---|--|-----|
| b0  | WDTUFS0 | Watchdog timer underflow period set bit               | <sup>b1 b0</sup><br>0 0: 03FFh<br>0 1: 0FFFh<br>1 0: 1FFFh<br>1 1: 3FFFh | R/W |
| b1  | WDTUFS1 |   |  | R/W |
| b2  | WDTRCS0 | Watchdog timer refresh acknowledgement period set bit | <sup>b3 b2</sup><br>0 0: 25%<br>0 1: 50%<br>1 0: 75%<br>1 1: 100%        | R/W |
| b3  | WDTRCS1 |   |  | R/W |
| b4  | —       | Reserved bits   | Set to 1.  | R/W |
| b5  | —       |   |  |     |
| b6  | —       |   |  |     |
| b7  | —       |   |  |     |

Note:

- The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.  
When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.  
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

### 13.3 Notes on Option Function Select Area

#### 13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
```

```
.lword reset | (0FF00000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
```

```
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

## 14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

### 14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.

Table 14.1 lists the Watchdog Timer Specifications.

Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.

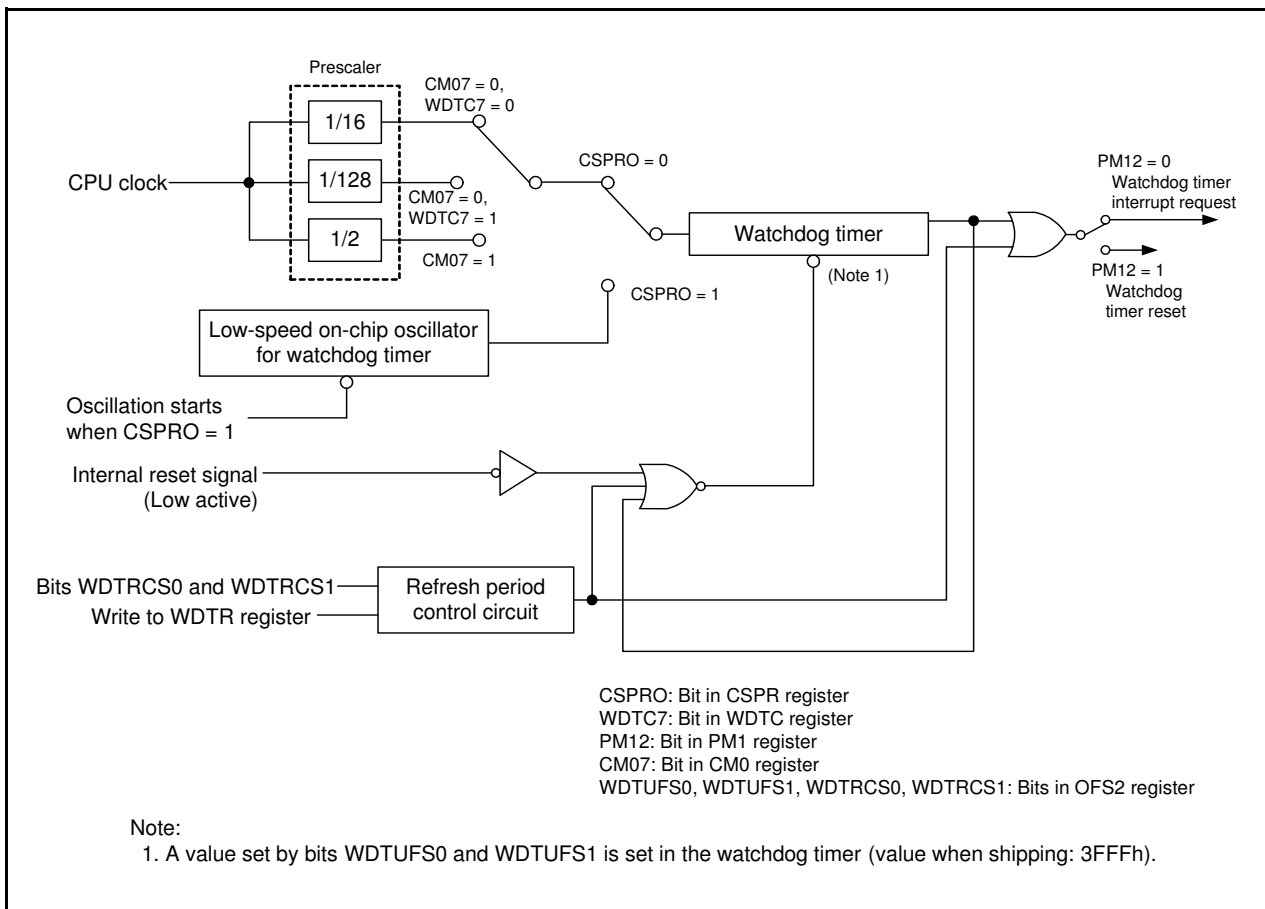
Figure 14.1 shows a Watchdog Timer Block Diagram.

**Table 14.1 Watchdog Timer Specifications**

| Item                                     | Count Source Protection Mode Disabled  | Count Source Protection Mode Enabled                      |
|--|--|---|
| Count source                             | CPU clock  | Low-speed on-chip oscillator clock for the watchdog timer |
| Count operation                          | Decrement  |   |
| Count start condition                    | Either of the following can be selected: <ul style="list-style-type: none"> <li>• After a reset, count starts automatically.</li> <li>• Count starts by writing to the WDTS register.</li> </ul>   |   |
| Count stop condition                     | Stop mode, wait mode   | None  |
| Watchdog timer initialization conditions | <ul style="list-style-type: none"> <li>• Reset</li> <li>• Write 00h and then FFh to the WDTR register (with acknowledgement period setting). <sup>(1)</sup></li> <li>• Underflow</li> </ul>  |   |
| Operations at underflow                  | Watchdog timer interrupt or watchdog timer reset   | Watchdog timer reset                                      |
| Selectable functions                     | <ul style="list-style-type: none"> <li>• Division ratio of the prescaler<br/>Selected by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register.</li> <li>• Count source protection mode<br/>Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program).</li> <li>• Start or stop of the watchdog timer after a reset<br/>Selected by the WDTON bit in the OFS register (flash memory).</li> <li>• Initial value of the watchdog timer<br/>Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register.</li> <li>• Refresh acknowledgement period for the watchdog timer<br/>Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.</li> </ul> |   |

Note:

1. Write the WDTR register during the count operation of the watchdog timer.



**Figure 14.1 Watchdog Timer Block Diagram**

## 14.2 Registers

### 14.2.1 Processor Mode Register 1 (PM1)

Address 0005h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2   | b1 | b0 |
|-------------|----|----|----|----|----|------|----|----|
| Symbol      | —  | —  | —  | —  | —  | PM12 | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0    | 0  | 0  |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | —      | Reserved bits   | Set to 0.   | R/W |
| b1  | —      |   |   |     |
| b2  | PM12   | WDT interrupt/reset switch bit  | 0: Watchdog timer interrupt<br>1: Watchdog timer reset <sup>(1)</sup> | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | —      |   |   |     |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      | Reserved bit  | Set to 0.   | R/W |

Note:

- The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

### 14.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit      | Function  | R/W |
|----------|---|-----|
| b7 to b0 | Writing 00h and then FFh to this register initializes the watchdog timer.<br>The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. <sup>(1)</sup> | W   |

Note:

- Write the WDTR register during the count operation of the watchdog timer.

### 14.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit      | Function  | R/W |
|----------|---|-----|
| b7 to b0 | A write instruction to this register starts the watchdog timer. | W   |

### 14.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

| Bit         | b7    | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|-------|----|----|----|----|----|----|----|
| Symbol      | WDTC7 | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 0     | 0  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit | Symbol | Bit Name  | Function                              | R/W |
|-----|--------|---|---------------------------------------|-----|
| b0  | —      | The following bits of the watchdog timer can be read. |                                       | R   |
| b1  | —      | When bits WDTUFS1 to WDTUFS0 in the OFS2 register are |                                       | R   |
| b2  | —      | 00b (03FFh): b5 to b0                                 |                                       | R   |
| b3  | —      | 01b (0FFFh): b7 to b2                                 |                                       | R   |
| b4  | —      | 10b (1FFFh): b8 to b3                                 |                                       | R   |
| b5  | —      | 11b (3FFFh): b9 to b4                                 |                                       | R   |
| b6  | —      | Reserved bit  | When read, the content is 0.          | R   |
| b7  | WDTC7  | Prescaler select bit                                  | 0: Divided-by-16<br>1: Divided-by-128 | R/W |

### 14.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

| Bit         | b7    | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|-------|----|----|----|----|----|----|----|
| Symbol      | CSPRO | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

The above applies when the CSPROINI bit in the OFS register is set to 1.

|             |   |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|---|
| After Reset | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|-------------|---|---|---|---|---|---|---|---|

The above applies when the CSPROINI bit in the OFS register is set to 0.

| Bit | Symbol | Bit Name   | Function  | R/W       |
|-----|--------|--|---|-----------|
| b0  | —      | Reserved bits  |   | Set to 0. |
| b1  | —      |  |   |           |
| b2  | —      |  |   |           |
| b3  | —      |  |   |           |
| b4  | —      |  |   |           |
| b5  | —      |  |   |           |
| b6  | —      |  |   |           |
| b7  | CSPRO  | Count source protection mode select bit <sup>(1)</sup> | 0: Count source protection mode disabled<br>1: Count source protection mode enabled | R/W       |

Note:

- To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts between writing 0 and writing 1.



### 14.2.6 Option Function Select Register (OFS)

|                |                                   |       |        |        |        |       |    |       |
|----------------|-----------------------------------|-------|--------|--------|--------|-------|----|-------|
| Address 0FFFFh |                                   |       |        |        |        |       |    |       |
| Bit            | b7                                | b6    | b5     | b4     | b3     | b2    | b1 | b0    |
| Symbol         | CSPROINI                          | LVDAS | VDSEL1 | VDSEL0 | ROMCP1 | ROMCR | —  | WDTON |
| After Reset    | User Setting Value <sup>(1)</sup> |       |        |        |        |       |    |       |

| Bit | Symbol   | Bit Name   | Function   | R/W |
|-----|----------|--|--|-----|
| b0  | WDTON    | Watchdog timer start select bit                      | 0: Watchdog timer automatically starts after reset.<br>1: Watchdog timer is stopped after reset.   | R/W |
| b1  | —        | Reserved bit   | Set to 1.  | R/W |
| b2  | ROMCR    | ROM code protect disable bit                         | 0: ROM code protect disabled<br>1: ROMCP1 bit enabled  | R/W |
| b3  | ROMCP1   | ROM code protect bit                                 | 0: ROM code protect enabled<br>1: ROM code protect disabled  | R/W |
| b4  | VDSEL0   | Voltage detection 0 level select bit <sup>(2)</sup>  | <sup>b5 b4</sup><br>0 0: 3.80 V selected (Vdet0_3)<br>0 1: 2.85 V selected (Vdet0_2)<br>1 0: 2.35 V selected (Vdet0_1)<br>1 1: 1.90 V selected (Vdet0_0) | R/W |
| b5  | VDSEL1   |  |  | R/W |
| b6  | LVDAS    | Voltage detection 0 circuit start bit <sup>(3)</sup> | 0: Voltage monitor 0 reset enabled after reset<br>1: Voltage monitor 0 reset disabled after reset  | R/W |
| b7  | CSPROINI | Count source protection mode after reset select bit  | 0: Count source protect mode enabled after reset<br>1: Count source protect mode disabled after reset  | R/W |

#### Notes:

- The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.  
When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
- The same level of the voltage detection 0 level selected by bits VDSEL0 and VDES L1 is set in both functions of voltage monitor 0 reset and power-on reset.
- To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

### LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

### 14.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

|             |                                   |    |    |    |         |         |         |         |
|-------------|-----------------------------------|----|----|----|---------|---------|---------|---------|
| Bit         | b7                                | b6 | b5 | b4 | b3      | b2      | b1      | b0      |
| Symbol      | —                                 | —  | —  | —  | WDTRCS1 | WDTRCS0 | WDTUFS1 | WDTUFS0 |
| After Reset | User Setting Value <sup>(1)</sup> |    |    |    |         |         |         |         |

| Bit | Symbol  | Bit Name  | Function   | R/W |
|-----|---------|---|--|-----|
| b0  | WDTUFS0 | Watchdog timer underflow period set bit               | <sup>b1 b0</sup><br>0 0: 03FFh<br>0 1: 0FFFh<br>1 0: 1FFFh<br>1 1: 3FFFh | R/W |
| b1  | WDTUFS1 |   |  | R/W |
| b2  | WDTRCS0 | Watchdog timer refresh acknowledgement period set bit | <sup>b3 b2</sup><br>0 0: 25%<br>0 1: 50%<br>1 0: 75%<br>1 1: 100%        | R/W |
| b3  | WDTRCS1 |   |  | R/W |
| b4  | —       | Reserved bits   | Set to 1.  | R/W |
| b5  | —       |   |  |     |
| b6  | —       |   |  |     |
| b7  | —       |   |  |     |

Note:

- The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.  
When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.

For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

## 14.3 Functional Description

### 14.3.1 Common Items for Multiple Modes

#### 14.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 14.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

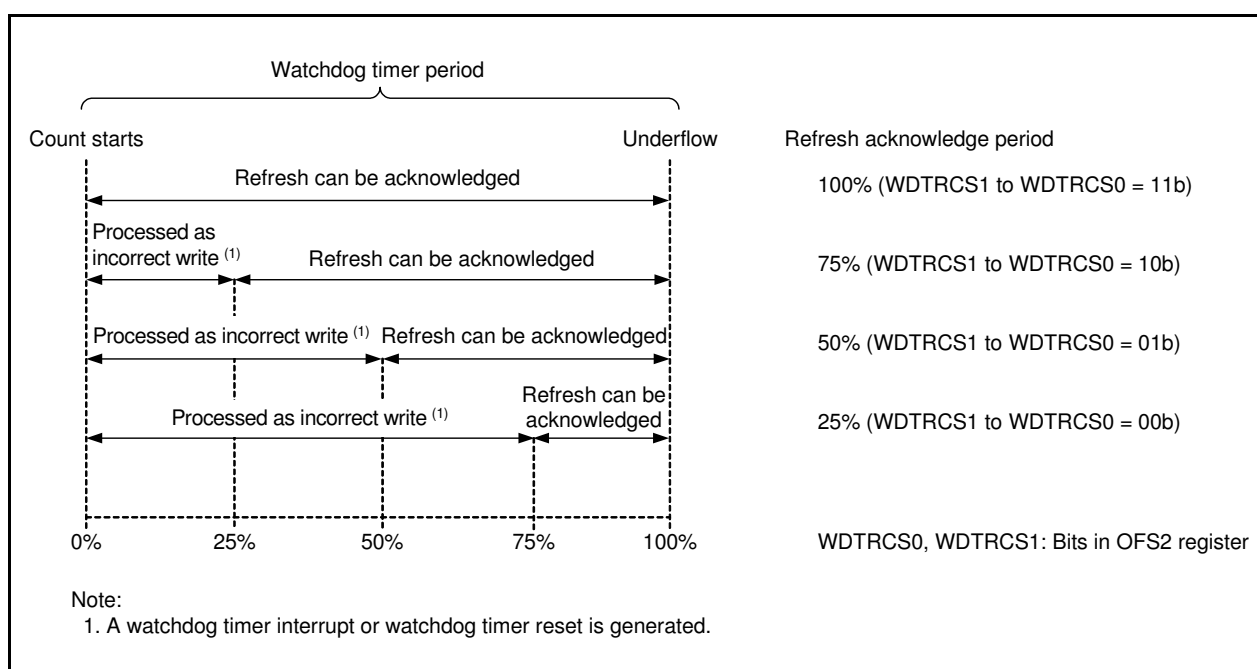


Figure 14.2 Refresh Acknowledgement Period for Watchdog Timer

### 14.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 14.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

**Table 14.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)**

| Item                                     | Specification   |
|--|---|
| Count source                             | CPU clock   |
| Count operation                          | Decrement   |
| Period                                   | $\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}$ <sup>(1)</sup><br>CPU clock<br>n: 16 or 128 (selected by the WDTC7 bit in the WDTC register), or<br>2 when selecting the low-speed clock (CM07 bit in CM0 register = 1)<br>m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register<br>Example:<br>The period is approximately 13.1 ms when:<br>- The CPU clock frequency is set to 20 MHz.<br>- The prescaler is divided by 16.<br>- Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).                           |
| Watchdog timer initialization conditions | <ul style="list-style-type: none"> <li>• Reset</li> <li>• Write 00h and then FFh to the WDTR register. <sup>(3)</sup></li> <li>• Underflow</li> </ul>   |
| Count start conditions                   | The operation of the watchdog timer after a reset is selected by the WDTON bit <sup>(2)</sup> in the OFS register (address 0FFFFh). <ul style="list-style-type: none"> <li>• When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to.</li> <li>• When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.</li> </ul> |
| Count stop condition                     | Stop mode, wait mode (Count resumes from the retained value after exiting.)   |
| Operations at underflow                  | <ul style="list-style-type: none"> <li>• When the PM12 bit in the PM1 register is set to 0.<br/>Watchdog timer interrupt</li> <li>• When the PM12 bit in the PM1 register is set to 1.<br/>Watchdog timer reset (refer to <b>5.5 Watchdog Timer Reset</b>)</li> </ul>   |

Notes:

1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

### 14.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.

Table 14.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

**Table 14.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)**

| Item                                     | Specification  |
|--|--|
| Count source                             | Low-speed on-chip oscillator clock   |
| Count operation                          | Decrement  |
| Period                                   | <p style="text-align: center;">Count value of watchdog timer (m)</p> <p>Low-speed on-chip oscillator clock for the watchdog timer<br/> m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register<br/> Example:<br/> The period is approximately 8.2 ms when:<br/> - The on-chip oscillator clock for the watchdog timer is set to 125 kHz.<br/> - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).</p>  |
| Watchdog timer initialization conditions | <ul style="list-style-type: none"> <li>• Reset</li> <li>• Write 00h and then FFh to the WDTR register. <sup>(3)</sup></li> <li>• Underflow</li> </ul>  |
| Count start conditions                   | <p>The operation of the watchdog timer after a reset is selected by the WDTON bit <sup>(1)</sup> in the OFS register (address 0FFFFh).</p> <ul style="list-style-type: none"> <li>• When the WDTON bit is set to 1 (watchdog timer is stopped after reset).<br/>The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to.</li> <li>• When the WDTON bit is set to 0 (watchdog timer starts automatically after reset).<br/>The watchdog timer and prescaler start counting automatically after a reset.</li> </ul> |
| Count stop condition                     | None (Count does not stop even in wait mode and stop mode once it starts.)   |
| Operation at underflow                   | Watchdog timer reset (Refer to <b>5.5 Watchdog Timer Reset.</b> )  |
| Registers, bits                          | <ul style="list-style-type: none"> <li>• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) <sup>(2)</sup>, the following are set automatically: <ul style="list-style-type: none"> <li>- The low-speed on-chip oscillator for the watchdog timer is on.</li> <li>- The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).</li> </ul> </li> </ul>  |

Notes:

1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

## 15. General Overview of Timers

The MCU has two 8-bit timers with 8-bit prescalers, a 16-bit timer, and a timer with a 4-bit counter and an 8-bit counter. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. The 16-bit timers are timer RC, and have input capture and output compare functions. The 4-bit and 8-bit counters are timer RE, and has an output compare function. All the timers operate independently.

Table 15.1 lists Functional Comparison of Timers.

**Table 15.1 Functional Comparison of Timers**

| Item              |   | Timer RA   | Timer RB   | Timer RC   | Timer RE   |
|-------------------|---|--|--|--|--|
| Configuration     |   | 8-bit timer with 8-bit prescaler (with reload register)  | 8-bit timer with 8-bit prescaler (with reload register)  | 16-bit timer (with input capture and output compare)   | 4-bit counter<br>8-bit counter   |
| Count             |   | Decrement  | Decrement  | Increment  | Increment  |
| Count sources     |   | <ul style="list-style-type: none"> <li>• f1</li> <li>• f2</li> <li>• f8</li> <li>• fOCO</li> <li>• fC32</li> <li>• fC</li> </ul> | <ul style="list-style-type: none"> <li>• f1</li> <li>• f2</li> <li>• f8</li> <li>• Timer RA underflow</li> </ul> | <ul style="list-style-type: none"> <li>• f1</li> <li>• f2</li> <li>• f4</li> <li>• f8</li> <li>• f32</li> <li>• fOCO40M</li> <li>• fOCO-F</li> <li>• TRCCLK</li> </ul> | <ul style="list-style-type: none"> <li>• f4</li> <li>• f8</li> <li>• f32</li> <li>• fC4</li> </ul> |
| Function          | Count of the internal count source      | Timer mode   | Timer mode   | Timer mode (output compare function)   | —  |
|                   | Count of the external count source      | Event counter mode   | —  | Timer mode (output compare function)   | —  |
|                   | External pulse width/period measurement | Pulse width measurement mode, pulse period measurement mode  | —  | Timer mode (input capture function; 4 pins)  | —  |
|                   | PWM output                              | Pulse output mode <sup>(1)</sup> , Event counter mode <sup>(1)</sup>   | Programmable waveform generation mode  | Timer mode (output compare function; 4 pins) <sup>(1)</sup> , PWM mode (3 pins), PWM2 mode (1 pin)   | —  |
|                   | One-shot waveform output                | —  | Programmable one-shot generation mode, Programmable wait one-shot generation mode                                | PWM mode (3 pins)  | —  |
|                   | Three-phase waveforms output            | —  | —  | —  | —  |
|                   | Timer                                   | Timer mode (only fC32 count)   | —  | —  | Real-time clock mode   |
| Input pin         |   | TRAIO  | INT0   | INT0, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD   | —  |
| Output pin        |   | TRA0, TRAIO  | TRBO   | TRCIOA, TRCIOB, TRCIOC, TRCIOD   | —  |
| Related interrupt |   | Timer RA interrupt   | Timer RB interrupt, INT0 interrupt   | Compare match/input capture A to D interrupt, Overflow interrupt, INT0 interrupt   | Timer RE interrupt   |
| Timer stop        |   | Provided   | Provided   | Provided   | Provided   |

Note:

1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

## 16. Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

### 16.1 Overview

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 16.2 to 16.6 the Specification of Each Modes**).

The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.

Figure 16.1 shows a Timer RA Block Diagram. Table 16.1 lists Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

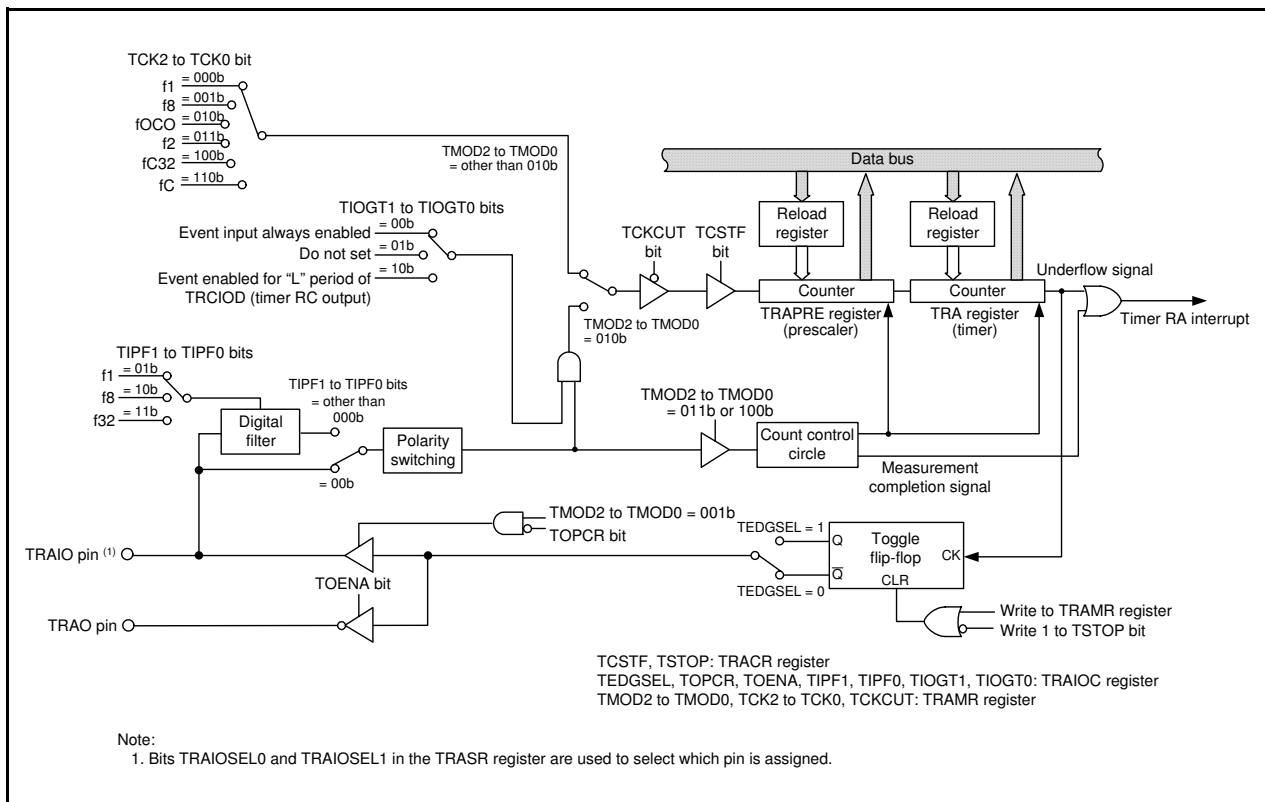


Figure 16.1 Timer RA Block Diagram

Table 16.1 Pin Configuration of Timer RA

| Pin Name | Assigned Pin | I/O    | Function  |
|----------|--------------|--------|---|
| TRAI0    | P1_5 or P1_7 | I/O    | Function differs according to the mode. Refer to descriptions of individual modes for details |
| TRAO     | P3_7         | Output |   |



## 16.2 Registers

### 16.2.1 Timer RA Control Register (TRACR)

Address 0100h

| Bit         | b7 | b6 | b5    | b4    | b3 | b2    | b1    | b0     |
|-------------|----|----|-------|-------|----|-------|-------|--------|
| Symbol      | —  | —  | TUNDF | TEDGF | —  | TSTOP | TCSTF | TSTART |
| After Reset | 0  | 0  | 0     | 0     | 0  | 0     | 0     | 0      |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | TSTART | Timer RA count start bit <sup>(1)</sup>                                   | 0: Count stops<br>1: Count starts   | R/W |
| b1  | TCSTF  | Timer RA count status flag <sup>(1)</sup>                                 | 0: Count stops<br>1: During count   | R   |
| b2  | TSTOP  | Timer RA count forcible stop bit <sup>(2)</sup>                           | When this bit is set to 1, the count is forcibly stopped.<br>When read, its content is 0. | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | TEDGF  | Active edge judgment flag <sup>(3, 4)</sup>                               | 0: Active edge not received<br>1: Active edge received (end of measurement period)        | R/W |
| b5  | TUNDF  | Timer RA underflow flag <sup>(3, 4)</sup>                                 | 0: No underflow<br>1: Underflow   | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b7  | —      |   |   |     |

Notes:

1. Refer to **16.8 Notes on Timer RA** for precautions regarding bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

### 16.2.2 Timer RA I/O Control Register (TRAIOC)

Address 0101h

| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                      | Function   | R/W |
|-----|---------|-------------------------------|--|-----|
| b0  | TEDGSEL | TRAI0 polarity switch bit     | Function varies according to the operating mode. | R/W |
| b1  | TOPCR   | TRAI0 output control bit      |  | R/W |
| b2  | TOENA   | TRAI0 output enable bit       |  | R/W |
| b3  | —       | Reserved bit                  | Set to 0.  | R/W |
| b4  | TIPF0   | TRAI0 input filter select bit | Function varies according to the operating mode. | R/W |
| b5  | TIPF1   |                               |  | R/W |
| b6  | TIOGT0  | TRAI0 event input control bit |  | R/W |
| b7  | TIOGT1  |                               |  | R/W |

### 16.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

|             |        |      |      |      |    |       |       |       |
|-------------|--------|------|------|------|----|-------|-------|-------|
| Bit         | b7     | b6   | b5   | b4   | b3 | b2    | b1    | b0    |
| Symbol      | TCKCUT | TCK2 | TCK1 | TCK0 | —  | TMOD2 | TMOD1 | TMOD0 |
| After Reset | 0      | 0    | 0    | 0    | 0  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name                           | Function  | R/W   |
|-----|--------|------------------------------------|---|---|
| b0  | TMOD0  | Timer RA operating mode select bit | b2 b1 b0<br>0 0 0: Timer mode<br>0 0 1: Pulse output mode<br>0 1 0: Event counter mode<br>0 1 1: Pulse width measurement mode<br>1 0 0: Pulse period measurement mode<br>1 0 1: Do not set.<br>1 1 0: Do not set.<br>1 1 1: Do not set. | R/W   |
| b1  | TMOD1  |                                    |   | R/W   |
| b2  | TMOD2  |                                    |   | R/W   |
| b3  | —      |                                    |   | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |
| b4  | TCK0   | Timer RA count source select bit   | b6 b5 b4<br>0 0 0: f1<br>0 0 1: f8<br>0 1 0: fOCO<br>0 1 1: f2<br>1 0 0: fC32<br>1 0 1: Do not set.<br>1 1 0: fC<br>1 1 1: Do not set.  | R/W   |
| b5  | TCK1   |                                    |   | R/W   |
| b6  | TCK2   |                                    |   | R/W   |
| b7  | TCKCUT | Timer RA count source cutoff bit   | 0: Provides count source<br>1: Cuts off count source  | R/W   |

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

### 16.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

|             |    |    |    |    |    |    |    |            |
|-------------|----|----|----|----|----|----|----|------------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0         |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —          |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 (Note 1) |

| Bit      | Mode                          | Function  | Setting Range | R/W |
|----------|-------------------------------|---|---------------|-----|
| b7 to b0 | Timer mode                    | Counts an internal count source   | 00h to FFh    | R/W |
|          | Pulse output mode             |   | 00h to FFh    | R/W |
|          | Event counter mode            | Counts an external count source   | 00h to FFh    | R/W |
|          | Pulse width measurement mode  | Measure pulse width of input pulses from external (counts internal count source)  | 00h to FFh    | R/W |
|          | Pulse period measurement mode | Measure pulse period of input pulses from external (counts internal count source) | 00h to FFh    | R/W |

Note:

- When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

### 16.2.5 Timer RA Register (TRA)

Address 0104h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0         |
|-------------|----|----|----|----|----|----|----|------------|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —          |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 (Note 1) |

| Bit      | Mode      | Function                               | Setting Range | R/W |
|----------|-----------|--|---------------|-----|
| b7 to b0 | All modes | Counts on underflow of TRAPRE register | 00h to FFh    | R/W |

Note:

- When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

### 16.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1         | b0         |
|-------------|----|----|----|----|----|----|------------|------------|
| Symbol      | —  | —  | —  | —  | —  | —  | TRAIOSSEL1 | TRAIOSSEL0 |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function   | R/W |
|-----|------------|---|--|-----|
| b0  | TRAIOSSEL0 | TRAIO pin select bit  | <sup>b1 b0</sup><br>0 0: TRAIIO pin not used<br>0 1: P1_7 assigned<br>1 0: P1_5 assigned<br>1 1: Do not set. | R/W |
| b1  | TRAIOSSEL1 |   |  | R/W |
| b2  | —          | Reserved bits   | Set to 0.  | R/W |
| b3  | —          |   |  |     |
| b4  | —          |   |  |     |
| b5  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b6  | —          |   |  |     |
| b7  | —          |   |  |     |

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.

Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

### 16.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 16.2 Timer Mode Specifications**).

**Table 16.2 Timer Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Count sources                       | f1, f2, f8, fOCO, fC32, fC  |
| Count operations                    | <ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer underflows, the contents of the reload register are reloaded and the count is continued.</li> </ul>  |
| Divide ratio                        | $1/(n+1)(m+1)$<br>n: Value set in TRAPRE register, m: Value set in TRA register   |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRACR register.  |
| Count stop conditions               | <ul style="list-style-type: none"> <li>0 (count stops) is written to the TSTART bit in the TRACR register.</li> <li>1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>  |
| Interrupt request generation timing | When timer RA underflows [timer RA interrupt].  |
| TRAIO pin function                  | Programmable I/O port   |
| TRAO pin function                   | Programmable I/O port   |
| Read from timer                     | The count value can be read by reading registers TRA and TRAPRE.  |
| Write to timer                      | <ul style="list-style-type: none"> <li>When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to <b>16.3.2 Timer Write Control during Count Operation</b>).</li> </ul> |

#### 16.3.1 Timer RA I/O Control Register (TRAIOC) in Timer Mode

Address 0101h

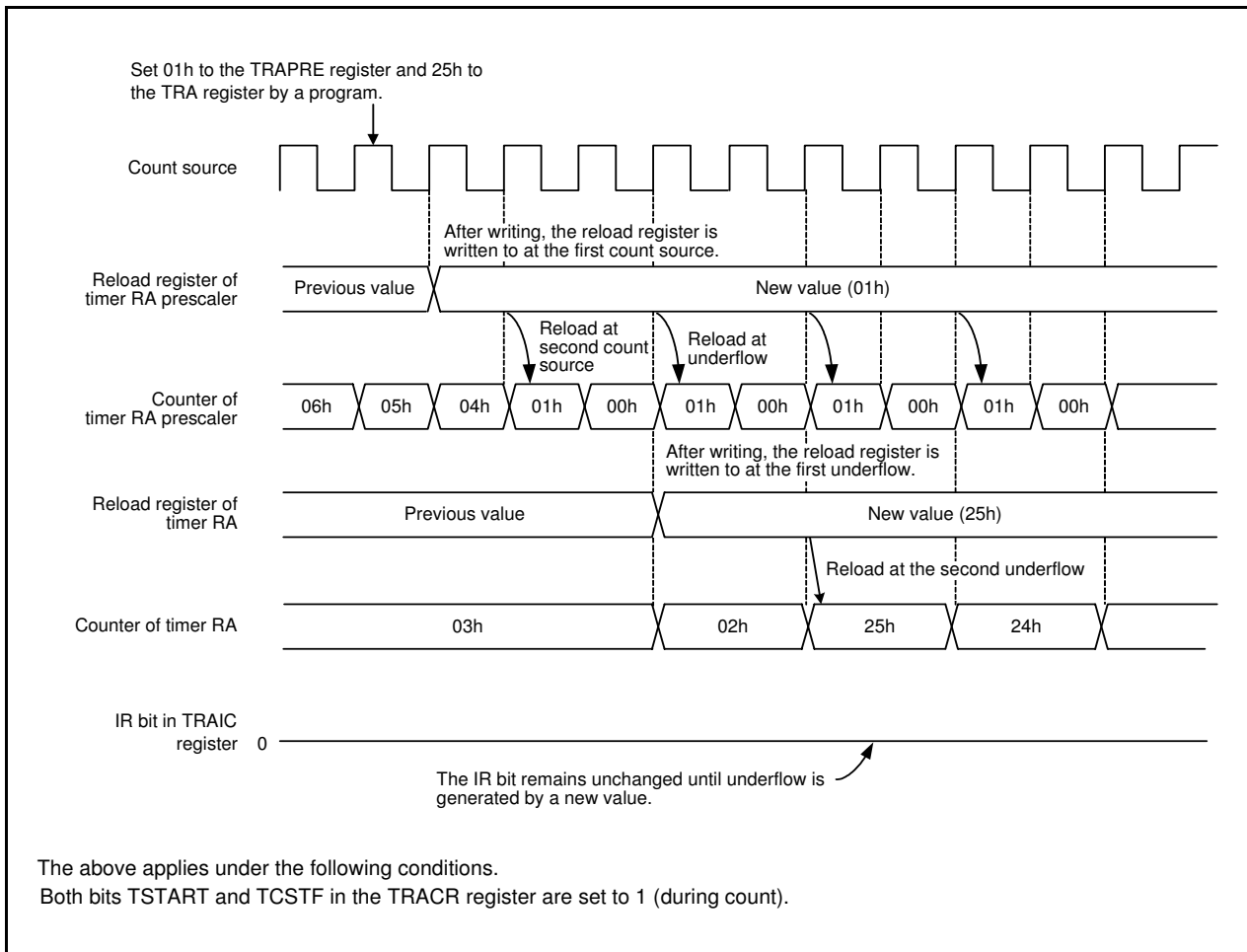
| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                      | Function                | R/W |
|-----|---------|-------------------------------|-------------------------|-----|
| b0  | TEDGSEL | TRAIO polarity switch bit     | Set to 0 in timer mode. | R/W |
| b1  | TOPCR   | TRAIO output control bit      |                         | R/W |
| b2  | TOENA   | TRAO output enable bit        |                         | R/W |
| b3  | —       | Reserved bit                  | Set to 0.               | R/W |
| b4  | TIPF0   | TRAIO input filter select bit | Set to 0 in timer mode. | R/W |
| b5  | TIPF1   |                               |                         | R/W |
| b6  | TIOGT0  | TRAIO event input control bit |                         | R/W |
| b7  | TIOGT1  |                               |                         | R/W |

### 16.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 16.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.



**Figure 16.2** Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

## 16.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAI0 pin each time the timer underflows (refer to **Table 16.3 Pulse Output Mode Specifications**).

**Table 16.3 Pulse Output Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Count sources                       | f1, f2, f8, fOCO, fC32, fC  |
| Count operations                    | <ul style="list-style-type: none"> <li>• Decrement</li> <li>• When the timer underflows, the contents in the reload register is reloaded and the count is continued.</li> </ul>   |
| Divide ratio                        | $1/(n+1)(m+1)$<br>n: Value set in TRAPRE register, m: Value set in TRA register   |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRACR register.  |
| Count stop conditions               | <ul style="list-style-type: none"> <li>• 0 (count stops) is written to the TSTART bit in the TRACR register.</li> <li>• 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>  |
| Interrupt request generation timing | When timer RA underflows [timer RA interrupt].  |
| TRAI0 pin function                  | Pulse output, programmable output port  |
| TRAO pin function                   | Programmable I/O port or inverted output of TRAI0   |
| Read from timer                     | The count value can be read by reading registers TRA and TRAPRE.  |
| Write to timer                      | <ul style="list-style-type: none"> <li>• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>• When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to <b>16.3.2 Timer Write Control during Count Operation</b>).</li> </ul>   |
| Selectable functions                | <ul style="list-style-type: none"> <li>• TRAI0 signal polarity switch function<br/>The level when the pulse output starts is selected by the TEDGSEL bit in the TRAI0C register. <sup>(1)</sup></li> <li>• TRAO output function<br/>Pulses inverted from the TRAI0 output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAI0C register).</li> <li>• Pulse output stop function<br/>Output from the TRAI0 pin is stopped by the TOPCR bit in the TRAI0C register.</li> <li>• TRAI0 pin select function<br/>P1_5 or P1_7 is selected by bits TRAI0SEL0 to TRAI0SEL1 in the TRASR register.</li> </ul> |

Note:

1. The level of the output pulse becomes the level when the pulse output starts when the TRAMP register is written to.

### 16.4.1 Timer RA I/O Control Register (TRAIOC) in Pulse Output Mode

Address 0101h

|             |        |        |       |       |    |       |       |         |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                      | Function  | R/W |
|-----|---------|-------------------------------|---|-----|
| b0  | TEDGSEL | TRAIO polarity switch bit     | 0: TRAI0 output starts at "H"<br>1: TRAI0 output starts at "L"              | R/W |
| b1  | TOPCR   | TRAIO output control bit      | 0: TRAI0 output<br>1: TRAI0 output disabled                                 | R/W |
| b2  | TOENA   | TRAO output enable bit        | 0: TRAO output disabled<br>1: TRAO output (inverted TRAI0 output from Port) | R/W |
| b3  | —       | Reserved bit                  | Set to 0.   | R/W |
| b4  | TIPF0   | TRAIO input filter select bit | Set to 0 in pulse output mode.  | R/W |
| b5  | TIPF1   |                               |   | R/W |
| b6  | TIOGT0  | TRAIO event input control bit |   | R/W |
| b7  | TIOGT1  |                               |   | R/W |

## 16.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAI0 pin are counted (refer to **Table 16.4 Event Counter Mode Specifications**).

**Table 16.4 Event Counter Mode Specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Count source                        | External signal which is input to TRAI0 pin (active edge selectable by a program)  |
| Count operations                    | <ul style="list-style-type: none"> <li>• Decrement</li> <li>• When the timer underflows, the contents of the reload register are reloaded and the count is continued.</li> </ul>   |
| Divide ratio                        | $1/(n+1)(m+1)$<br>n: setting value of TRAPRE register, m: setting value of TRA register  |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRACR register.   |
| Count stop conditions               | <ul style="list-style-type: none"> <li>• 0 (count stops) is written to the TSTART bit in the TRACR register.</li> <li>• 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>   |
| Interrupt request generation timing | When timer RA underflows [timer RA interrupt].   |
| TRAI0 pin function                  | Count source input   |
| TRAO pin function                   | Programmable I/O port or pulse output <sup>(1)</sup>   |
| Read from timer                     | The count value can be read by reading registers TRA and TRAPRE.   |
| Write to timer                      | <ul style="list-style-type: none"> <li>• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>• When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to <b>16.3.2 Timer Write Control during Count Operation</b>).</li> </ul>  |
| Selectable functions                | <ul style="list-style-type: none"> <li>• TRAI0 input polarity switch function<br/>The active edge of the count source is selected by the TEDGSEL bit in the TRAI0C register.</li> <li>• Count source input pin select function<br/>P1_5 or P1_7 is selected by bits TRAI0SEL0 to TRAI0SEL1 in the TRASR register.</li> <li>• Pulse output function<br/>Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAI0C register). <sup>(1)</sup></li> <li>• Digital filter function<br/>Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAI0C register.</li> <li>• Event input control function<br/>The enabled period for the event input to the TRAI0 pin is selected by bits TIOGT0 and TIOGT1 in the TRAI0C register.</li> </ul> |

Note:

1. The level of the output pulse becomes the level when the pulse output starts when the TRAMP register is written to.



### 16.5.1 Timer RA I/O Control Register (TRAIOC) in Event Counter Mode

Address 0101h

|             |        |        |       |       |    |       |       |         |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                          | Function  | R/W |
|-----|---------|-----------------------------------|---|-----|
| b0  | TEDGSEL | TRAIO polarity switch bit         | 0: Starts counting at rising edge of the TRAI0 input and TRAO starts output at "L"<br>1: Starts counting at falling edge of the TRAI0 input and TRAO starts output at "H" | R/W |
| b1  | TOPCR   | TRAIO output control bit          | Set to 0 in event counter mode.   | R/W |
| b2  | TOENA   | TRAO output enable bit            | 0: TRAO output disabled<br>1: TRAO output   | R/W |
| b3  | —       | Reserved bit                      | Set to 0.   | R/W |
| b4  | TIPF0   | TRAIO input filter select bit (1) | <sup>b5 b4</sup><br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling                                       | R/W |
| b5  | TIPF1   |                                   |   | R/W |
| b6  | TIOGT0  | TRAIO event input control bit     | <sup>b7 b6</sup><br>0 0: Event input always enabled<br>0 1: Do not set.<br>1 0: Event input enabled for "L" period of TRCIOD (timer RC output)<br>1 1: Do not set.        | R/W |
| b7  | TIOGT1  |                                   |   | R/W |

Note:

1. When the same value from the TRAI0 pin is sampled three times continuously, the input is determined.

## 16.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAI0 pin is measured (refer to **Table 16.5 Pulse Width Measurement Mode Specifications**).

Figure 16.3 shows an Operating Example of Pulse Width Measurement Mode.

**Table 16.5 Pulse Width Measurement Mode Specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Count sources                       | f1, f2, f8, fOCO, fC32, fC   |
| Count operations                    | <ul style="list-style-type: none"> <li>• Decrement</li> <li>• Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level.</li> <li>• When the timer underflows, the contents of the reload register are reloaded and the count is continued.</li> </ul>  |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRACR register.   |
| Count stop conditions               | <ul style="list-style-type: none"> <li>• 0 (count stops) is written to the TSTART bit in the TRACR register.</li> <li>• 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>   |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• When timer RA underflows [timer RA interrupt].</li> <li>• Rising or falling of the TRAI0 input (end of measurement period) [timer RA interrupt]</li> </ul>  |
| TRAI0 pin function                  | Measured pulse input   |
| TRAO pin function                   | Programmable I/O port  |
| Read from timer                     | The count value can be read by reading registers TRA and TRAPRE.   |
| Write to timer                      | <ul style="list-style-type: none"> <li>• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>• When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to <b>16.3.2 Timer Write Control during Count Operation</b>).</li> </ul>  |
| Selectable functions                | <ul style="list-style-type: none"> <li>• Measurement level setting<br/>The “H” level or “L” level period is selected by the TEDGSEL bit in the TRAI0C register.</li> <li>• Measured pulse input pin select function<br/>P1_5 or P1_7 is selected by bits TRAI0SEL0 to TRAI0SEL1 in the TRASR register.</li> <li>• Digital filter function<br/>Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAI0C register.</li> </ul> |

### 16.6.1 Timer RA I/O Control Register (TRAIOC) in Pulse Width Measurement Mode

Address 0101h

| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                                     | Function   | R/W |
|-----|---------|--|--|-----|
| b0  | TEDGSEL | TRAIO polarity switch bit                    | 0: TRAI0 input starts at "L"<br>1: TRAI0 input starts at "H"   | R/W |
| b1  | TOPCR   | TRAIO output control bit                     | Set to 0 in pulse width measurement mode.  | R/W |
| b2  | TOENA   | TRAIO output enable bit                      |  | R/W |
| b3  | —       | Reserved bit                                 | Set to 0.  | R/W |
| b4  | TIPF0   | TRAIO input filter select bit <sup>(1)</sup> | b5 b4<br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b5  | TIPF1   |  |  | R/W |
| b6  | TIOGT0  | TRAIO event input control bit                | Set to 0 in pulse width measurement mode.  | R/W |
| b7  | TIOGT1  |  |  | R/W |

Note:

1. When the same value from the TRAI0 pin is sampled three times continuously, the input is determined.

### 16.6.2 Operating Example

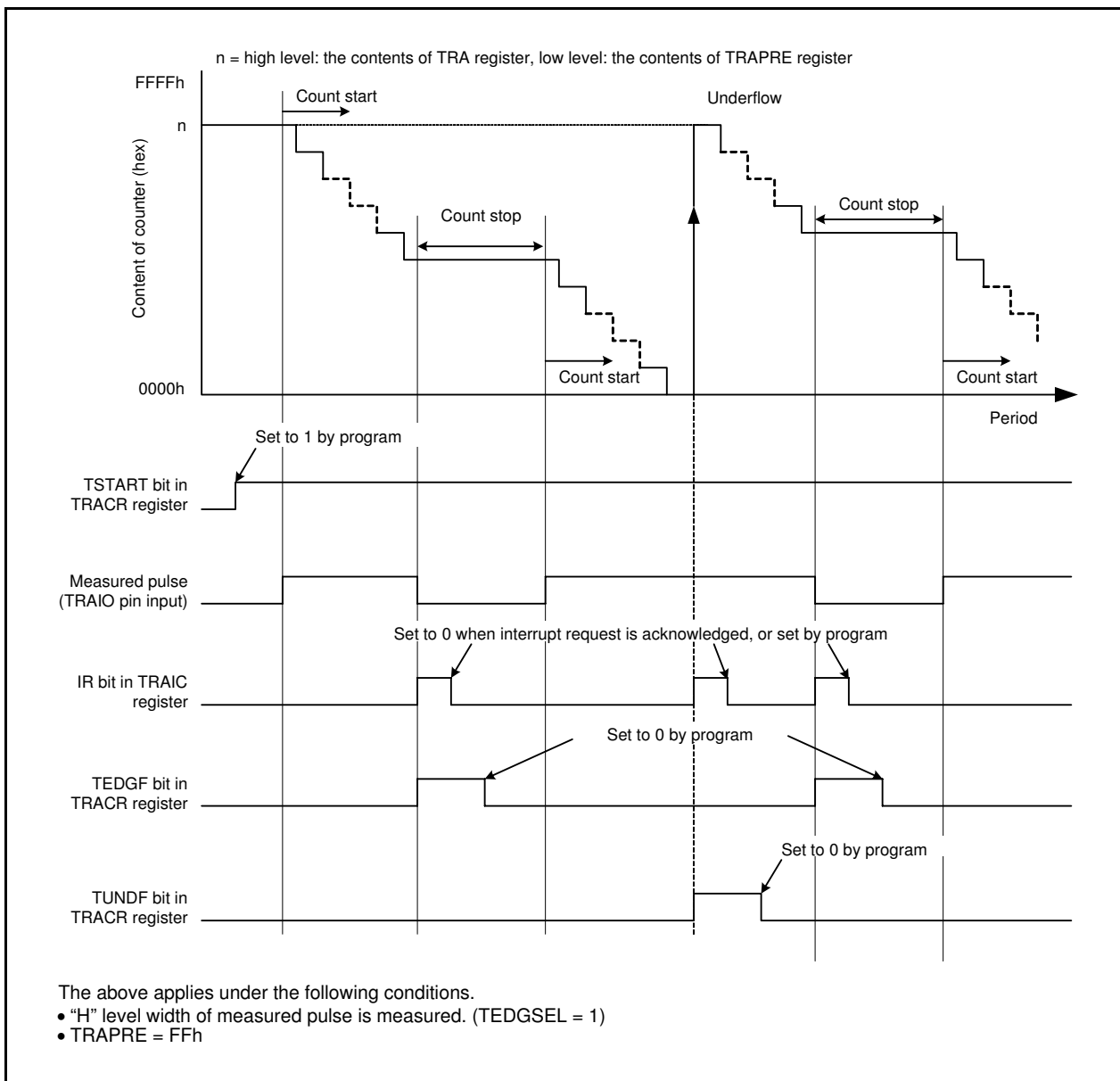


Figure 16.3 Operating Example of Pulse Width Measurement Mode

## 16.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAI0 pin is measured (refer to **Table 16.6 Pulse Period Measurement Mode Specifications**).

Figure 16.4 shows an Operating Example of Pulse Period Measurement Mode.

**Table 16.6 Pulse Period Measurement Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Count sources                       | f1, f2, f8, fOCO, fC32, fC  |
| Count operations                    | <ul style="list-style-type: none"> <li>Decrement</li> <li>After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.</li> </ul>   |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRACR register.  |
| Count stop conditions               | <ul style="list-style-type: none"> <li>0 (count stops) is written to TSTART bit in the TRACR register.</li> <li>1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.</li> </ul>  |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>When timer RA underflows or reloads [timer RA interrupt].</li> <li>Rising or falling of the TRAI0 input (end of measurement period) [timer RA interrupt]</li> </ul>  |
| TRAI0 pin function                  | Measured pulse input (1)  |
| TRAO pin function                   | Programmable I/O port   |
| Read from timer                     | The count value can be read by reading registers TRA and TRAPRE.  |
| Write to timer                      | <ul style="list-style-type: none"> <li>When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to <b>16.3.2 Timer Write Control during Count Operation</b>).</li> </ul>   |
| Selectable functions                | <ul style="list-style-type: none"> <li>Measurement period selection<br/>The measurement period of the input pulse is selected by the TEDGSEL in the TRAI0C register.</li> <li>Measured pulse input pin select function<br/>P1_5 or P1_7 is selected by bits TRAI0SEL0 to TRAI0SEL1 in the TRASR register.</li> <li>Digital filter function<br/>Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAI0C register.</li> </ul> |

Note:

- Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer "H" and "L" width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAI0 pin, the input may be ignored.

### 16.7.1 Timer RA I/O Control Register (TRAIOC) in Pulse Period Measurement Mode

Address 0101h

| Bit         | b7     | b6     | b5    | b4    | b3 | b2    | b1    | b0      |
|-------------|--------|--------|-------|-------|----|-------|-------|---------|
| Symbol      | TIOGT1 | TIOGT0 | TIPF1 | TIPF0 | —  | TOENA | TOPCR | TEDGSEL |
| After Reset | 0      | 0      | 0     | 0     | 0  | 0     | 0     | 0       |

| Bit | Symbol  | Bit Name                                     | Function   | R/W |
|-----|---------|--|--|-----|
| b0  | TEDGSEL | TRAI0 polarity switch bit                    | 0: Measures measurement pulse from one rising edge to next rising edge<br>1: Measures measurement pulse from one falling edge to next falling edge | R/W |
| b1  | TOPCR   | TRAI0 output control bit                     | Set to 0 in pulse period measurement mode.   | R/W |
| b2  | TOENA   | TRAI0 output enable bit                      |  | R/W |
| b3  | —       | Reserved bit                                 | Set to 0.  | R/W |
| b4  | TIPF0   | TRAI0 input filter select bit <sup>(1)</sup> | b5 b4<br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling                           | R/W |
| b5  | TIPF1   |  |  | R/W |
| b6  | TIOGT0  | TRAI0 event input control bit                | Set to 0 in pulse period measurement mode.   | R/W |
| b7  | TIOGT1  |  |  | R/W |

Note:

- When the same value from the TRAI0 pin is sampled three times continuously, the input is determined.

### 16.7.2 Operating Example

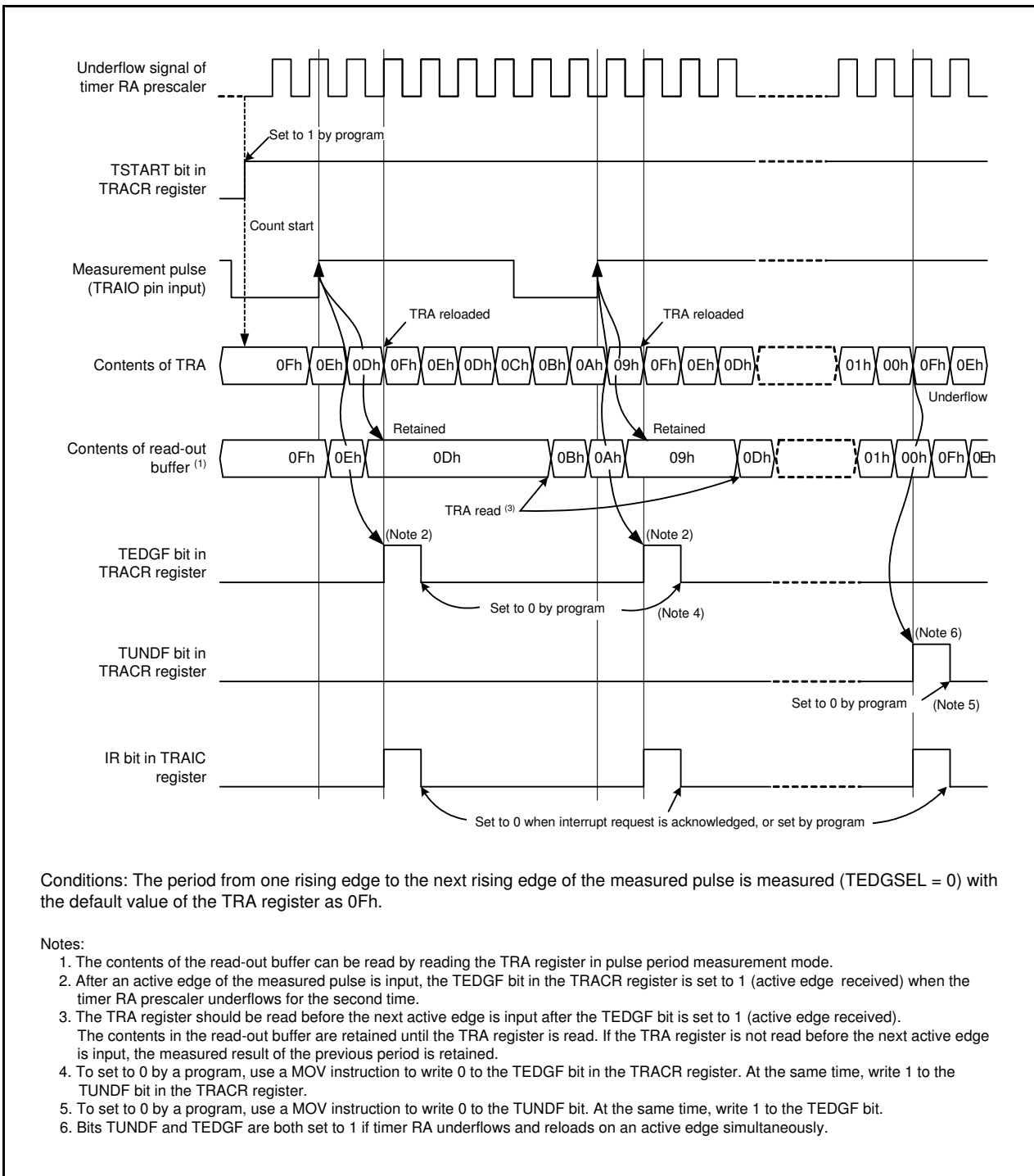


Figure 16.4 Operating Example of Pulse Period Measurement Mode

## 16.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

During this time, do not access registers associated with timer RA <sup>(1)</sup> other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

During this time, do not access registers associated with timer RA <sup>(1)</sup> other than the TCSTF bit.

Note:

1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.



## 17. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

### 17.1 Overview

The prescaler and timer each consist of a reload register and counter (refer to **Tables 17.2 to 17.5 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers. The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.

Figure 17.1 shows a Timer RB Block Diagram. Table 17.1 lists Pin Configuration of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

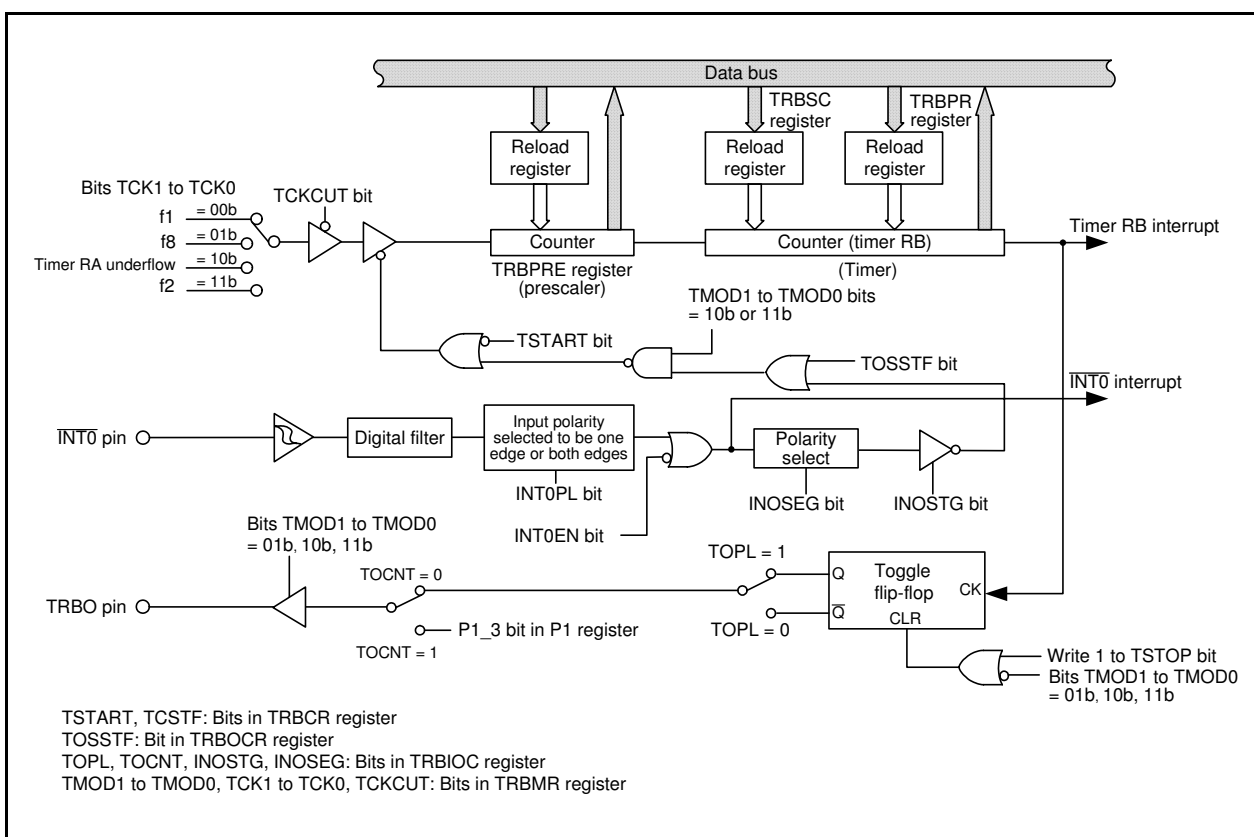


Figure 17.1 Timer RB Block Diagram

Table 17.1 Pin Configuration of Timer RB

| Pin Name | Assigned Pin | I/O    | Function  |
|----------|--------------|--------|---|
| TRBO     | P1_3         | Output | Pulse output (Programmable waveform generation mode, Programmable one-shot generation mode, Programmable wait one-shot generation mode) |

## 17.2 Registers

### 17.2.1 Timer RB Control Register (TRBCR)

Address 0108h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1    | b0     |
|-------------|----|----|----|----|----|-------|-------|--------|
| Symbol      | —  | —  | —  | —  | —  | TSTOP | TCSTF | TSTART |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0     | 0     | 0      |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TSTART | Timer RB count start bit <sup>(1)</sup>                                   | 0: Count stops<br>1: Count starts  | R/W |
| b1  | TCSTF  | Timer RB count status flag <sup>(1)</sup>                                 | 0: Count stops<br>1: During count <sup>(3)</sup>                                       | R   |
| b2  | TSTOP  | Timer RB count forcible stop bit <sup>(1, 2)</sup>                        | When this bit is set to 1, the count is forcibly stopped. When read, the content is 0. | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | —      |   |  |     |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Notes:

1. Refer to **17.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

### 17.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2     | b1    | b0    |
|-------------|----|----|----|----|----|--------|-------|-------|
| Symbol      | —  | —  | —  | —  | —  | TOSSTF | TOSSP | TOSST |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0      | 0     | 0     |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TOSST  | Timer RB one-shot start bit   | When this bit is set to 1, one-shot trigger generated. When read, its content is 0.  | R/W |
| b1  | TOSSP  | Timer RB one-shot stop bit  | When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0. | R/W |
| b2  | TOSSTF | Timer RB one-shot status flag <sup>(1)</sup>                              | 0: One-shot stopped<br>1: One-shot operating (Including wait period)   | R   |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | —      |   |  |     |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Note:

1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

### 17.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

| Bit         | b7 | b6 | b5 | b4 | b3     | b2     | b1    | b0   |
|-------------|----|----|----|----|--------|--------|-------|------|
| Symbol      | —  | —  | —  | —  | INOSEG | INOSTG | TOCNT | TOPL |
| After Reset | 0  | 0  | 0  | 0  | 0      | 0      | 0     | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TOPL   | Timer RB output level select bit  | Function varies according to the operating mode. | R/W |
| b1  | TOCNT  | Timer RB output switch bit  |  | R/W |
| b2  | INOSTG | One-shot trigger control bit  |  | R/W |
| b3  | INOSEG | One-shot trigger polarity select bit                                      |  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

### 17.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

| Bit         | b7     | b6 | b5   | b4   | b3   | b2 | b1    | b0    |
|-------------|--------|----|------|------|------|----|-------|-------|
| Symbol      | TCKCUT | —  | TCK1 | TCK0 | TWRC | —  | TMOD1 | TMOD0 |
| After Reset | 0      | 0  | 0    | 0    | 0    | 0  | 0     | 0     |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TMOD0  | Timer RB operating mode select bit <sup>(1)</sup>                         | <sup>b1 b0</sup><br>0 0: Timer mode<br>0 1: Programmable waveform generation mode<br>1 0: Programmable one-shot generation mode<br>1 1: Programmable wait one-shot generation mode | R/W |
| b1  | TMOD1  |   |  | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b3  | TWRC   | Timer RB write control bit <sup>(2)</sup>                                 | 0: Write to reload register and counter<br>1: Write to reload register only  | R/W |
| b4  | TCK0   | Timer RB count source select bit <sup>(1)</sup>                           | <sup>b5 b4</sup><br>0 0: f1<br>0 1: f8<br>1 0: Timer RA underflow <sup>(3)</sup><br>1 1: f2  | R/W |
| b5  | TCK1   |   |  | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b7  | TCKCUT | Timer RB count source cutoff bit <sup>(1)</sup>                           | 0: Provides count source<br>1: Cuts off count source   | R/W |

Notes:

- Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
- The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

### 17.2.5 Timer RB Prescaler Register (TRBPRES)

Address 010Ch

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit      | Mode                                       | Function   | Setting Range | R/W |
|----------|--|--|---------------|-----|
| b7 to b0 | Timer mode                                 | Counts an internal count source or timer RA underflows | 00h to FFh    | R/W |
|          | Programmable waveform generation mode      |  | 00h to FFh    | R/W |
|          | Programmable one-shot generation mode      |  | 00h to FFh    | R/W |
|          | Programmable wait one-shot generation mode |  | 00h to FFh    | R/W |

When the TSTOP bit in the TRBCR register is set to 1, the TRBPRES register is set to FFh.

### 17.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit      | Mode                                       | Function   | Setting Range | R/W              |
|----------|--|--|---------------|------------------|
| b7 to b0 | Timer mode                                 | Disabled   | 00h to FFh    | —                |
|          | Programmable waveform generation mode      | Counts timer RB prescaler underflows <sup>(1)</sup>              | 00h to FFh    | W <sup>(2)</sup> |
|          | Programmable one-shot generation mode      | Disabled   | 00h to FFh    | —                |
|          | Programmable wait one-shot generation mode | Counts timer RB prescaler underflows (one-shot width is counted) | 00h to FFh    | W <sup>(2)</sup> |

Notes:

1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.

To write to the TRBSC register, perform the following steps.

- (1) Write the value to the TRBSC register.
- (2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

### 17.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit      | Mode                                       | Function  | Setting Range | R/W |
|----------|--|---|---------------|-----|
| b7 to b0 | Timer mode                                 | Counts timer RB prescaler underflows                                | 00h to FFh    | R/W |
|          | Programmable waveform generation mode      | Counts timer RB prescaler underflows <sup>(1)</sup>                 | 00h to FFh    | R/W |
|          | Programmable one-shot generation mode      | Counts timer RB prescaler underflows (one-shot width is counted)    | 00h to FFh    | R/W |
|          | Programmable wait one-shot generation mode | Counts timer RB prescaler underflows (wait period width is counted) | 00h to FFh    | R/W |

Note:

1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

### 17.3 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 17.2 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.

**Table 17.2 Timer Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Count sources                       | f1, f2, f8, timer RA underflow  |
| Count operations                    | <ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).</li> </ul>  |
| Divide ratio                        | $1/(n+1)(m+1)$<br>n: setting value in TRBPRES register, m: setting value in TRBPR register  |
| Count start condition               | 1 (count starts) is written to the TSTART bit in the TRBCR register.  |
| Count stop conditions               | <ul style="list-style-type: none"> <li>0 (count stops) is written to the TSTART bit in the TRBCR register.</li> <li>1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.</li> </ul>   |
| Interrupt request generation timing | When timer RB underflows [timer RB interrupt].  |
| TRBO pin function                   | Programmable I/O port   |
| INT0 pin function                   | Programmable I/O port or $\overline{\text{INT0}}$ interrupt input   |
| Read from timer                     | The count value can be read out by reading registers TRBPR and TRBPRES.   |
| Write to timer                      | <ul style="list-style-type: none"> <li>When registers TRBPRES and TRBPR are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRBPRES and TRBPR are written to while count operation is in progress:<br/>               If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter.<br/>               If the TWRC bit is set to 1, the value is written to the reload register only.<br/>               (Refer to <b>17.3.2 Timer Write Control during Count Operation.</b>)</li> </ul> |

#### 17.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

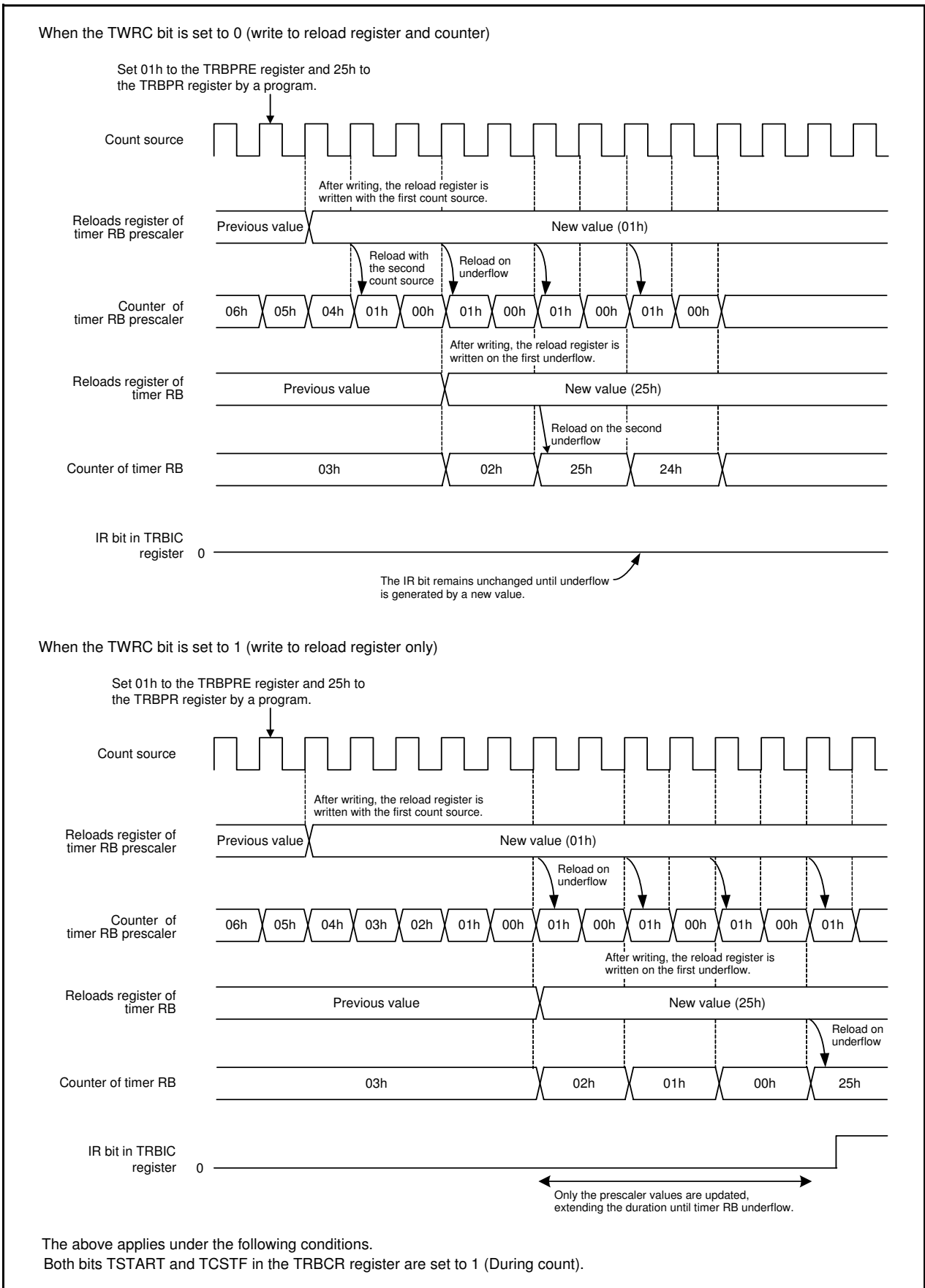
| Bit         | b7 | b6 | b5 | b4 | b3     | b2     | b1    | b0   |
|-------------|----|----|----|----|--------|--------|-------|------|
| Symbol      | —  | —  | —  | —  | INOSEG | INOSTG | TOCNT | TOPL |
| After Reset | 0  | 0  | 0  | 0  | 0      | 0      | 0     | 0    |

| Bit | Symbol | Bit Name  | Function                | R/W |
|-----|--------|---|-------------------------|-----|
| b0  | TOPL   | Timer RB output level select bit  | Set to 0 in timer mode. | R/W |
| b1  | TOCNT  | Timer RB output switch bit  |                         | R/W |
| b2  | INOSTG | One-shot trigger control bit  |                         | R/W |
| b3  | INOSEG | One-shot trigger polarity select bit                                      |                         | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                         | —   |
| b5  | —      |   |                         |     |
| b6  | —      |   |                         |     |
| b7  | —      |   |                         |     |

### 17.3.2 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 17.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.



**Figure 17.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation**



## 17.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to Table 17.3 Programmable Waveform Generation Mode Specifications). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.

Figure 17.3 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

**Table 17.3 Programmable Waveform Generation Mode Specifications**

| Item                                  | Specification   |
|---------------------------------------|---|
| Count sources                         | f1, f2, f8, timer RA underflow  |
| Count operations                      | <ul style="list-style-type: none"> <li>Decrement</li> <li>When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.</li> </ul>  |
| Width and period of output waveform   | Primary period: $(n+1)(m+1)/f_i$<br>Secondary period: $(n+1)(p+1)/f_i$<br>Period: $(n+1)\{(m+1)+(p+1)\}/f_i$<br>$f_i$ : Count source frequency<br>$n$ : Value set in TRBPRES register<br>$m$ : Value set in TRBPR register<br>$p$ : Value set in TRBSC register   |
| Count start condition                 | 1 (count start) is written to the TSTART bit in the TRBCR register.   |
| Count stop conditions                 | <ul style="list-style-type: none"> <li>0 (count stop) is written to the TSTART bit in the TRBCR register.</li> <li>1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.</li> </ul>  |
| Interrupt request generation timing   | In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]  |
| TRBO pin function                     | Programmable output port or pulse output  |
| $\overline{\text{INT0}}$ pin function | Programmable I/O port or $\overline{\text{INT0}}$ interrupt input   |
| Read from timer                       | The count value can be read out by reading registers TRBPR and TRBPRES (1).   |
| Write to timer                        | <ul style="list-style-type: none"> <li>When registers TRBPRES, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRBPRES, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)</li> </ul>  |
| Selectable functions                  | <ul style="list-style-type: none"> <li>Output level select function<br/>The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register.</li> <li>TRBO pin output switch function<br/>Timer RB pulse output or P1_3 latch output is selected by the TOCNT bit in the TRBIOC register. (3)</li> </ul> |

Notes:

- Even when counting the secondary period, the TRBPR register may be read.
- The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
- The value written to the TOCNT bit is enabled by the following.
  - When counting starts.
  - When a timer RB interrupt request is generated.
 The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

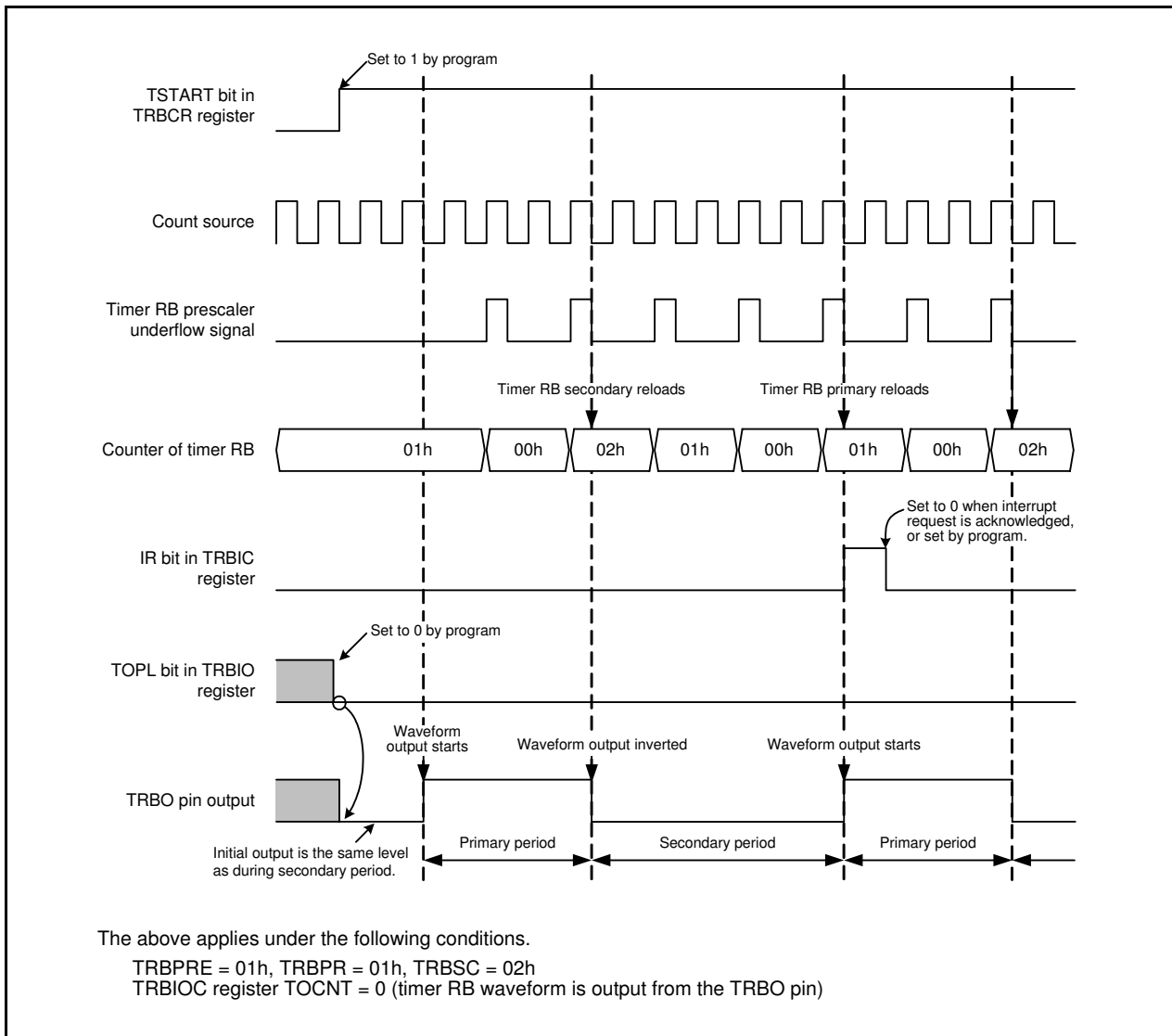
### 17.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

|             |    |    |    |    |        |        |       |      |
|-------------|----|----|----|----|--------|--------|-------|------|
| Bit         | b7 | b6 | b5 | b4 | b3     | b2     | b1    | b0   |
| Symbol      | —  | —  | —  | —  | INOSEG | INOSTG | TOCNT | TOPL |
| After Reset | 0  | 0  | 0  | 0  | 0      | 0      | 0     | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TOPL   | Timer RB output level select bit  | 0: Outputs "H" for primary period<br>Outputs "L" for secondary period<br>Outputs "L" when the timer is stopped<br>1: Outputs "L" for primary period<br>Outputs "H" for secondary period<br>Outputs "H" when the timer is stopped | R/W |
| b1  | TOCNT  | Timer RB output switch bit  | 0: Outputs timer RB waveform<br>1: Outputs value in P1_3 port register   | R/W |
| b2  | INOSTG | One-shot trigger control bit  | Set to 0 in programmable waveform generation mode.   | R/W |
| b3  | INOSEG | One-shot trigger polarity select bit                                      |  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

### 17.4.2 Operating Example



**Figure 17.3 Operating Example of Timer RB in Programmable Waveform Generation Mode**

## 17.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the  $\overline{\text{INT0}}$  pin) (refer to **Table 17.4 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.

Figure 17.4 shows an Operating Example of Programmable One-Shot Generation Mode.

**Table 17.4 Programmable One-Shot Generation Mode Specifications**

| Item                                   | Specification   |
|--|---|
| Count sources                          | f1, f2, f8, timer RA underflow  |
| Count operations                       | <ul style="list-style-type: none"> <li>Decrement the setting value in the TRBPR register</li> <li>When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops).</li> <li>When the count stops, the timer reloads the contents of the reload register before it stops.</li> </ul>  |
| One-shot pulse output time             | $(n+1)(m+1)/f_i$<br>$f_i$ : Count source frequency,<br>$n$ : Setting value in TRBPRE register, $m$ : Setting value in TRBPR register  |
| Count start conditions                 | <ul style="list-style-type: none"> <li>The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated</li> <li>Set the TOSST bit in the TRBOCR register to 1 (one-shot starts)</li> <li>Input trigger to the <math>\overline{\text{INT0}}</math> pin</li> </ul>  |
| Count stop conditions                  | <ul style="list-style-type: none"> <li>When reloading completes after timer RB underflows during primary period</li> <li>When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops)</li> <li>When the TSTART bit in the TRBCR register is set to 0 (stops counting)</li> <li>When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)</li> </ul>  |
| Interrupt request generation timing    | In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]   |
| TRBO pin function                      | Pulse output  |
| $\overline{\text{INT0}}$ pin functions | <ul style="list-style-type: none"> <li>When the INOSTG bit in the TRBIOC register is set to 0 (<math>\overline{\text{INT0}}</math> one-shot trigger disabled): programmable I/O port or <math>\overline{\text{INT0}}</math> interrupt input</li> <li>When the INOSTG bit in the TRBIOC register is set to 1 (<math>\overline{\text{INT0}}</math> one-shot trigger enabled): external trigger (<math>\overline{\text{INT0}}</math> interrupt input)</li> </ul> |
| Read from timer                        | The count value can be read out by reading registers TRBPR and TRBPRE.  |
| Write to timer                         | <ul style="list-style-type: none"> <li>When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter.</li> <li>When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload) <sup>(1)</sup>.</li> </ul>  |
| Selectable functions                   | <ul style="list-style-type: none"> <li>Output level select function<br/>The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register.</li> <li>One-shot trigger select function<br/>Refer to <b>17.5.3 One-Shot Trigger Selection</b>.</li> </ul>   |

Note:

- The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

### 17.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

Address 010Ah

| Bit         | b7 | b6 | b5 | b4 | b3     | b2     | b1    | b0   |
|-------------|----|----|----|----|--------|--------|-------|------|
| Symbol      | —  | —  | —  | —  | INOSEG | INOSTG | TOCNT | TOPL |
| After Reset | 0  | 0  | 0  | 0  | 0      | 0      | 0     | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TOPL   | Timer RB output level select bit  | 0: Outputs one-shot pulse "H"<br>Outputs "L" when the timer is stopped<br>1: Outputs one-shot pulse "L"<br>Outputs "H" when the timer is stopped | R/W |
| b1  | TOCNT  | Timer RB output switch bit  | Set to 0 in programmable one-shot generation mode.   | R/W |
| b2  | INOSTG | One-shot trigger control bit <sup>(1)</sup>                               | 0: $\overline{\text{INT0}}$ pin one-shot trigger disabled<br>1: $\overline{\text{INT0}}$ pin one-shot trigger enabled                            | R/W |
| b3  | INOSEG | One-shot trigger polarity select bit <sup>(1)</sup>                       | 0: Falling edge trigger<br>1: Rising edge trigger  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Note:

1. Refer to **17.5.3 One-Shot Trigger Selection**.

## 17.5.2 Operating Example

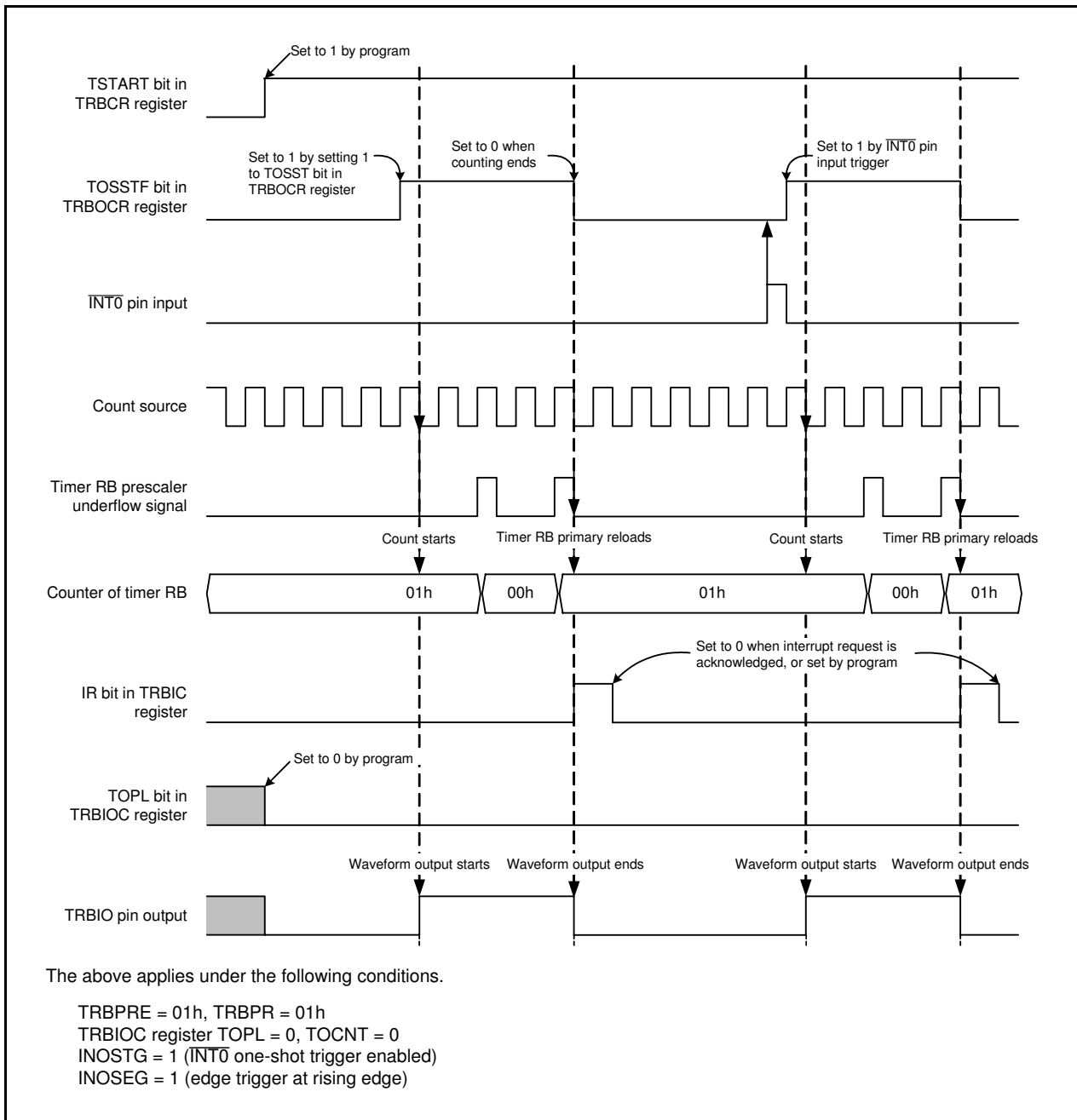


Figure 17.4 Operating Example of Programmable One-Shot Generation Mode

### 17.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).

A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the  $\overline{\text{INT0}}$  pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the  $\overline{\text{INT0}}$  pin, input the trigger after making the following settings:

- Set the PD4\_5 bit in the PD4 register to 0 (input port).
- Select the  $\overline{\text{INT0}}$  digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ( $\overline{\text{INT0}}$  pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the  $\overline{\text{INT0}}$  pin.

- Processing to handle the interrupts is required. Refer to **11. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect  $\overline{\text{INT0}}$  interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

## 17.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the  $\overline{\text{INT0}}$  pin) (refer to **Table 17.5 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.

Figure 17.5 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

**Table 17.5 Programmable Wait One-Shot Generation Mode Specifications**

| Item                                   | Specification   |
|--|---|
| Count sources                          | f1, f2, f8, timer RA underflow  |
| Count operations                       | <ul style="list-style-type: none"> <li>Decrement the timer RB primary setting value.</li> <li>When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues.</li> <li>When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops).</li> <li>When the count stops, the timer reloads the contents of the reload register before it stops.</li> </ul> |
| Wait time                              | $(n+1)(m+1)/f_i$<br>$f_i$ : Count source frequency<br>$n$ : Value set in the TRBPRES register, $m$ : Value set in the TRBPR register  |
| One-shot pulse output time             | $(n+1)(p+1)/f_i$<br>$f_i$ : Count source frequency<br>$n$ : Value set in the TRBPRES register, $p$ : Value set in the TRBSC register  |
| Count start conditions                 | <ul style="list-style-type: none"> <li>The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated.</li> <li>Set the TOSST bit in the TRBOCR register to 1 (one-shot starts).</li> <li>Input trigger to the <math>\overline{\text{INT0}}</math> pin</li> </ul>  |
| Count stop conditions                  | <ul style="list-style-type: none"> <li>When reloading completes after timer RB underflows during secondary period.</li> <li>When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops).</li> <li>When the TSTART bit in the TRBCR register is set to 0 (starts counting).</li> <li>When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).</li> </ul>   |
| Interrupt request generation timing    | In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].  |
| TRBO pin function                      | Pulse output  |
| $\overline{\text{INT0}}$ pin functions | <ul style="list-style-type: none"> <li>When the INOSTG bit in the TRBIOC register is set to 0 (<math>\overline{\text{INT0}}</math> one-shot trigger disabled): programmable I/O port or <math>\overline{\text{INT0}}</math> interrupt input</li> <li>When the INOSTG bit in the TRBIOC register is set to 1 (<math>\overline{\text{INT0}}</math> one-shot trigger enabled): external trigger (<math>\overline{\text{INT0}}</math> interrupt input)</li> </ul>   |
| Read from timer                        | The count value can be read out by reading registers TRBPR and TRBPRES.   |
| Write to timer                         | <ul style="list-style-type: none"> <li>When registers TRBPRES, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter.</li> <li>When registers TRBPRES, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. <sup>(1)</sup></li> </ul>  |
| Selectable functions                   | <ul style="list-style-type: none"> <li>Output level select function<br/>The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register.</li> <li>One-shot trigger select function<br/>Refer to <b>17.5.3 One-Shot Trigger Selection</b>.</li> </ul>   |

Note:

- The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.



### 17.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

Address 010Ah

| Bit         | b7 | b6 | b5 | b4 | b3     | b2     | b1    | b0   |
|-------------|----|----|----|----|--------|--------|-------|------|
| Symbol      | —  | —  | —  | —  | INOSEG | INOSTG | TOCNT | TOPL |
| After Reset | 0  | 0  | 0  | 0  | 0      | 0      | 0     | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TOPL   | Timer RB output level select bit  | 0: Outputs one-shot pulse "H"<br>Outputs "L" when the timer stops or during wait<br>1: Outputs one-shot pulse "L"<br>Outputs "H" when the timer stops or during wait | R/W |
| b1  | TOCNT  | Timer RB output switch bit  | Set to 0 in programmable wait one-shot generation mode.  | R/W |
| b2  | INOSTG | One-shot trigger control bit <sup>(1)</sup>                               | 0: $\overline{\text{INT0}}$ pin one-shot trigger disabled<br>1: $\overline{\text{INT0}}$ pin one-shot trigger enabled  | R/W |
| b3  | INOSEG | One-shot trigger polarity select bit <sup>(1)</sup>                       | 0: Falling edge trigger<br>1: Rising edge trigger  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      |   |  |     |

Note:

1. Refer to **17.5.3 One-Shot Trigger Selection**.

### 17.6.2 Operating Example

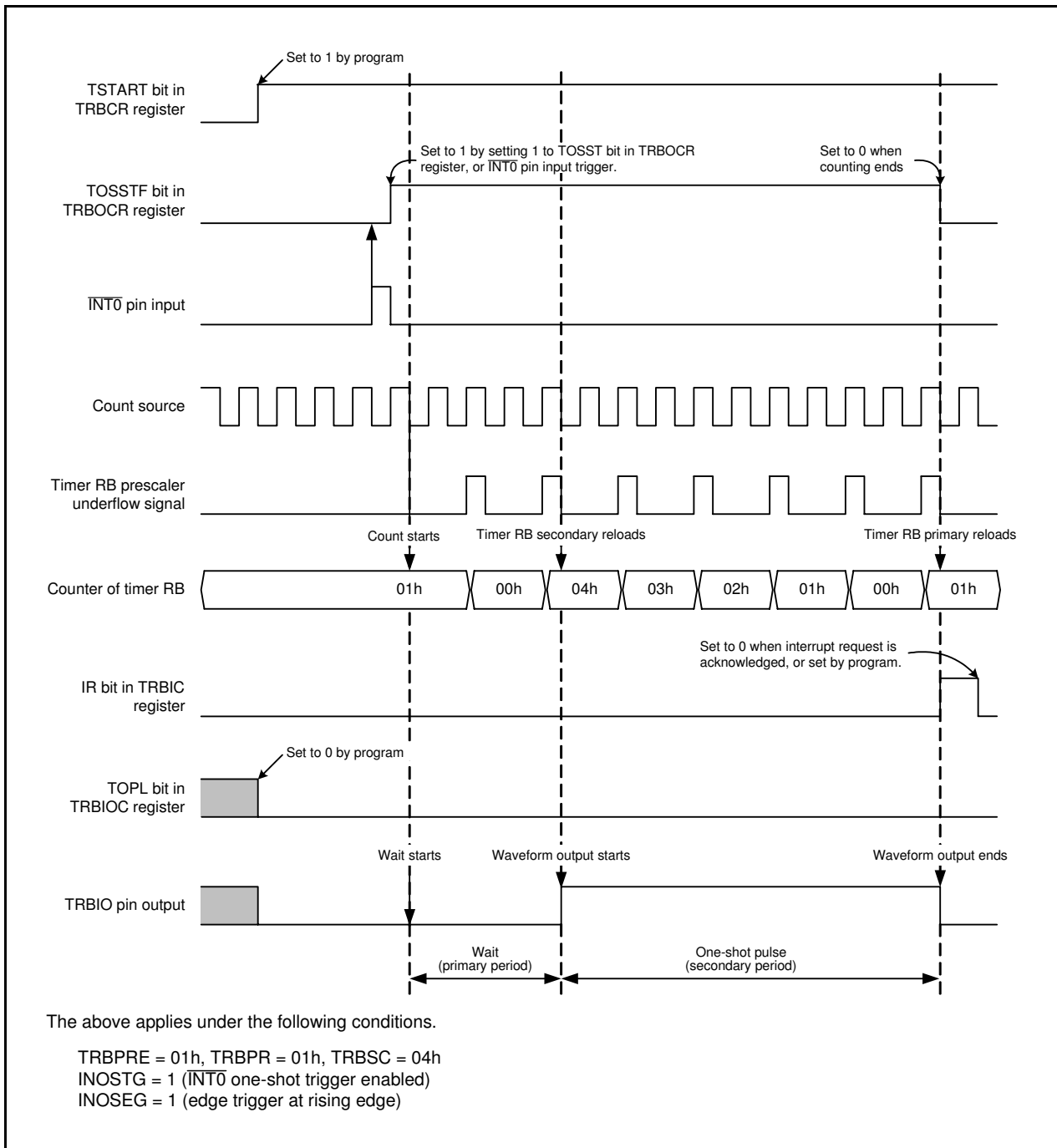


Figure 17.5 Operating Example of Programmable Wait One-Shot Generation Mode

## 17.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

During this time, do not access registers associated with timer RB <sup>(1)</sup> other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.

During this time, do not access registers associated with timer RB <sup>(1)</sup> other than the TCSTF bit.

Note:

1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRES, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

### 17.7.1 Timer Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

### 17.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

### 17.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

### 17.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

## 18. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

### 18.1 Overview

Timer RC uses either f1, fOCO40M or fOCO-F as its operation clock. Table 18.1 lists the Timer RC Operation Clock.

**Table 18.1 Timer RC Operation Clock**

| Condition  | Timer RC Operation Clock |
|--|--------------------------|
| Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b) | f1                       |
| Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)   | fOCO40M                  |
| Count source is fOCO-F (bits TCK2 to TCK0 in TRCCR1 register are set to 111b)  | fOCO-F                   |

Table 18.2 lists the Pin Configuration of Timer RC, and Figure 18.1 shows a Timer RC Block Diagram.

Timer RC has three modes.

- Timer mode

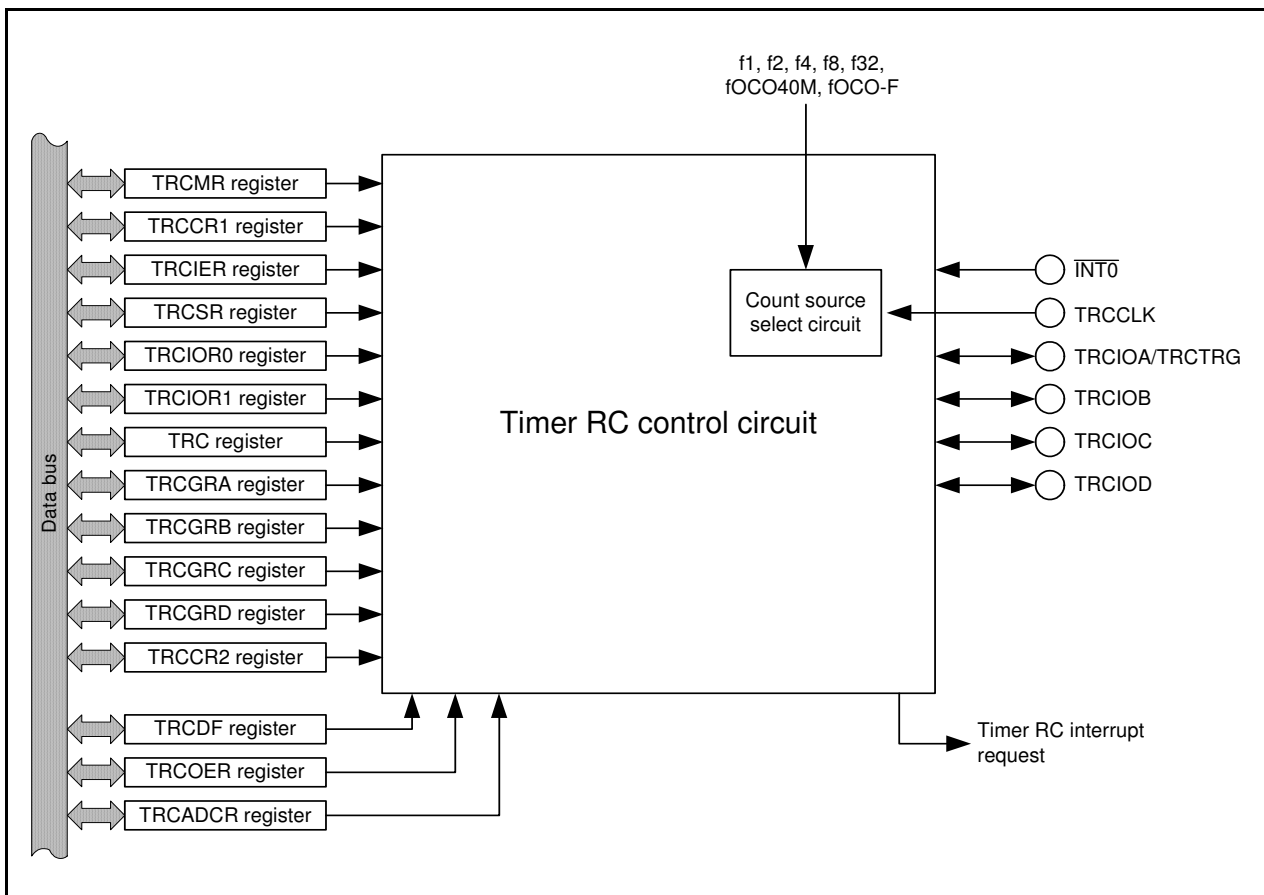
- Input capture function      The counter value is captured to a register, using an external signal as the trigger.
- Output compare function      Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function.

- PWM mode      Pulses of a given width are output continuously.
- PWM2 mode      A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.

In PWM2 mode waveforms are output based on a combination of the counter or the register.



**Figure 18.1** Timer RC Block Diagram

**Table 18.2** Pin Configuration of Timer RC

| Pin Name | Assigned Pin        | I/O   | Function  |
|----------|---------------------|-------|---|
| TRCIOA   | P0_1, P0_2, or P1_1 | I/O   | Function differs according to the mode. Refer to descriptions of individual modes for details |
| TRCIOB   | P1_2                |       |   |
| TRCIOC   | P0_7, P1_3, or P3_4 |       |   |
| TRCIOD   | P0_6, P1_0, or P3_5 |       |   |
| TRCLK    | P1_4 or P3_3        | Input | External clock input  |
| TRCTR    | P0_1, P0_2, or P1_1 | Input | PWM2 mode external trigger input  |

## 18.2 Registers

Table 18.3 lists the Registers Associated with Timer RC.

**Table 18.3 Registers Associated with Timer RC**

| Address        | Symbol  | Mode                   |                         |       |       | Related Information  |
|----------------|---------|------------------------|-------------------------|-------|-------|--|
|                |         | Timer                  |                         | PWM   | PWM2  |  |
|                |         | Input Capture Function | Output Compare Function |       |       |  |
| 0008h          | MSTCR   | Valid                  | Valid                   | Valid | Valid | 18.2.1 Module Standby Control Register (MSTCR)   |
| 0120h          | TRCMR   | Valid                  | Valid                   | Valid | Valid | 18.2.2 Timer RC Mode Register (TRCMR)  |
| 0121h          | TRCCR1  | Valid                  | Valid                   | Valid | Valid | Timer RC control register 1<br>18.2.3 Timer RC Control Register 1 (TRCCR1)<br>18.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function<br>18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode<br>18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode   |
| 0122h          | TRCIER  | Valid                  | Valid                   | Valid | Valid | 18.2.4 Timer RC Interrupt Enable Register (TRCIER)   |
| 0123h          | TRCSR   | Valid                  | Valid                   | Valid | Valid | 18.2.5 Timer RC Status Register (TRCSR)  |
| 0124h          | TRCIOR0 | Valid                  | Valid                   | –     | –     | Timer RC I/O control register 0, timer RC I/O control register 1<br>18.2.6 Timer RC I/O Control Register 0 (TRCIOR0)<br>18.2.7 Timer RC I/O Control Register 1 (TRCIOR1)<br>18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function<br>18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function<br>18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function<br>18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function |
| 0125h          | TRCIOR1 |                        |                         |       |       |  |
| 0126h<br>0127h | TRC     | Valid                  | Valid                   | Valid | Valid | 18.2.8 Timer RC Counter (TRC)  |
| 0128h<br>0129h | TRCGRA  | Valid                  | Valid                   | Valid | Valid | 18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)  |
| 012Ah<br>012Bh | TRCGRB  |                        |                         |       |       |  |
| 012Ch<br>012Dh | TRCGRC  |                        |                         |       |       |  |
| 012Eh<br>012Fh | TRCGRD  |                        |                         |       |       |  |
| 0130h          | TRCCR2  | –                      | Valid                   | Valid | Valid | 18.2.10 Timer RC Control Register 2 (TRCCR2)   |
| 0131h          | TRCDF   | Valid                  | –                       | –     | Valid | 18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)   |
| 0132h          | TRCOER  | –                      | Valid                   | Valid | Valid | 18.2.12 Timer RC Output Master Enable Register (TRCOER)  |
| 0133h          | TRCADCR | –                      | Valid                   | Valid | Valid | 18.2.13 Timer RC Trigger Control Register (TRCADCR)  |
| 0181h          | TRBRCSR | Valid                  | Valid                   | Valid | Valid | 18.2.14 Timer RC Pin Select Register (TRBRCSR)   |
| 0182h          | TRCPSR0 | Valid                  | Valid                   | Valid | Valid | 18.2.15 Timer RC Pin Select Register 0 (TRCPSR0)   |
| 0183h          | TRCPSR1 | Valid                  | Valid                   | Valid | Valid | 18.2.16 Timer RC Pin Select Register 1 (TRCPSR1)   |

–: Invalid

### 18.2.1 Module Standby Control Register (MSTCR)

Address 0008h

|             |    |    |        |    |    |    |    |    |
|-------------|----|----|--------|----|----|----|----|----|
| Bit         | b7 | b6 | b5     | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | MSTTRC | —  | —  | —  | —  | —  |
| After Reset | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  |

| Bit | Symbol | Bit Name  | Function                               | R/W |
|-----|--------|---|--|-----|
| b0  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b1  | —      |   |  |     |
| b2  | —      |   |  |     |
| b3  | —      | Reserved bits   | Set to 0.                              | R/W |
| b4  | —      |   |  |     |
| b5  | MSTTRC | Timer RC standby bit  | 0: Active<br>1: Standby <sup>(1)</sup> | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b7  | —      |   |  |     |

Note:

- When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.

### 18.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

|             |        |    |     |     |      |      |      |      |
|-------------|--------|----|-----|-----|------|------|------|------|
| Bit         | b7     | b6 | b5  | b4  | b3   | b2   | b1   | b0   |
| Symbol      | TSTART | —  | BFD | BFC | PWM2 | PWMD | PWMC | PWMB |
| After Reset | 0      | 1  | 0   | 0   | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | PWMB   | PWM mode of TRCIOB select bit <sup>(1)</sup>                              | 0: Timer mode<br>1: PWM mode                                 | R/W |
| b1  | PWMC   | PWM mode of TRCIOC select bit <sup>(1)</sup>                              | 0: Timer mode<br>1: PWM mode                                 | R/W |
| b2  | PWMD   | PWM mode of TRCIOD select bit <sup>(1)</sup>                              | 0: Timer mode<br>1: PWM mode                                 | R/W |
| b3  | PWM2   | PWM2 mode select bit  | 0: PWM 2 mode<br>1: Timer mode or PWM mode                   | R/W |
| b4  | BFC    | TRCGRC register function select bit <sup>(2)</sup>                        | 0: General register<br>1: Buffer register of TRCGRA register | R/W |
| b5  | BFD    | TRCGRD register function select bit                                       | 0: General register<br>1: Buffer register of TRCGRB register | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |  | —   |
| b7  | TSTART | TRC count start bit   | 0: Count stops<br>1: Count starts                            | R/W |

Notes:

- These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
- Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.



### 18.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

| Bit         | b7   | b6   | b5   | b4   | b3  | b2  | b1  | b0  |
|-------------|------|------|------|------|-----|-----|-----|-----|
| Symbol      | CCLR | TCK2 | TCK1 | TCK0 | TOD | TOC | TOB | TOA |
| After Reset | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name                                      | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | TOA    | TRCIOA output level select bit <sup>(1)</sup> | Function varies according to the operating mode (function).   | R/W |
| b1  | TOB    | TRCIOB output level select bit <sup>(1)</sup> |   | R/W |
| b2  | TOC    | TRCIOC output level select bit <sup>(1)</sup> |   | R/W |
| b3  | TOD    | TRCIOD output level select bit <sup>(1)</sup> |   | R/W |
| b4  | TCK0   | Count source select bit <sup>(1)</sup>        | b6 b5 b4<br>0 0 0: f1<br>0 0 1: f2<br>0 1 0: f4<br>0 1 1: f8<br>1 0 0: f32<br>1 0 1: TRCCLK input rising edge<br>1 1 0: fOCO40M<br>1 1 1: fOCO-F <sup>(2)</sup> | R/W |
| b5  | TCK1   |   |   | R/W |
| b6  | TCK2   |   |   | R/W |
| b7  | CCLR   | TRC counter clear select bit                  | 0: Disable clear (free-running operation)<br>1: Clear TRC counter by input capture or by compare match in TRCGRA  | R/W |

Notes:

1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

### 18.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

| Bit         | b7   | b6 | b5 | b4 | b3    | b2    | b1    | b0    |
|-------------|------|----|----|----|-------|-------|-------|-------|
| Symbol      | OVIE | —  | —  | —  | IMIED | IMIEC | IMIEB | IMIEA |
| After Reset | 0    | 1  | 1  | 1  | 0     | 0     | 0     | 0     |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | IMIEA  | Input capture / compare match interrupt enable bit A                      | 0: Disable interrupt (IMIA) by the IMFA bit<br>1: Enable interrupt (IMIA) by the IMFA bit | R/W |
| b1  | IMIEB  | Input capture / compare match interrupt enable bit B                      | 0: Disable interrupt (IMIB) by the IMFB bit<br>1: Enable interrupt (IMIB) by the IMFB bit | R/W |
| b2  | IMIEC  | Input capture / compare match interrupt enable bit C                      | 0: Disable interrupt (IMIC) by the IMFC bit<br>1: Enable interrupt (IMIC) by the IMFC bit | R/W |
| b3  | IMIED  | Input capture / compare match interrupt enable bit D                      | 0: Disable interrupt (IMID) by the IMFD bit<br>1: Enable interrupt (IMID) by the IMFD bit | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | OVIE   | Overflow interrupt enable bit   | 0: Disable interrupt (OVI) by the OVF bit<br>1: Enable interrupt (OVI) by the OVF bit     | R/W |

### 18.2.5 Timer RC Status Register (TRCSR)

Address 0123h

|             |     |    |    |    |      |      |      |      |
|-------------|-----|----|----|----|------|------|------|------|
| Bit         | b7  | b6 | b5 | b4 | b3   | b2   | b1   | b0   |
| Symbol      | OVF | —  | —  | —  | IMFD | IMFC | IMFB | IMFA |
| After Reset | 0   | 1  | 1  | 1  | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | IMFA   | Input capture / compare match flag A                                      | [Source for setting this bit to 0]  | R/W |
| b1  | IMFB   | Input capture / compare match flag B                                      | Write 0 after read <sup>(1)</sup> .   | R/W |
| b2  | IMFC   | Input capture / compare match flag C                                      | [Source for setting this bit to 1]  | R/W |
| b3  | IMFD   | Input capture / compare match flag D                                      | Refer to <b>Table 18.4 Source for Setting Bit of Each Flag to 1.</b>  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | OVF    | Overflow flag   | [Source for setting this bit to 0]<br>Write 0 after read <sup>(1)</sup> .<br>[Source for setting this bit to 1]<br>Refer to <b>Table 18.4 Source for Setting Bit of Each Flag to 1.</b> | R/W |

Note:

1. The writing results are as follows:

- This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
- This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
- This bit remains unchanged if 1 is written to it.

**Table 18.4 Source for Setting Bit of Each Flag to 1**

| Bit Symbol | Timer Mode                           |   | PWM Mode | PWM2 Mode |
|------------|--------------------------------------|---|----------|-----------|
|            | Input capture Function               | Output Compare Function   |          |           |
| IMFA       | TRCIOA pin input edge <sup>(1)</sup> | When the values of the registers TRC and TRCGRA match.                |          |           |
| IMFB       | TRCIOB pin input edge <sup>(1)</sup> | When the values of the registers TRC and TRCGRB match.                |          |           |
| IMFC       | TRCIOC pin input edge <sup>(1)</sup> | When the values of the registers TRC and TRCGRC match. <sup>(2)</sup> |          |           |
| IMFD       | TRCIOD pin input edge <sup>(1)</sup> | When the values of the registers TRC and TRCGRD match. <sup>(2)</sup> |          |           |
| OVF        | When the TRC register overflows.     |   |          |           |

Notes:

1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

### 18.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

| Bit         | b7 | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
|-------------|----|------|------|------|------|------|------|------|
| Symbol      | —  | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 |
| After Reset | 1  | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | IOA0   | TRCGRA control bit  | Function varies according to the operating mode (function). | R/W |
| b1  | IOA1   |   |   | R/W |
| b2  | IOA2   | TRCGRA mode select bit <sup>(1)</sup>                                     | 0: Output compare function<br>1: Input capture function     | R/W |
| b3  | IOA3   | TRCGRA input capture input switch bit <sup>(3)</sup>                      | 0: fOCO128 signal<br>1: TRCIOA pin input                    | R/W |
| b4  | IOB0   | TRCGRB control bit  | Function varies according to the operating mode (function). | R/W |
| b5  | IOB1   |   |   | R/W |
| b6  | IOB2   | TRCGRB mode select bit <sup>(2)</sup>                                     | 0: Output compare function<br>1: Input capture function     | R/W |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |

Notes:

1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

### 18.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

| Bit         | b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
|-------------|------|------|------|------|------|------|------|------|
| Symbol      | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 |
| After Reset | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                              | Function  | R/W |
|-----|--------|---------------------------------------|---|-----|
| b0  | IOC0   | TRCGRC control bit                    | Function varies according to the operating mode (function).         | R/W |
| b1  | IOC1   |                                       |   | R/W |
| b2  | IOC2   | TRCGRC mode select bit <sup>(1)</sup> | 0: Output compare function<br>1: Input capture function             | R/W |
| b3  | IOC3   | TRCGRC register function select bit   | 0: TRCIOA output register<br>1: General register or buffer register | R/W |
| b4  | IOD0   | TRCGRD control bit                    | Function varies according to the operating mode (function).         | R/W |
| b5  | IOD1   |                                       |   | R/W |
| b6  | IOD2   | TRCGRD mode select bit <sup>(2)</sup> | 0: Output compare function<br>1: Input capture function             | R/W |
| b7  | IOD3   | TRCGRD register function select bit   | 0: TRCIOB output register<br>1: General register or buffer register | R/W |

Notes:

1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

### 18.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

|             |     |     |     |     |     |     |    |    |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | —  |
| After Reset | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  |

| Bit       | Function   | Setting Range  | R/W |
|-----------|--|----------------|-----|
| b15 to b0 | Count a count source. Count operation is incremented.<br>When an overflow occurs, the OVF bit in the TRCSR register is set to 1. | 0000h to FFFFh | R/W |

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

### 18.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB), 012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

|             |     |     |     |     |     |     |    |    |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | —  |
| After Reset | 1   | 1   | 1   | 1   | 1   | 1   | 1  | 1  |

| Bit       | Function   | R/W |
|-----------|--|-----|
| b15 to b0 | Function varies according to the operating mode. | R/W |

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

### 18.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

| Bit         | b7    | b6    | b5   | b4 | b3 | b2   | b1   | b0   |
|-------------|-------|-------|------|----|----|------|------|------|
| Symbol      | TCEG1 | TCEG0 | CSEL | —  | —  | POLD | POLC | POLB |
| After Reset | 0     | 0     | 0    | 1  | 1  | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | POLB   | PWM mode output level control bit B <sup>(1)</sup>                        | 0: TRCIOB output level selected as “L” active<br>1: TRCIOB output level selected as “H” active  | R/W |
| b1  | POLC   | PWM mode output level control bit C <sup>(1)</sup>                        | 0: TRCIOC output level selected as “L” active<br>1: TRCIOC output level selected as “H” active  | R/W |
| b2  | POLD   | PWM mode output level control bit D <sup>(1)</sup>                        | 0: TRCIOD output level selected as “L” active<br>1: TRCIOD output level selected as “H” active  | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b4  | —      |   |   |     |
| b5  | CSEL   | TRC count operation select bit <sup>(2)</sup>                             | 0: Count continues at compare match with the TRCGRA register<br>1: Count stops at compare match with the TRCGRA register                            | R/W |
| b6  | TCEG0  | TRCTRIG input edge select bit <sup>(3)</sup>                              | b7 b6<br>0 0: Disable the trigger input from the TRCTRIG pin<br>0 1: Rising edge selected<br>1 0: Falling edge selected<br>1 1: Both edges selected | R/W |
| b7  | TCEG1  |   |   | R/W |

Notes:

1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

### 18.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

| Bit         | b7    | b6    | b5 | b4    | b3  | b2  | b1  | b0  |
|-------------|-------|-------|----|-------|-----|-----|-----|-----|
| Symbol      | DFCK1 | DFCK0 | —  | DFTRG | DFD | DFC | DFB | DFA |
| After Reset | 0     | 0     | 0  | 0     | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | DFA    | TRCIOA pin digital filter function select bit <sup>(1)</sup>              | 0: Function is not used<br>1: Function is used  | R/W |
| b1  | DFB    | TRCIOB pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b2  | DFC    | TRCIOC pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b3  | DFD    | TRCIOD pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b4  | DFTRG  | TRCTRIG pin digital filter function select bit <sup>(2)</sup>             |   | R/W |
| b5  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b6  | DFCK0  | Clock select bits for digital filter function <sup>(1, 2)</sup>           | b7 b6<br>0 0: f32<br>0 1: f8<br>1 0: f1<br>1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register) | R/W |
| b7  | DFCK1  |   |   | R/W |

Notes:

1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRIG trigger input enabled).

### 18.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

| Bit         | b7  | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|-----|----|----|----|----|----|----|----|
| Symbol      | PTO | —  | —  | —  | ED | EC | EB | EA |
| After Reset | 0   | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | EA     | TRCIOA output disable bit <sup>(1)</sup>  | 0: Enable output<br>1: Disable output (The TRCIOA pin is used as a programmable I/O port.)  | R/W |
| b1  | EB     | TRCIOB output disable bit <sup>(1)</sup>  | 0: Enable output<br>1: Disable output (The TRCIOB pin is used as a programmable I/O port.)  | R/W |
| b2  | EC     | TRCIOC output disable bit <sup>(1)</sup>  | 0: Enable output<br>1: Disable output (The TRCIOC pin is used as a programmable I/O port.)  | R/W |
| b3  | ED     | TRCIOD output disable bit <sup>(1)</sup>  | 0: Enable output<br>1: Disable output (The TRCIOD pin is used as a programmable I/O port.)  | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1.       |   | —   |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | PTO    | $\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit | 0: Pulse output forced cutoff input disabled<br>1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when "L" is applied to the $\overline{\text{INT0}}$ pin) | R/W |

Note:

1. These bits are disabled for input pins set to the input capture function.

### 18.2.13 Timer RC Trigger Control Register (TRCADCR)

Address 0133h

| Bit         | b7 | b6 | b5 | b4 | b3      | b2      | b1      | b0      |
|-------------|----|----|----|----|---------|---------|---------|---------|
| Symbol      | —  | —  | —  | —  | ADTRGDE | ADTRGCE | ADTRGBE | ADTRGAE |
| After Reset | 0  | 0  | 0  | 0  | 0       | 0       | 0       | 0       |

| Bit | Symbol  | Bit Name  | Function   | R/W |
|-----|---------|---|--|-----|
| b0  | ADTRGAE | A/D trigger A enable bit  | 0: A/D trigger disabled<br>1: A/D trigger generated at compare match with registers TRC and TRCGRA | R/W |
| b1  | ADTRGBE | A/D trigger B enable bit  | 0: A/D trigger disabled<br>1: A/D trigger generated at compare match with registers TRC and TRCGRB | R/W |
| b2  | ADTRGCE | A/D trigger C enable bit  | 0: A/D trigger disabled<br>1: A/D trigger generated at compare match with registers TRC and TRCGRC | R/W |
| b3  | ADTRGDE | A/D trigger D enable bit  | 0: A/D trigger disabled<br>1: A/D trigger generated at compare match with registers TRC and TRCGRD | R/W |
| b4  | —       | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | —       |   |  |     |
| b6  | —       |   |  |     |
| b7  | —       |   |  |     |

### 18.2.14 Timer RC Pin Select Register (TRBRCSR)

Address 0181h

|             |    |    |            |            |    |    |    |    |
|-------------|----|----|------------|------------|----|----|----|----|
| Bit         | b7 | b6 | b5         | b4         | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | TRCCLKSEL1 | TRCCLKSEL0 | —  | —  | —  | —  |
| After Reset | 0  | 0  | 0          | 0          | 0  | 0  | 0  | 0  |

| Bit | Symbol     | Bit Name  | Function   | R/W |
|-----|------------|---|--|-----|
| b0  | —          | Reserved bits   | Set to 0.  | R/W |
| b1  | —          |   |  | R/W |
| b2  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b3  | —          |   |  | —   |
| b4  | TRCCLKSEL0 | TRCCLK pin select bit   | <sup>b5 b4</sup><br>0 0: TRCCLK pin not used<br>0 1: P1_4 assigned<br>1 0: P3_3 assigned<br>1 1: Do not set. | R/W |
| b5  | TRCCLKSEL1 |   |  | R/W |
| b6  | —          | Reserved bit  | Set to 0.  | R/W |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

The TRBRCSR register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set bits TRCCLKSEL0 and TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of bits TRCCLKSEL0 and TRCCLKSEL1 during timer RC operation.

### 18.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

| Bit         | b7 | b6 | b5 | b4         | b3 | b2         | b1         | b0         |
|-------------|----|----|----|------------|----|------------|------------|------------|
| Symbol      | —  | —  | —  | TRCIOBSEL0 | —  | TRCIOASEL2 | TRCIOASEL1 | TRCIOASEL0 |
| After Reset | 0  | 0  | 0  | 0          | 0  | 0          | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function   | R/W |
|-----|------------|---|--|-----|
| b0  | TRCIOASEL0 | TRCIOA/TRCTRG pin select bit  | b2 b1 b0<br>0 0 0: TRCIOA/TRCTRG pin not used<br>0 0 1: P1_1 assigned<br>0 1 1: P0_1 assigned<br>1 0 0: P0_2 assigned<br>Other than above: Do not set. | R/W |
| b1  | TRCIOASEL1 |   |  | R/W |
| b2  | TRCIOASEL2 |   |  | R/W |
| b3  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | TRCIOBSEL0 | TRCIOB pin select bit   | 0: TRCIOB pin not used<br>1: P1_2 assigned   | R/W |
| b5  | —          | Reserved bits   | Set to 0.  | R/W |
| b6  | —          |   |  |     |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

### 18.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

| Bit         | b7 | b6 | b5         | b4         | b3 | b2 | b1         | b0         |
|-------------|----|----|------------|------------|----|----|------------|------------|
| Symbol      | —  | —  | TRCIODSEL1 | TRCIODSEL0 | —  | —  | TRCIOCSEL1 | TRCIOCSEL0 |
| After Reset | 0  | 0  | 0          | 0          | 0  | 0  | 0          | 0          |

| Bit | Symbol     | Bit Name  | Function  | R/W |
|-----|------------|---|---|-----|
| b0  | TRCIOCSEL0 | TRCIOC pin select bit   | b1 b0<br>0 0: TRCIOC pin not used<br>0 1: P1_3 assigned<br>1 0: P3_4 assigned<br>1 1: P0_7 assigned | R/W |
| b1  | TRCIOCSEL1 |   |   | R/W |
| b2  | —          | Reserved bit  | Set to 0.   | R/W |
| b3  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | TRCIODSEL0 | TRCIOD pin select bit   | b5 b4<br>0 0: TRCIOD pin not used<br>0 1: P1_0 assigned<br>1 0: P3_5 assigned<br>1 1: P0_6 assigned | R/W |
| b5  | TRCIODSEL1 |   |   | R/W |
| b6  | —          | Reserved bit  | Set to 0.   | R/W |
| b7  | —          | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.

Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.



## 18.3 Common Items for Multiple Modes

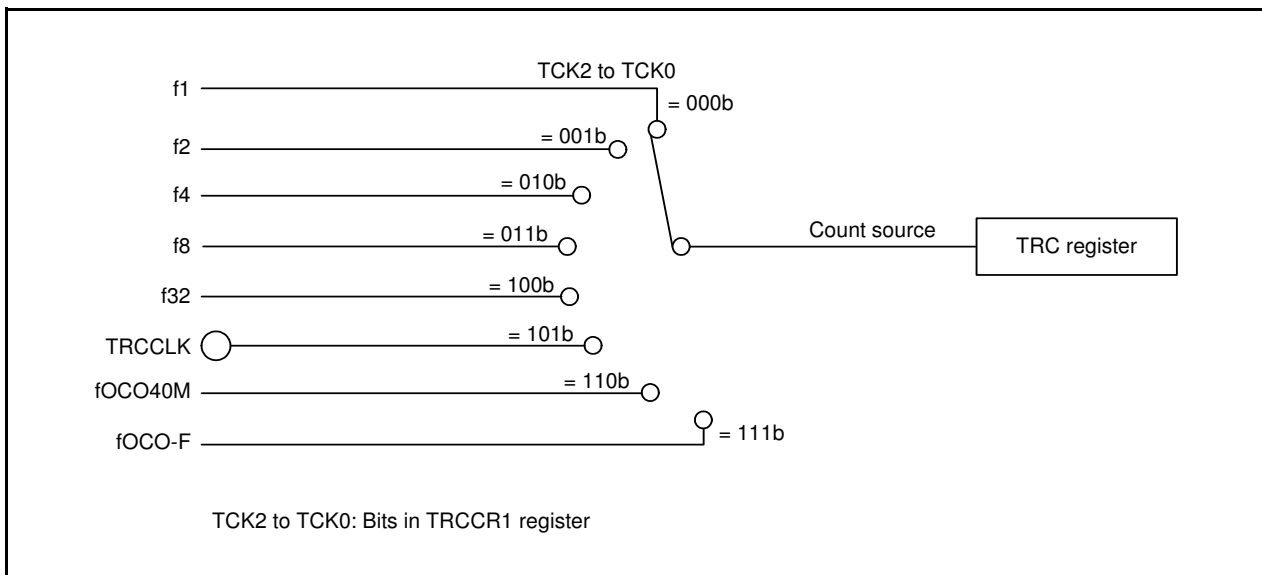
### 18.3.1 Count Source

The method of selecting the count source is common to all modes.

Table 18.5 lists the Count Source Selection, and Figure 18.2 shows a Count Source Block Diagram.

**Table 18.5 Count Source Selection**

| Count Source                           | Selection Method   |
|--|--|
| f1, f2, f4, f8, f32                    | Count source selected using bits TCK2 to TCK0 in TRCCR1 register   |
| fOCO40M<br>fOCO-F                      | FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on)<br>Bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M)<br>Bits TCK2 to TCK0 in TRCCR1 register are set to 111b (fOCO-F)              |
| External signal input<br>to TRCCLK pin | Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge<br>of external clock) and the corresponding direction bit in the corresponding direction<br>register is set is set to 0 (input mode) |



**Figure 18.2 Count Source Block Diagram**

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (see **Table 18.1 Timer RC Operation Clock**).

To select fOCO40M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M) or 111b (fOCO-F).

### 18.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

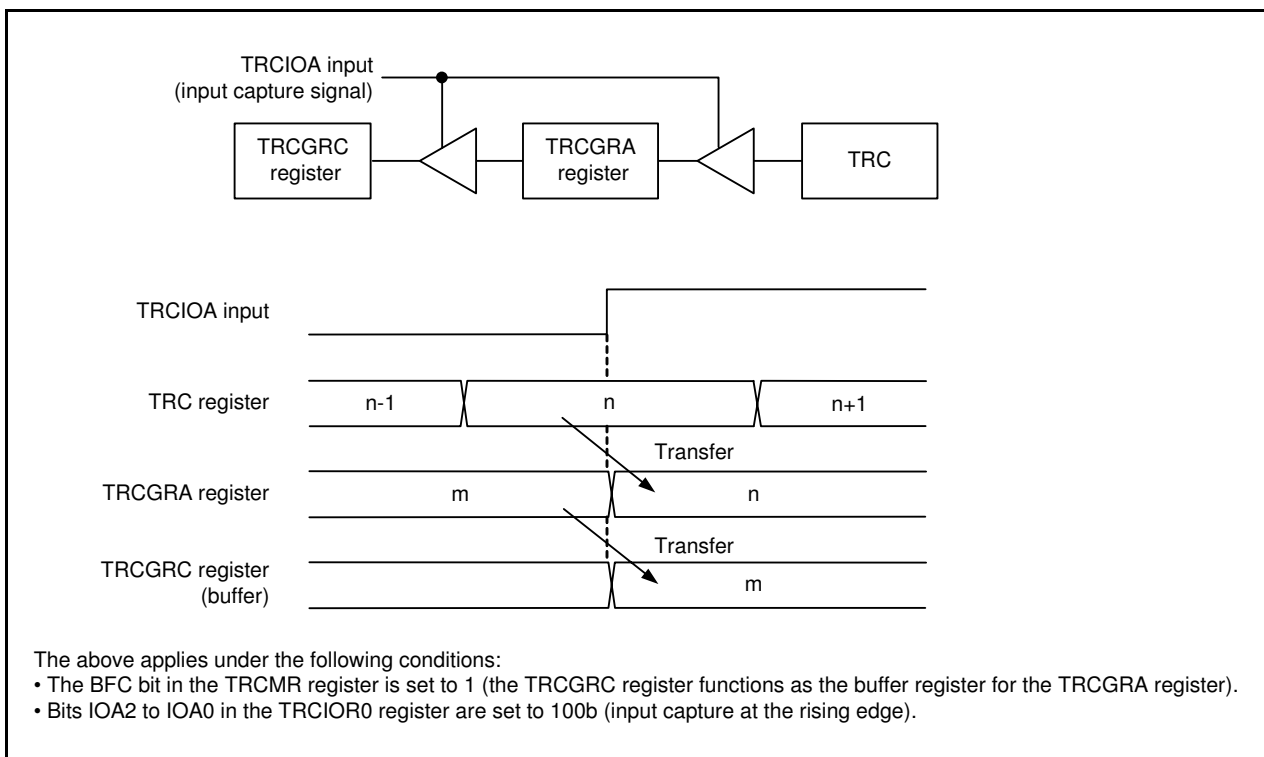
- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

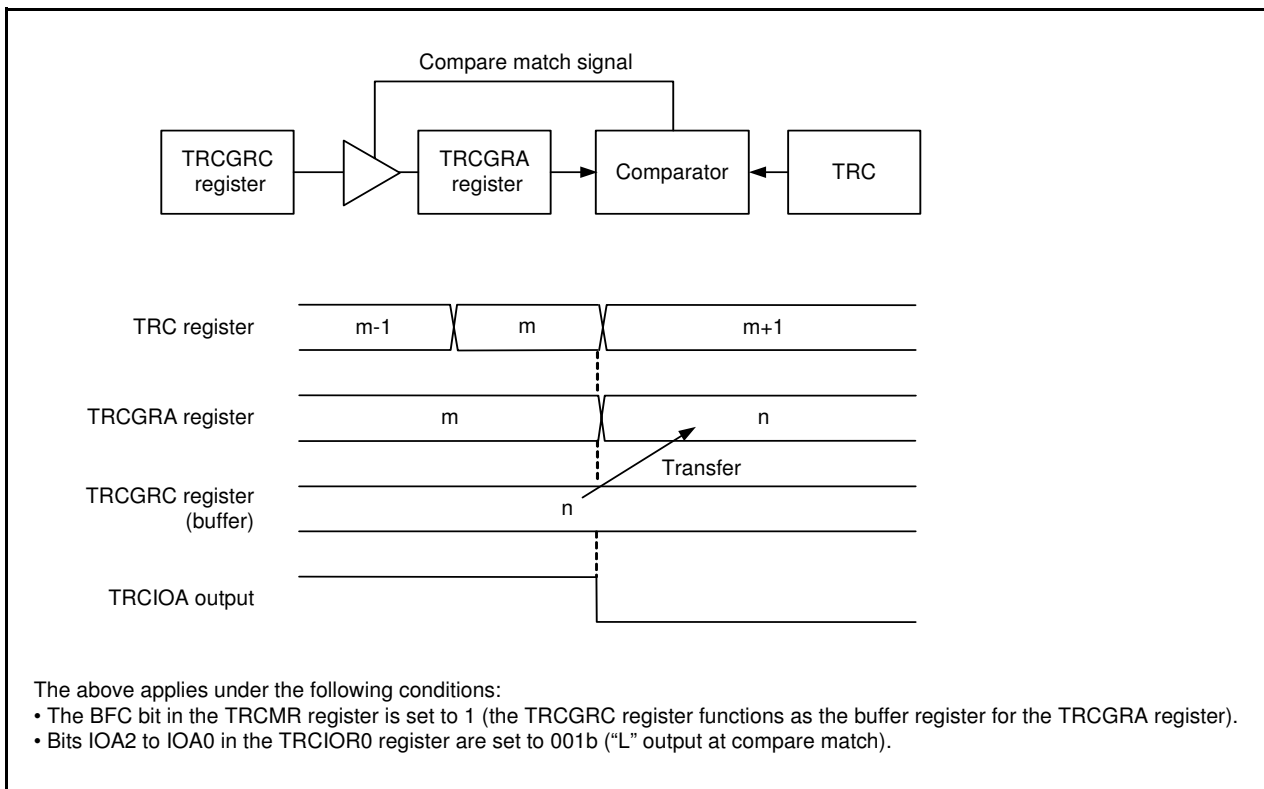
Table 18.6 lists the Buffer Operation in Each Mode, Figure 18.3 shows the Buffer Operation for Input Capture Function, and Figure 18.4 shows the Buffer Operation for Output Compare Function.

**Table 18.6 Buffer Operation in Each Mode**

| Function, Mode          | Transfer Timing   | Transfer Destination Register   |
|-------------------------|---|---|
| Input capture function  | Input capture signal input  | Contents of TRCGRA (TRCGRB) register are transferred to buffer register |
| Output compare function | Compare match between TRC register and TRCGRA (TRCGRB) register   | Contents of buffer register are transferred to TRCGRA (TRCGRB) register |
| PWM mode                |   |   |
| PWM2 mode               | <ul style="list-style-type: none"> <li>• Compare match between TRC register and TRCGRA register</li> <li>• TRCTRIG pin trigger input</li> </ul> | Contents of buffer register (TRCGRD) are transferred to TRCGRB register |



**Figure 18.3 Buffer Operation for Input Capture Function**



**Figure 18.4 Buffer Operation for Output Compare Function**

Make the following settings in timer mode.

- To use the TRCGRC register as the buffer register for the TRCGRA register:  
Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:  
Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The output compare function, PWM mode, or PWM2 mode, and the TRCGRC or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.

The input capture function and the TRCGRC register or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC pin or TRCIOD pin.

### 18.3.3 Digital Filter

The input to TRCTR<sub>j</sub> or TRCIO<sub>j</sub> (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 18.5 shows a Digital Filter Block Diagram.

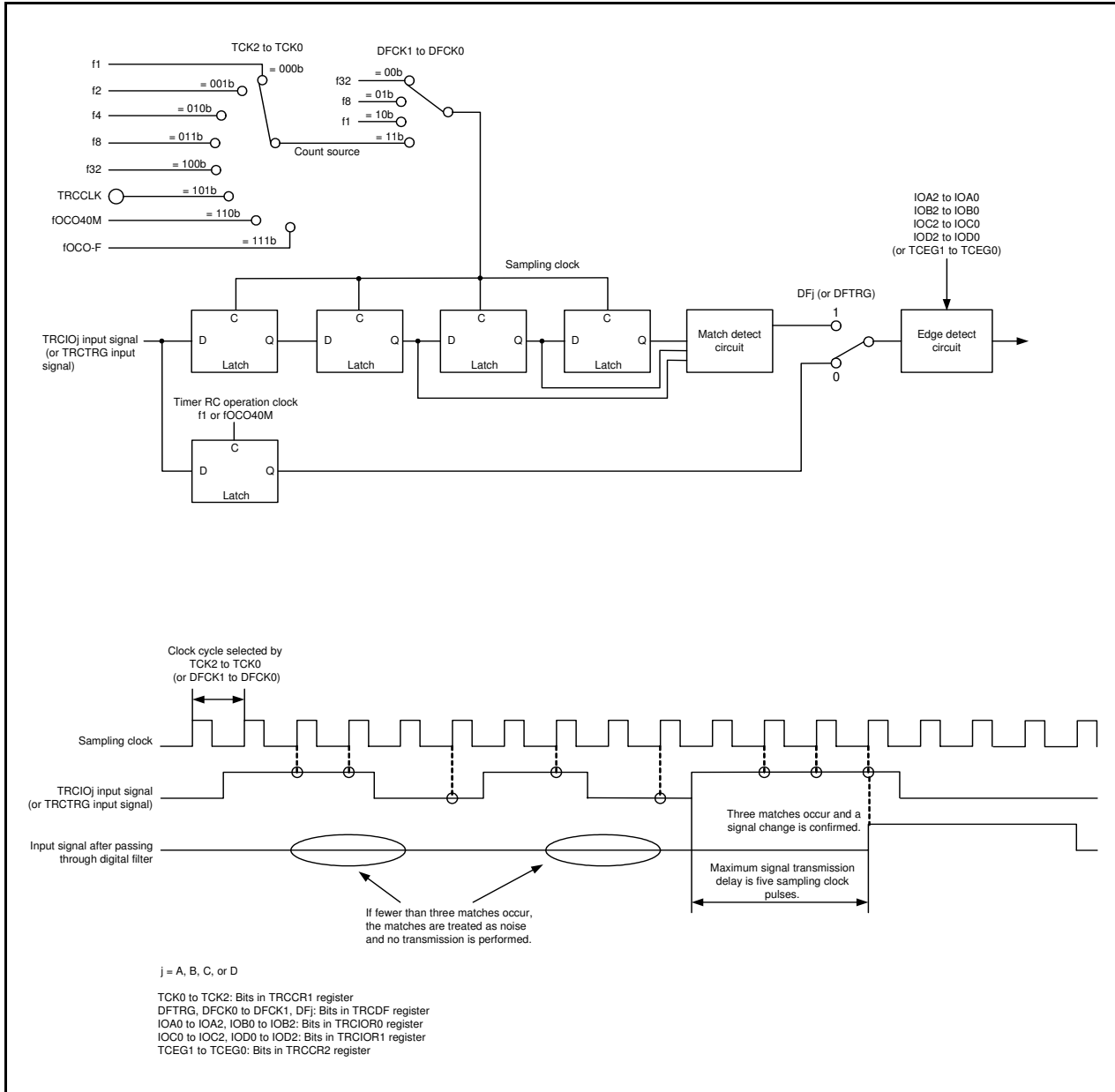


Figure 18.5 Digital Filter Block Diagram

### 18.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the  $\overline{\text{INT0}}$  pin.

A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the  $\overline{\text{INT0}}$  pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input  $\overline{\text{INT0}}$  enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the  $\overline{\text{INT0}}$  pin (refer to **Table 18.1 Timer RC Operation Clock**) has elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function.

- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output). (Refer to **7. I/O Ports**.)
- Set the INT0EN bit in the INTEN register to 1 ( $\overline{\text{INT0}}$  input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INTOIC register to 0 (falling edge selected).
- Set the PD4\_5 bit in the PD4 register to 0 (input mode).
- Select the  $\overline{\text{INT0}}$  digital filter by means of bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input  $\overline{\text{INT0}}$  enabled).

The IR bit in the INTOIC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INTOIC register and the INT0PL bit in the INTEN register and a change in the  $\overline{\text{INT0}}$  pin input (refer to **11.8 Notes on Interrupts**).

For details on interrupts, refer to **11. Interrupts**.

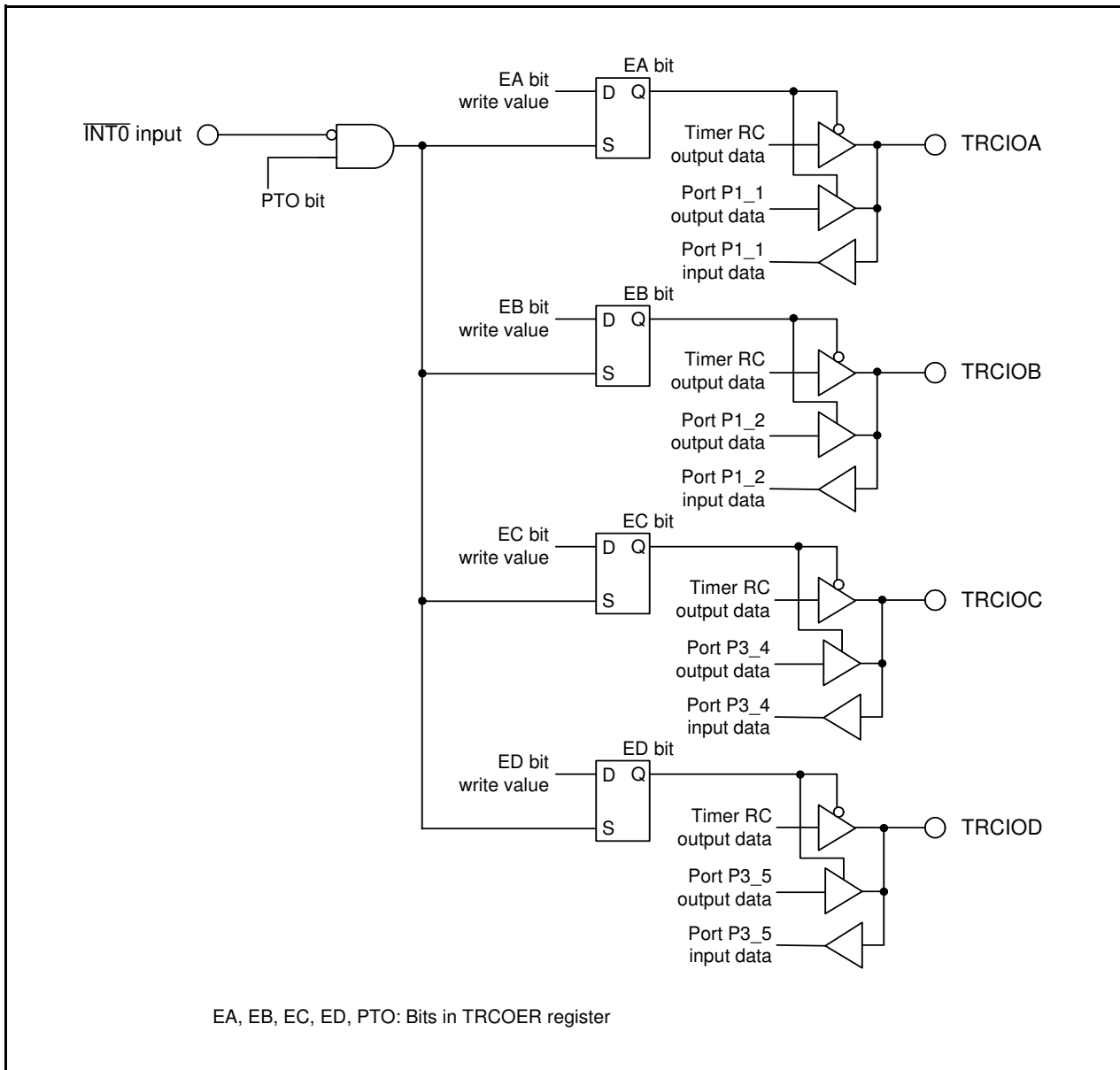


Figure 18.6 Forced Cutoff of Pulse Output

## 18.4 Timer Mode (Input Capture Function)

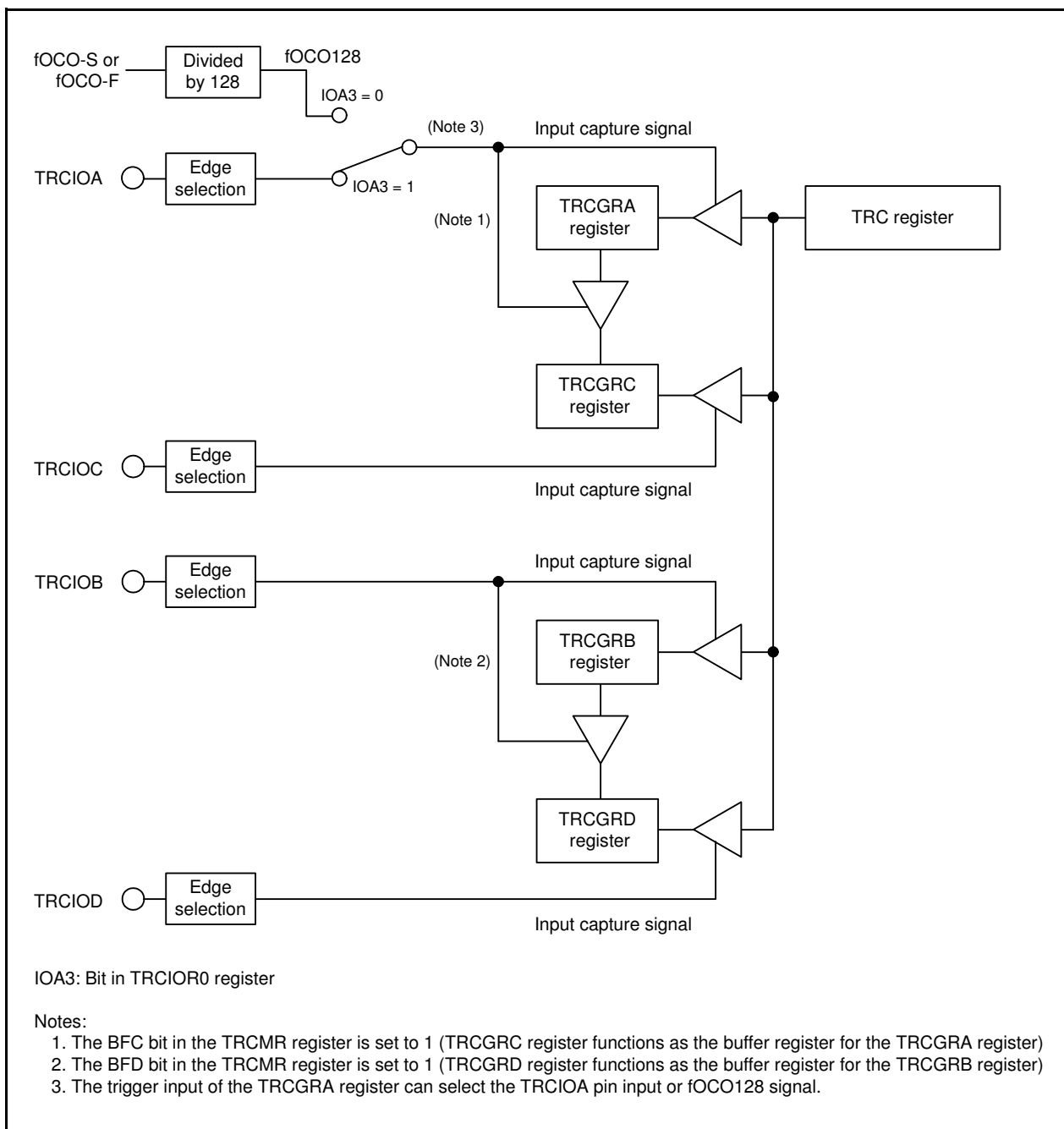
This function measures the width or period of an external signal. An external signal input to the TRCIO<sub>j</sub> (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGR<sub>j</sub> register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. The TRCGRA register can also select fOCO128 signal as input-capture trigger input.

Table 18.7 lists the Specifications of Input Capture Function, Figure 18.7 shows a Block Diagram of Input Capture Function, Table 18.8 lists the Functions of TRCGR<sub>j</sub> Register when Using Input Capture Function, and Figure 18.8 shows an Operating Example of Input Capture Function.

**Table 18.7 Specifications of Input Capture Function**

| Item   | Specification  |
|--|--|
| Count source                                     | f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin   |
| Count operation                                  | Increment  |
| Count period                                     | <ul style="list-style-type: none"> <li>• The CCLR bit in the TRCCR1 register is set to 0 (free running operation):<br/> <math>1/f_k \times 65,536</math><br/>           f<sub>k</sub>: Count source frequency</li> <li>• The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match):<br/> <math>1/f_k \times (n + 1)</math><br/>           n: TRCGRA register setting value</li> </ul>  |
| Count start condition                            | 1 (count starts) is written to the TSTART bit in the TRCMR register.   |
| Count stop condition                             | 0 (count stops) is written to the TSTART bit in the TRCMR register.<br>The TRC register retains a value before count stops.  |
| Interrupt request generation timing              | <ul style="list-style-type: none"> <li>• Input capture (valid edge of TRCIO<sub>j</sub> input or fOCO128 signal edge)</li> <li>• The TRC register overflows.</li> </ul>  |
| TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions | Programmable I/O port or input capture input (selectable individually for each pin)  |
| INT0 pin function                                | Programmable I/O port or INT0 interrupt input  |
| Read from timer                                  | The count value can be read by reading TRC register.   |
| Write to timer                                   | The TRC register can be written to.  |
| Select functions                                 | <ul style="list-style-type: none"> <li>• Input capture input pin selection<br/>One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD</li> <li>• Input capture input valid edge selection<br/>Rising edge, falling edge, or both rising and falling edges</li> <li>• Buffer operation (Refer to <b>18.3.2 Buffer Operation.</b>)</li> <li>• Digital filter (Refer to <b>18.3.3 Digital Filter.</b>)</li> <li>• Timing for setting the TRC register to 0000h<br/>Overflow or input capture</li> <li>• Input-capture trigger selected<br/>fOCO128 can be selected for input-capture trigger input of the TRCGRA register.</li> </ul> |

j = A, B, C, or D



**Figure 18.7 Block Diagram of Input Capture Function**



### 18.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function

Address 0124h

|             |    |      |      |      |      |      |      |      |
|-------------|----|------|------|------|------|------|------|------|
| Bit         | b7 | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | —  | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 |
| After Reset | 1  | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | IOA0   | TRCGRA control bit  | <sup>b1 b0</sup><br>0 0: Input capture to the TRCGRA register at the rising edge<br>0 1: Input capture to the TRCGRA register at the falling edge<br>1 0: Input capture to the TRCGRA register at both edges<br>1 1: Do not set. | R/W |
| b1  | IOA1   |   |  | R/W |
| b2  | IOA2   | TRCGRA mode select bit <sup>(1)</sup>                                     | Set to 1 (input capture) in the input capture function.  | R/W |
| b3  | IOA3   | TRCGRA input capture input switch bit <sup>(3)</sup>                      | 0: fOCO128 signal<br>1: TRCIOA pin input   | R/W |
| b4  | IOB0   | TRCGRB control bit  | <sup>b5 b4</sup><br>0 0: Input capture to the TRCGRB register at the rising edge<br>0 1: Input capture to the TRCGRB register at the falling edge<br>1 0: Input capture to the TRCGRB register at both edges<br>1 1: Do not set. | R/W |
| b5  | IOB1   |   |  | R/W |
| b6  | IOB2   | TRCGRB mode select bit <sup>(2)</sup>                                     | Set to 1 (input capture) in the input capture function.  | R/W |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |  | —   |

## Notes:

1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

### 18.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function

Address 0125h

|             |      |      |      |      |      |      |      |      |
|-------------|------|------|------|------|------|------|------|------|
| Bit         | b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 |
| After Reset | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                              | Function   | R/W |
|-----|--------|---------------------------------------|--|-----|
| b0  | IOC0   | TRCGRC control bit                    | <sup>b1 b0</sup><br>0 0: Input capture to the TRCGRC register at the rising edge<br>0 1: Input capture to the TRCGRC register at the falling edge<br>1 0: Input capture to the TRCGRC register at both edges<br>1 1: Do not set. | R/W |
| b1  | IOC1   |                                       |  | R/W |
| b2  | IOC2   | TRCGRC mode select bit <sup>(1)</sup> | Set to 1 (input capture) in the input capture function.  | R/W |
| b3  | IOC3   | TRCGRC register function select bit   | Set to 1.  | R/W |
| b4  | IOD0   | TRCGRD control bit                    | <sup>b5 b4</sup><br>0 0: Input capture to the TRCGRD register at the rising edge<br>0 1: Input capture to the TRCGRD register at the falling edge<br>1 0: Input capture to the TRCGRD register at both edges<br>1 1: Do not set. | R/W |
| b5  | IOD1   |                                       |  | R/W |
| b6  | IOD2   | TRCGRD mode select bit <sup>(2)</sup> | Set to 1 (input capture) in the input capture function.  | R/W |
| b7  | IOD3   | TRCGRD register function select bit   | Set to 1.  | R/W |

Notes:

- When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

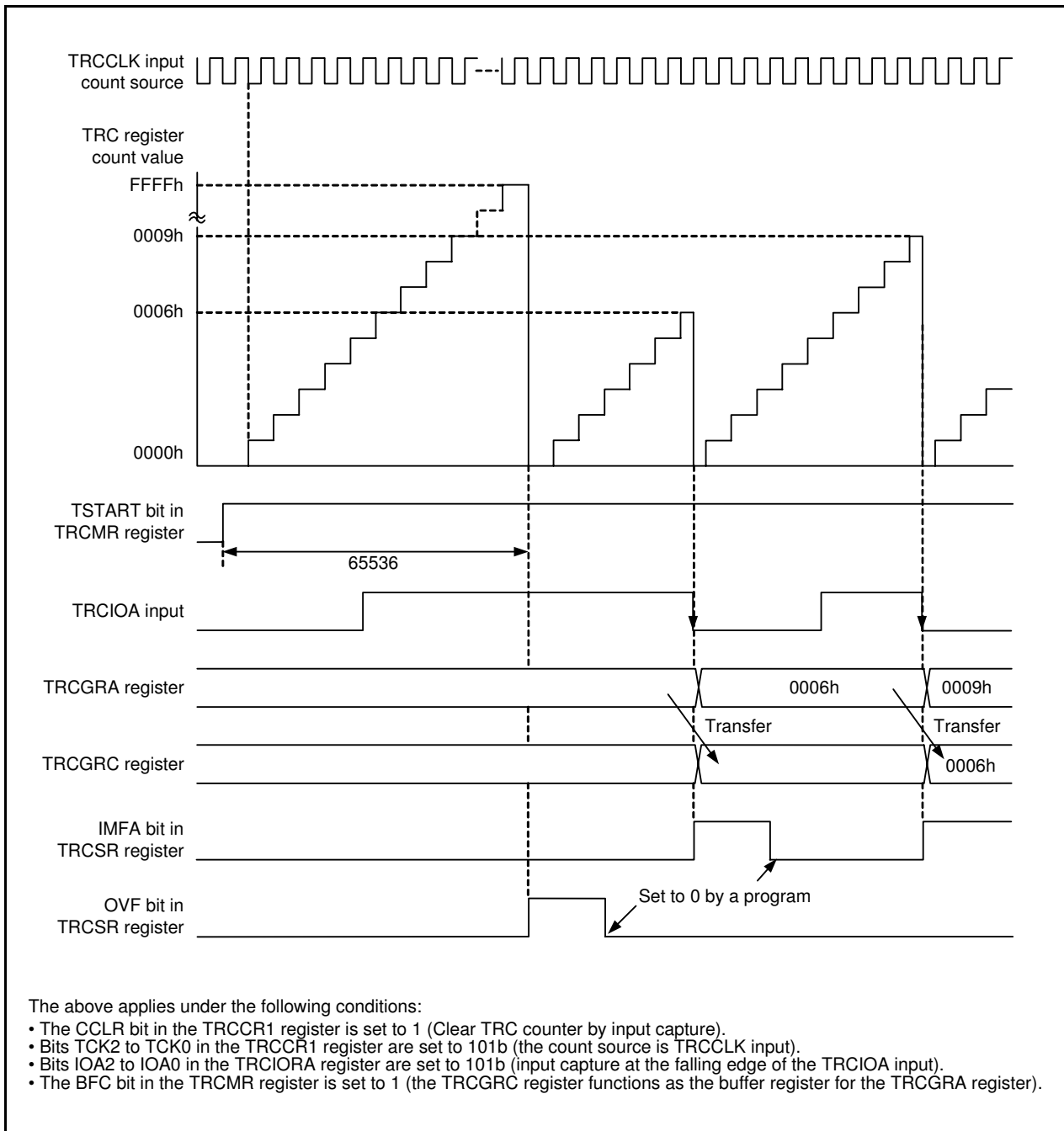
**Table 18.8 Functions of TRCGRj Register when Using Input Capture Function**

| Register | Setting | Register Function  | Input Capture Input Pin |
|----------|---------|--|-------------------------|
| TRCGRA   | –       | General register. Can be used to read the TRC register value at input capture.   | TRCIOA                  |
| TRCGRB   |         |  | TRCIOB                  |
| TRCGRC   | BFC = 0 | General register. Can be used to read the TRC register value at input capture.   | TRCIOC                  |
| TRCGRD   | BFD = 0 |  | TRCIOD                  |
| TRCGRC   | BFC = 1 | Buffer registers. Can be used to hold transferred value from the general register. (Refer to <b>18.3.2 Buffer Operation.</b> ) | TRCIOA                  |
| TRCGRD   | BFD = 1 |  | TRCIOB                  |

j = A, B, C, or D

BFC, BFD: Bits in TRCMR register

### 18.4.3 Operating Example



**Figure 18.8 Operating Example of Input Capture Function**

## 18.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.

Table 18.9 lists the Specifications of Output Compare Function, Figure 18.9 shows a Block Diagram of Output Compare Function, Table 18.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 18.10 shows an Operating Example of Output Compare Function.

**Table 18.9 Specifications of Output Compare Function**

| Item   | Specification  |
|--|--|
| Count source                                     | f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin   |
| Count operation                                  | Increment  |
| Count period                                     | <ul style="list-style-type: none"> <li>The CCLR bit in the TRCCR1 register is set to 0 (free running operation):<br/> <math>1/fk \times 65,536</math><br/> fk: Count source frequency</li> <li>The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match):<br/> <math>1/fk \times (n + 1)</math><br/> n: TRCGRA register setting value</li> </ul>   |
| Waveform output timing                           | Compare match  |
| Count start condition                            | 1 (count starts) is written to the TSTART bit in the TRCMR register.   |
| Count stop condition                             | <ul style="list-style-type: none"> <li>When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA).<br/> 0 (count stops) is written to the TSTART bit in the TRCMR register.<br/> The output compare output pin retains output level before count stops, the TRC register retains a value before count stops.</li> <li>When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register).<br/> The count stops at the compare match with the TRCGRA register. The output compare output pin retains the level after the output is changed by the compare match.</li> </ul>   |
| Interrupt request generation timing              | <ul style="list-style-type: none"> <li>Compare match (contents of registers TRC and TRCGRj match)</li> <li>The TRC register overflows.</li> </ul>  |
| TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions | Programmable I/O port or output compare output (Selectable individually for each pin)  |
| INT0 pin function                                | Programmable I/O port, pulse output forced cutoff signal input, or INT0 interrupt input  |
| Read from timer                                  | The count value can be read by reading the TRC register.   |
| Write to timer                                   | The TRC register can be written to.  |
| Select functions                                 | <ul style="list-style-type: none"> <li>Output compare output pin selection<br/> One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD</li> <li>Compare match output level selection<br/> "L" output, "H" output, or toggle output</li> <li>Initial output level selection<br/> Sets output level for period from count start to compare match</li> <li>Timing for setting the TRC register to 0000h<br/> Overflow or compare match with the TRCGRA register</li> <li>Buffer operation (Refer to <b>18.3.2 Buffer Operation</b>.)</li> <li>Pulse output forced cutoff signal input (Refer to <b>18.3.4 Forced Cutoff of Pulse Output</b>.)</li> <li>Can be used as an internal timer by disabling timer RC output</li> <li>Changing output pins for registers TRCGRC and TRCGRD<br/> TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin.</li> <li>A/D trigger generation</li> </ul> |

j = A, B, C, or D

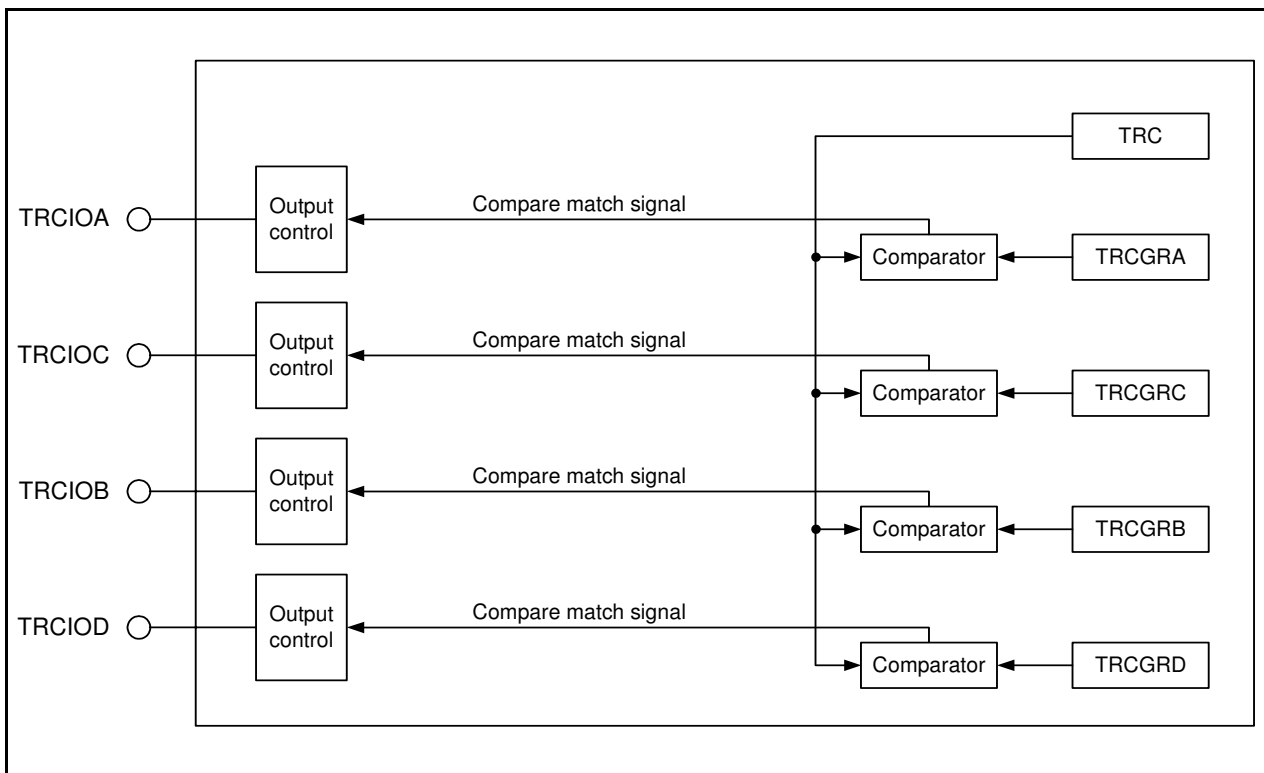


Figure 18.9 Block Diagram of Output Compare Function

### 18.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function

Address 0121h

| Bit         | b7   | b6   | b5   | b4   | b3  | b2  | b1  | b0  |
|-------------|------|------|------|------|-----|-----|-----|-----|
| Symbol      | CCLR | TCK2 | TCK1 | TCK0 | TOD | TOC | TOB | TOA |
| After Reset | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name                              | Function   | R/W |
|-----|--------|---------------------------------------|--|-----|
| b0  | TOA    | TRCIOA output level select bit (1, 2) | 0: Initial output "L"<br>1: Initial output "H"   | R/W |
| b1  | TOB    | TRCIOB output level select bit (1, 2) |  | R/W |
| b2  | TOC    | TRCIOC output level select bit (1, 2) |  | R/W |
| b3  | TOD    | TRCIOD output level select bit (1, 2) |  | R/W |
| b4  | TCK0   | Count source select bit (1)           | b6 b5 b4<br>0 0 0: f1<br>0 0 1: f2<br>0 1 0: f4<br>0 1 1: f8<br>1 0 0: f32<br>1 0 1: TRCCLK input rising edge<br>1 1 0: fOCO40M<br>1 1 1: fOCO-F (3) | R/W |
| b5  | TCK1   |                                       |  | R/W |
| b6  | TCK2   |                                       |  | R/W |
| b7  | CCLR   | TRC counter clear select bit          | 0: Disable clear (free-running operation)<br>1: Clear by compare match in the TRCGRA register  | R/W |

Notes:

1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

**Table 18.10 Functions of TRCGRj Register when Using Output Compare Function**

| Register | Setting | Register Function  | Output Compare Output Pin |
|----------|---------|--|---------------------------|
| TRCGRA   | -       | General register. Write a compare value to one of these registers.   | TRCIOA                    |
| TRCGRB   |         |  | TRCIOB                    |
| TRCGRC   | BFC = 0 | General register. Write a compare value to one of these registers.   | TRCIOC                    |
| TRCGRD   | BFD = 0 |  | TRCIOD                    |
| TRCGRC   | BFC = 1 | Buffer register. Write the next compare value to one of these registers. (Refer to <b>18.3.2 Buffer Operation</b> .) | TRCIOA                    |
| TRCGRD   | BFD = 1 |  | TRCIOB                    |

j = A, B, C, or D

BFC, BFD: Bits in TRCMR register

## 18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

|             |    |      |      |      |      |      |      |      |
|-------------|----|------|------|------|------|------|------|------|
| Bit         | b7 | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | —  | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 |
| After Reset | 1  | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | IOA0   | TRCGRA control bit  | <sup>b1 b0</sup><br>0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port)<br>0 1: "L" output by compare match in the TRCGRA register<br>1 0: "H" output by compare match in the TRCGRA register<br>1 1: Toggle output by compare match in the TRCGRA register | R/W |
| b1  | IOA1   |   |  | R/W |
| b2  | IOA2   | TRCGRA mode select bit <sup>(1)</sup>                                     | Set to 0 (output compare) in the output compare function.  | R/W |
| b3  | IOA3   | TRCGRA input capture input switch bit                                     | Set to 1.  | R/W |
| b4  | IOB0   | TRCGRB control bit  | <sup>b5 b4</sup><br>0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port)<br>0 1: "L" output by compare match in the TRCGRB register<br>1 0: "H" output by compare match in the TRCGRB register<br>1 1: Toggle output by compare match in the TRCGRB register | R/W |
| b5  | IOB1   |   |  | R/W |
| b6  | IOB2   | TRCGRB mode select bit <sup>(2)</sup>                                     | Set to 0 (output compare) in the output compare function.  | R/W |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |  | —   |

## Notes:

- When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

### 18.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function

Address 0125h

|             |      |      |      |      |      |      |      |      |
|-------------|------|------|------|------|------|------|------|------|
| Bit         | b7   | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 |
| After Reset | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                              | Function  | R/W |
|-----|--------|---------------------------------------|---|-----|
| b0  | IOC0   | TRCGRC control bit                    | b1 b0<br>0 0: Disable pin output by compare match<br>0 1: "L" output by compare match in the TRCGRC register<br>1 0: "H" output by compare match in the TRCGRC register<br>1 1: Toggle output by compare match in the TRCGRC register | R/W |
| b1  | IOC1   |                                       |   | R/W |
| b2  | IOC2   | TRCGRC mode select bit <sup>(1)</sup> | Set to 0 (output compare) in the output compare function.   | R/W |
| b3  | IOC3   | TRCGRC register function select bit   | 0: TRCIOA output register<br>1: General register or buffer register   | R/W |
| b4  | IOD0   | TRCGRD control bit                    | b5 b4<br>0 0: Disable pin output by compare match<br>0 1: "L" output by compare match in the TRCGRD register<br>1 0: "H" output by compare match in the TRCGRD register<br>1 1: Toggle output by compare match in the TRCGRD register | R/W |
| b5  | IOD1   |                                       |   | R/W |
| b6  | IOD2   | TRCGRD mode select bit <sup>(2)</sup> | Set to 0 (output compare) in the output compare function.   | R/W |
| b7  | IOD3   | TRCGRD register function select bit   | 0: TRCIOB output register<br>1: General register or buffer register   | R/W |

## Notes:

- When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.



### 18.5.4 Timer RC Control Register 2 (TRCCR2) for Output Compare Function

Address 0130h

|             |       |       |      |    |    |      |      |      |
|-------------|-------|-------|------|----|----|------|------|------|
| Bit         | b7    | b6    | b5   | b4 | b3 | b2   | b1   | b0   |
| Symbol      | TCEG1 | TCEG0 | CSEL | —  | —  | POLD | POLC | POLB |
| After Reset | 0     | 0     | 0    | 1  | 1  | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | POLB   | PWM mode output level control bit B <sup>(1)</sup>                        | 0: TRCIOB output level selected as “L” active<br>1: TRCIOB output level selected as “H” active  | R/W |
| b1  | POLC   | PWM mode output level control bit C <sup>(1)</sup>                        | 0: TRCIOC output level selected as “L” active<br>1: TRCIOC output level selected as “H” active  | R/W |
| b2  | POLD   | PWM mode output level control bit D <sup>(1)</sup>                        | 0: TRCIOD output level selected as “L” active<br>1: TRCIOD output level selected as “H” active  | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b4  | —      |   |   |     |
| b5  | CSEL   | TRC count operation select bit <sup>(2)</sup>                             | 0: Count continues at compare match with the TRCGRA register<br>1: Count stops at compare match with the TRCGRA register                                      | R/W |
| b6  | TCEG0  | TRCTRG input edge select bit <sup>(3)</sup>                               | <sup>b7 b6</sup><br>0 0: Disable the trigger input from the TRCTRG pin<br>0 1: Rising edge selected<br>1 0: Falling edge selected<br>1 1: Both edges selected | R/W |
| b7  | TCEG1  |   |   | R/W |

Notes:

1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

### 18.5.5 Operating Example

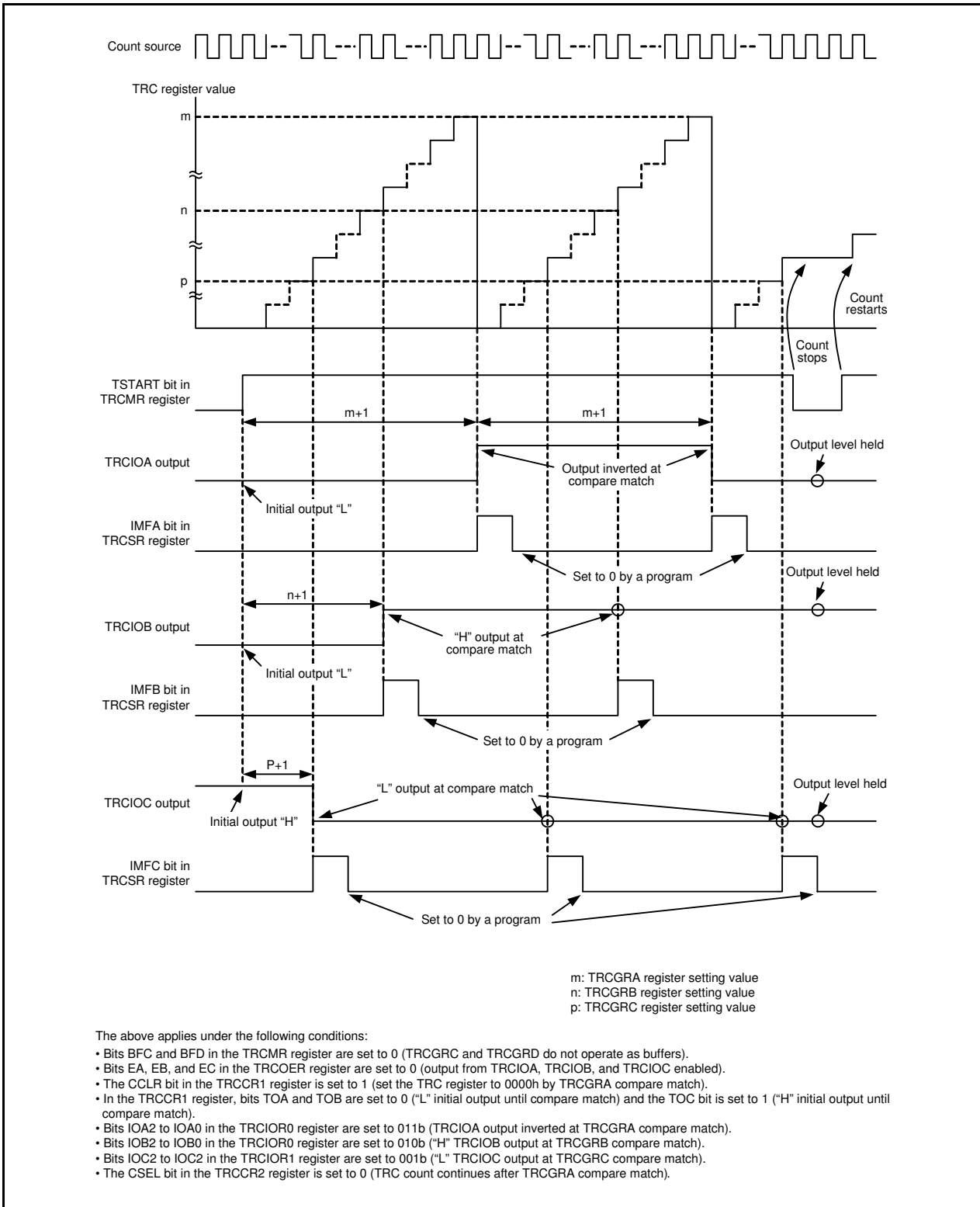


Figure 18.10 Operating Example of Output Compare Function

### 18.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 18.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.

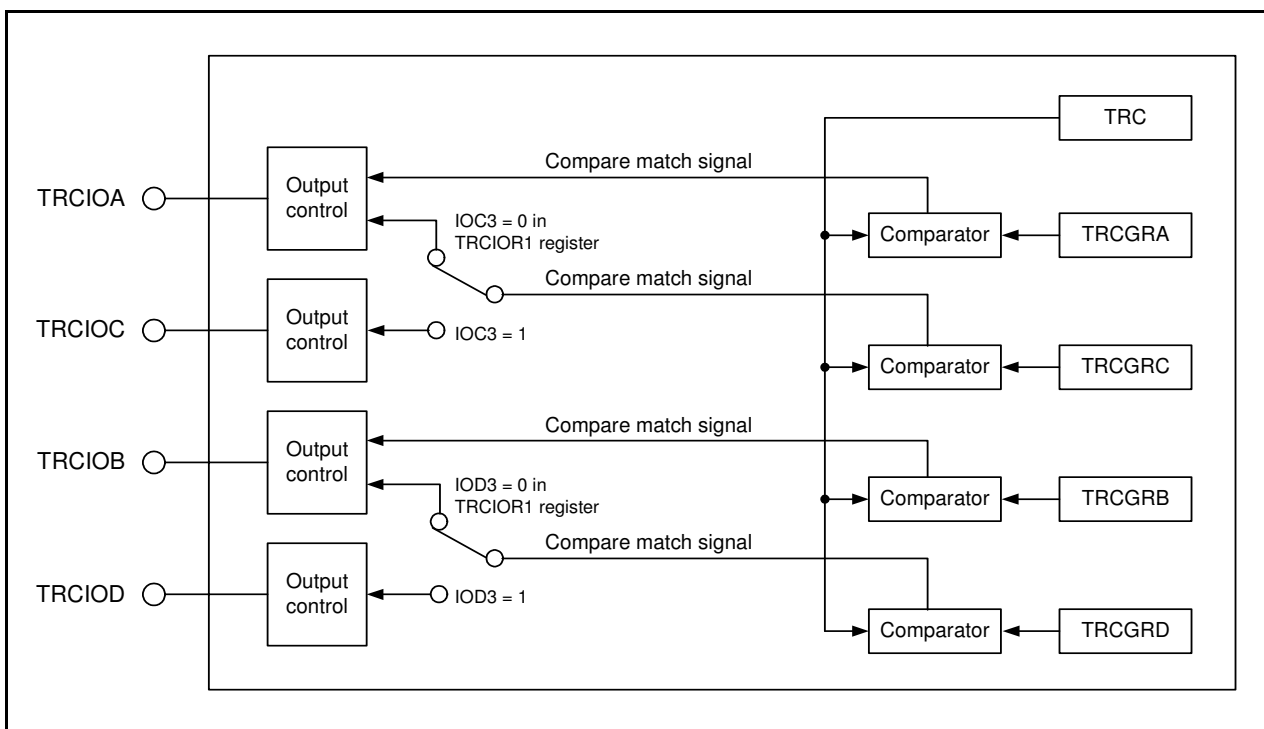
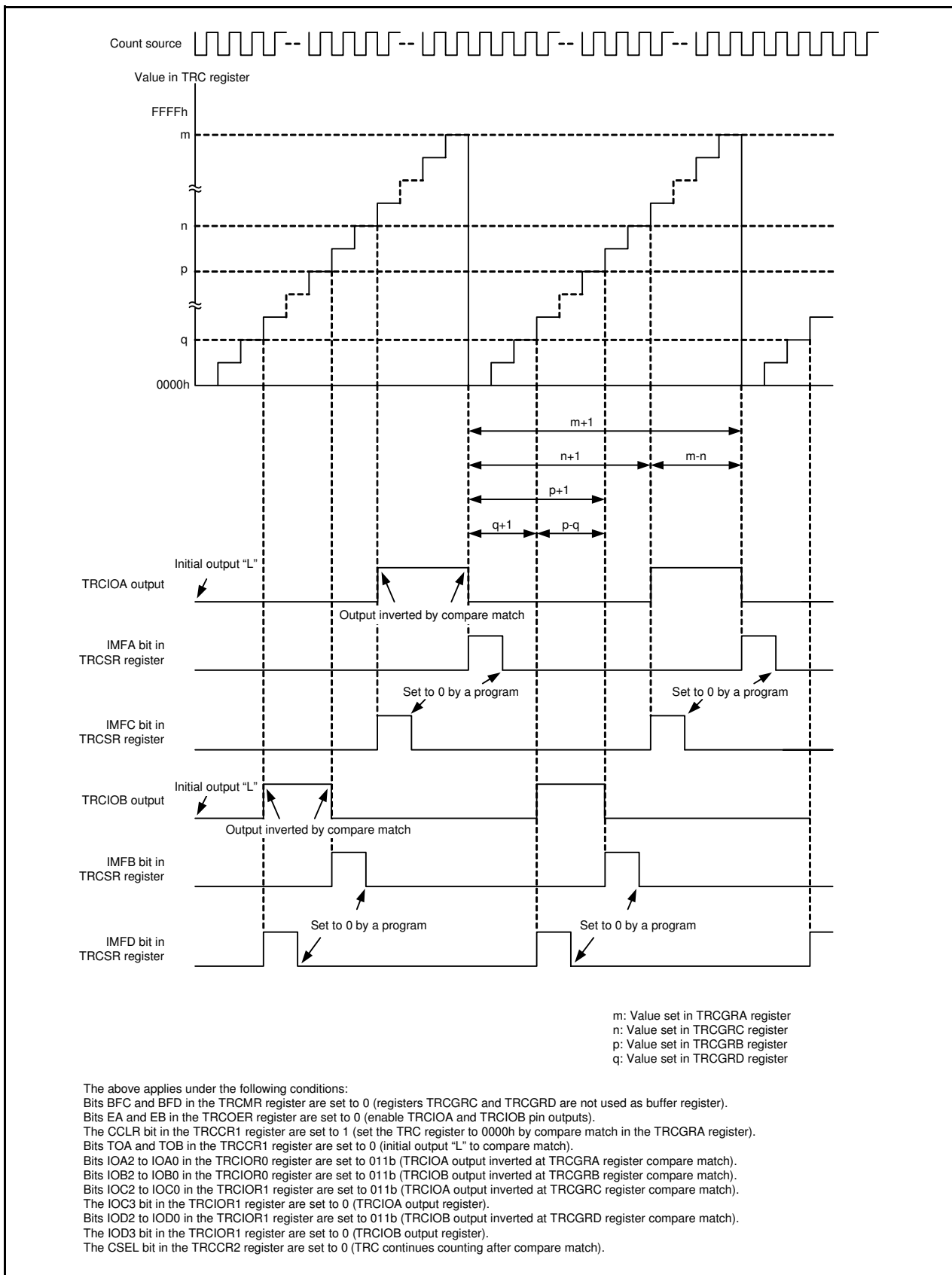


Figure 18.11 Changing Output Pins in Registers TRCGRC and TRCGRD

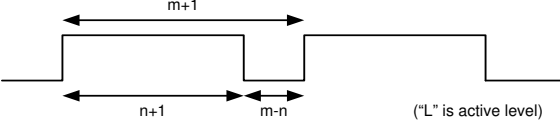


**Figure 18.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin**

## 18.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.) Table 18.11 lists the Specifications of PWM Mode, Figure 18.13 shows a PWM Mode Block Diagram, Table 18.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 18.14 and 18.15 show Operating Examples of PWM Mode.

**Table 18.11 Specifications of PWM Mode**

| Item                                     | Specification   |
|--|---|
| Count source                             | f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin  |
| Count operation                          | Increment   |
| PWM waveform                             | PWM period: $1/f_k \times (m + 1)$<br>Active level width: $1/f_k \times (m - n)$<br>Inactive width: $1/f_k \times (n + 1)$<br>$f_k$ : Count source frequency<br>$m$ : TRCGRA register setting value<br>$n$ : TRCGRj register setting value<br>   |
| Count start condition                    | 1 (count starts) is written to the TSTART bit in the TRCMR register.  |
| Count stop condition                     | <ul style="list-style-type: none"> <li>When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops.</li> <li>When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.</li> </ul> |
| Interrupt request generation timing      | <ul style="list-style-type: none"> <li>Compare match (contents of registers TRC and TRCGRh match)</li> <li>The TRC register overflows.</li> </ul>   |
| TRCIOA pin function                      | Programmable I/O port   |
| TRCIOB, TRCIOC, and TRCIOD pin functions | Programmable I/O port or PWM output (selectable individually for each pin)  |
| INT0 pin function                        | Programmable I/O port, pulse output forced cutoff signal input, or INT0 interrupt input   |
| Read from timer                          | The count value can be read by reading the TRC register.  |
| Write to timer                           | The TRC register can be written to.   |
| Select functions                         | <ul style="list-style-type: none"> <li>One to three pins selectable as PWM output pins<br/>One or more of pins TRCIOB, TRCIOC, and TRCIOD</li> <li>Active level selectable for each pin</li> <li>Initial level selectable for each pin</li> <li>Buffer operation (Refer to <b>18.3.2 Buffer Operation.</b>)</li> <li>Pulse output forced cutoff signal input (Refer to <b>18.3.4 Forced Cutoff of Pulse Output.</b>)</li> <li>A/D trigger generation</li> </ul>   |

j = B, C, or D

h = A, B, C, or D

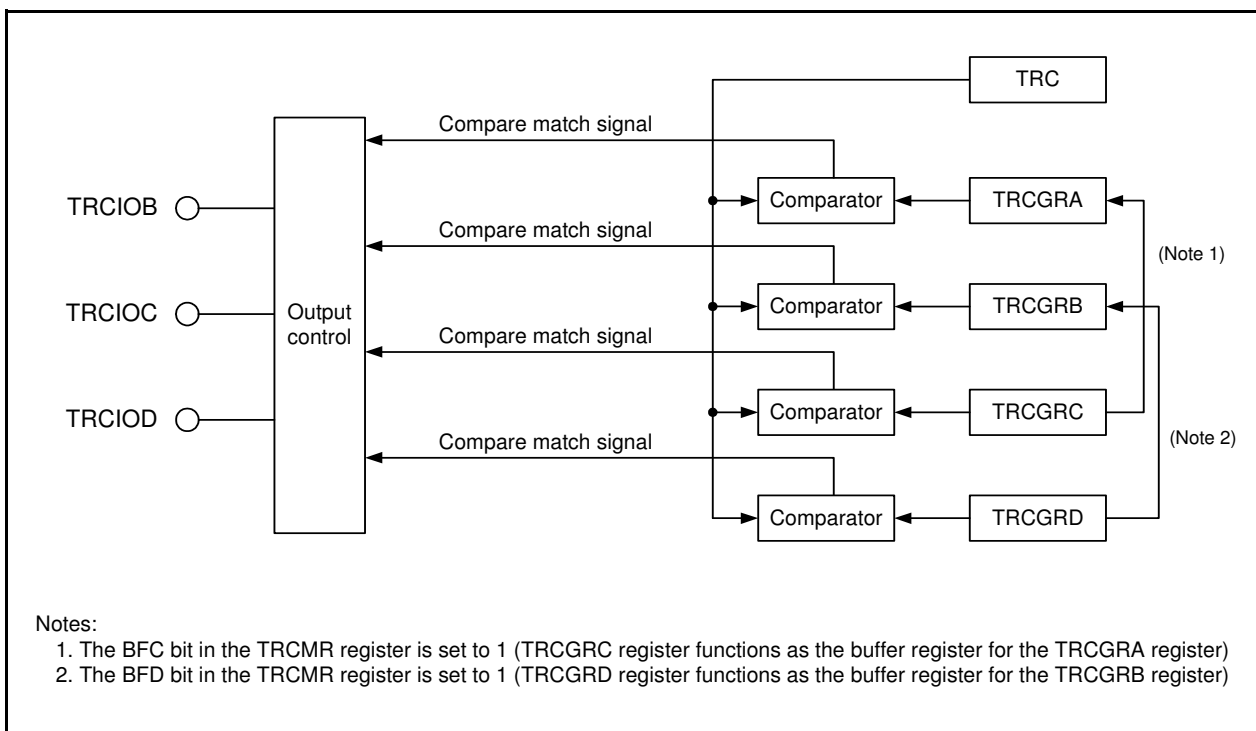


Figure 18.13 PWM Mode Block Diagram

### 18.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

|             |      |      |      |      |     |     |     |     |
|-------------|------|------|------|------|-----|-----|-----|-----|
| Bit         | b7   | b6   | b5   | b4   | b3  | b2  | b1  | b0  |
| Symbol      | CCLR | TCK2 | TCK1 | TCK0 | TOD | TOC | TOB | TOA |
| After Reset | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name                              | Function   | R/W |
|-----|--------|---------------------------------------|--|-----|
| b0  | TOA    | TRCIOA output level select bit (1)    | Disabled in PWM mode   | R/W |
| b1  | TOB    | TRCIOB output level select bit (1, 2) | 0: Initial output selected as non-active level<br>1: Initial output selected as active level   | R/W |
| b2  | TOC    | TRCIOC output level select bit (1, 2) |  | R/W |
| b3  | TOD    | TRCIOD output level select bit (1, 2) |  | R/W |
| b4  | TCK0   | Count source select bit (1)           | b6 b5 b4<br>0 0 0: f1<br>0 0 1: f2<br>0 1 0: f4<br>0 1 1: f8<br>1 0 0: f32<br>1 0 1: TRCCLK input rising edge<br>1 1 0: fOCO40M<br>1 1 1: fOCO-F (3) | R/W |
| b5  | TCK1   |                                       |  | R/W |
| b6  | TCK2   |                                       |  | R/W |
| b7  | CCLR   | TRC counter clear select bit          | 0: Disable clear (free-running operation)<br>1: Clear by compare match in the TRCGRA register  | R/W |

Notes:

1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

## 18.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

|             |       |       |      |    |    |      |      |      |
|-------------|-------|-------|------|----|----|------|------|------|
| Bit         | b7    | b6    | b5   | b4 | b3 | b2   | b1   | b0   |
| Symbol      | TCEG1 | TCEG0 | CSEL | —  | —  | POLD | POLC | POLB |
| After Reset | 0     | 0     | 0    | 1  | 1  | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | POLB   | PWM mode output level control bit B <sup>(1)</sup>                        | 0: TRCIOB output level selected as “L” active<br>1: TRCIOB output level selected as “H” active  | R/W |
| b1  | POLC   | PWM mode output level control bit C <sup>(1)</sup>                        | 0: TRCIOC output level selected as “L” active<br>1: TRCIOC output level selected as “H” active  | R/W |
| b2  | POLD   | PWM mode output level control bit D <sup>(1)</sup>                        | 0: TRCIOD output level selected as “L” active<br>1: TRCIOD output level selected as “H” active  | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b4  | —      |   |   |     |
| b5  | CSEL   | TRC count operation select bit <sup>(2)</sup>                             | 0: Count continues at compare match with the TRCGRA register<br>1: Count stops at compare match with the TRCGRA register                            | R/W |
| b6  | TCEG0  | TRCTRIG input edge select bit <sup>(3)</sup>                              | b7 b6<br>0 0: Disable the trigger input from the TRCTRIG pin<br>0 1: Rising edge selected<br>1 0: Falling edge selected<br>1 1: Both edges selected | R/W |
| b7  | TCEG1  |   |   | R/W |

Notes:

1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

**Table 18.12 Functions of TRCGRh Register in PWM Mode**

| Register | Setting | Register Function  | PWM Output Pin |
|----------|---------|--|----------------|
| TRCGRA   | —       | General register. Set the PWM period.  | —              |
| TRCGRB   | —       | General register. Set the PWM output change point.   | TRCIOB         |
| TRCGRC   | BFC = 0 | General register. Set the PWM output change point.   | TRCIOC         |
| TRCGRD   | BFD = 0 |  | TRCIOD         |
| TRCGRC   | BFC = 1 | Buffer register. Set the next PWM period. (Refer to <b>18.3.2 Buffer Operation</b> .)              | —              |
| TRCGRD   | BFD = 1 | Buffer register. Set the next PWM output change point. (Refer to <b>18.3.2 Buffer Operation</b> .) | TRCIOB         |

h = A, B, C, or D

BFC, BFD: Bits in TRCMR register

Note:

1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.



### 18.6.3 Operating Example

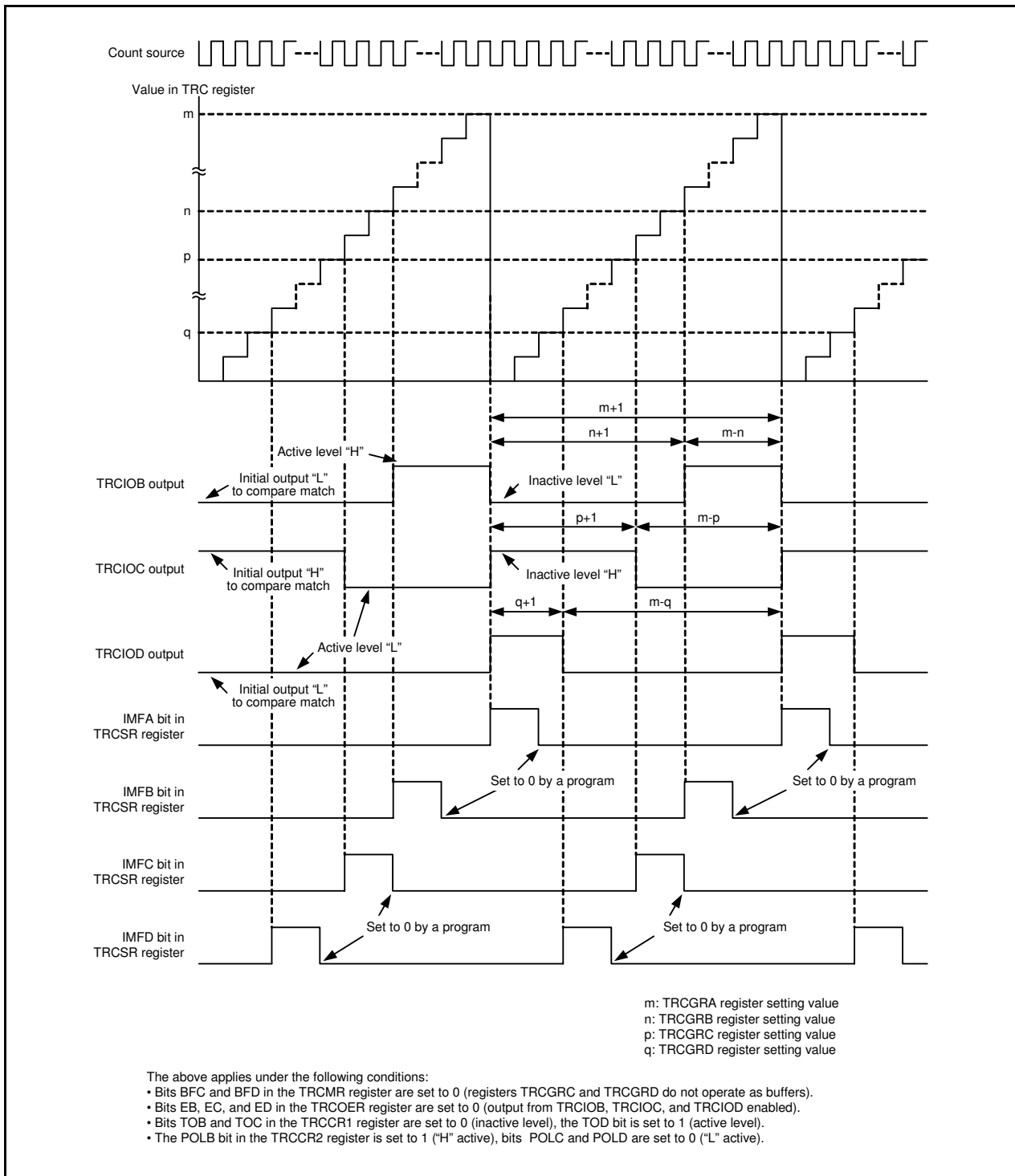


Figure 18.14 Operating Example of PWM Mode

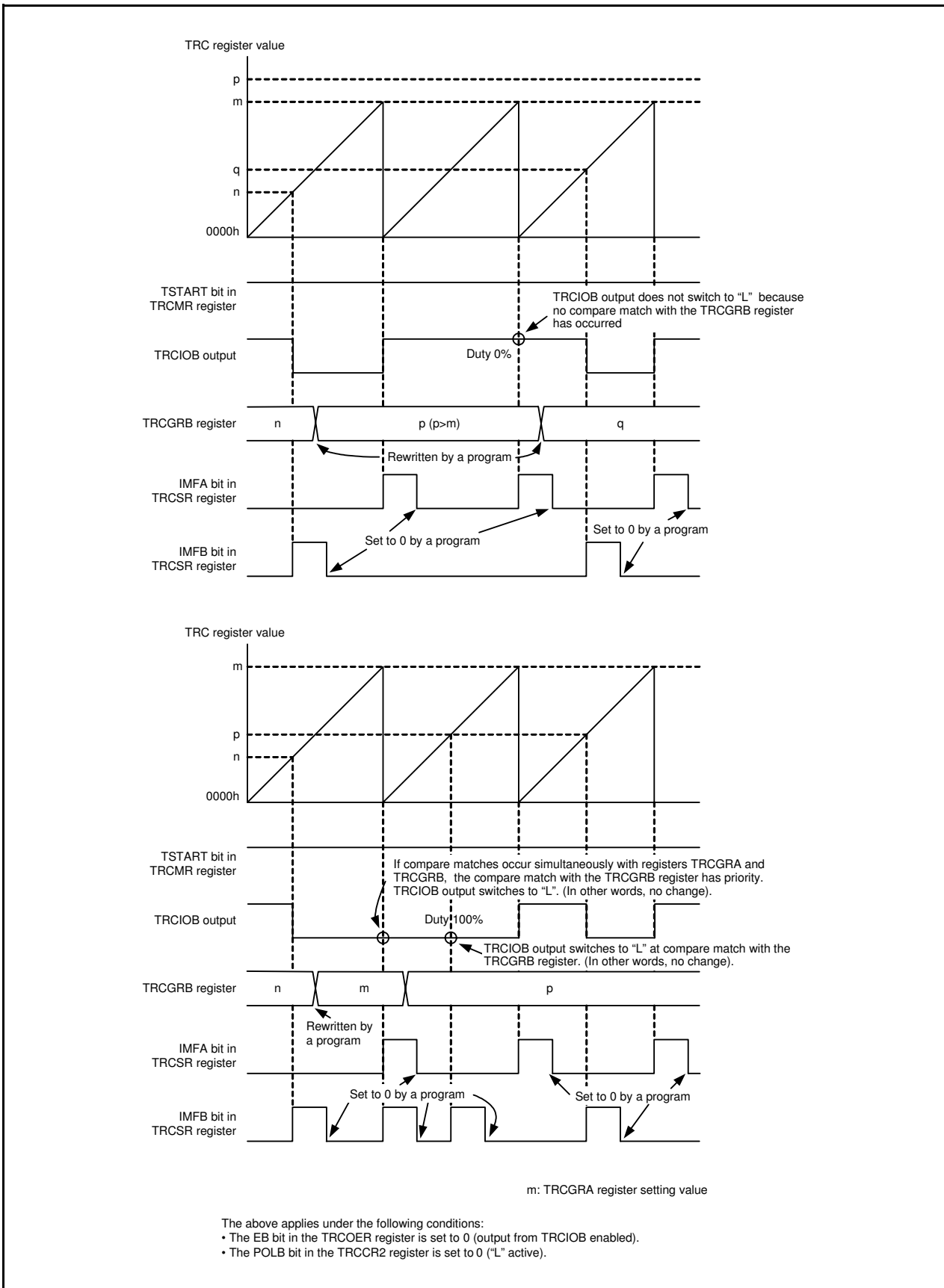
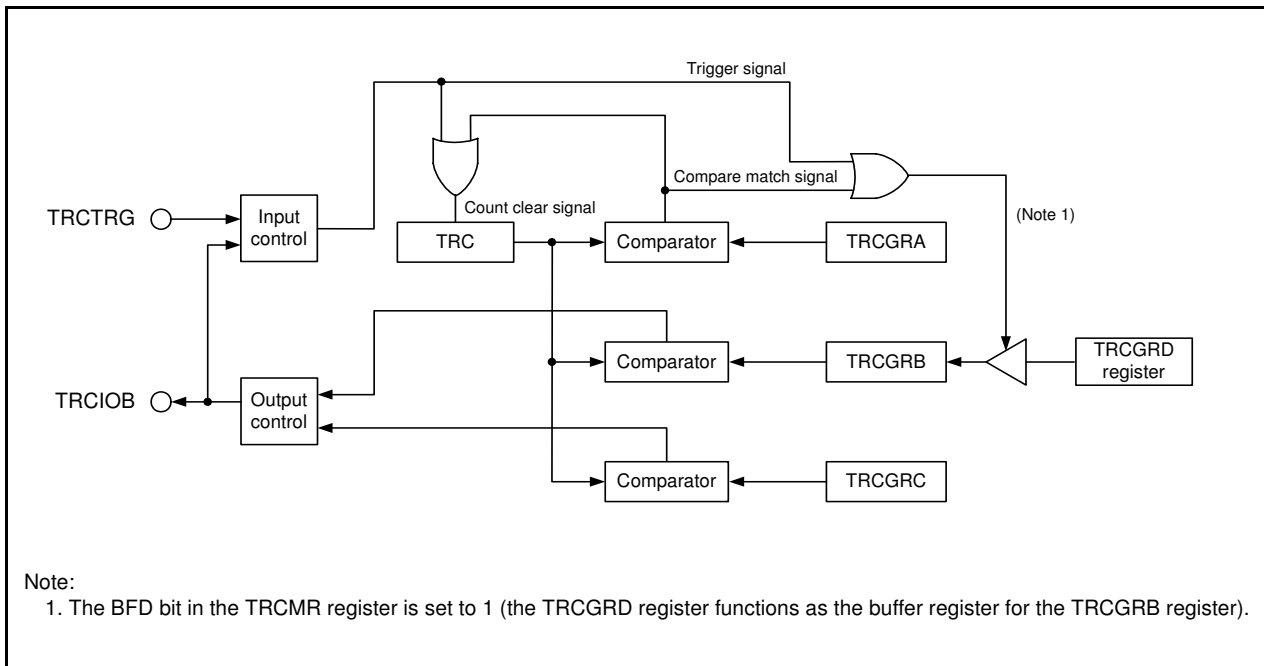


Figure 18.15 Operating Example of PWM Mode (Duty 0% and Duty 100%)

## 18.7 PWM2 Mode

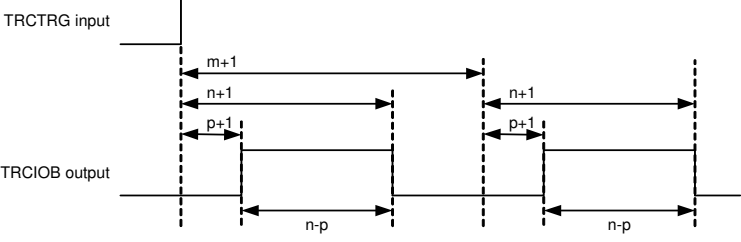
This mode outputs a single PWM waveform. After a given wait duration has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.

Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 18.16 shows a PWM2 Mode Block Diagram, Table 18.13 lists the Specifications of PWM2 Mode, Table 18.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 18.17 to 18.19 show Operating Examples of PWM2 Mode.



**Figure 18.16 PWM2 Mode Block Diagram**

**Table 18.13 Specifications of PWM2 Mode**

| Item                                | Specification  |
|-------------------------------------|--|
| Count source                        | f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin   |
| Count operation                     | Increase TRC register  |
| PWM waveform                        | <p>PWM period: <math>1/fk \times (m + 1)</math> (no TRCTRIG input)<br/> Active level width: <math>1/fk \times (n - p)</math><br/> Wait time from count start or trigger: <math>1/fk \times (p + 1)</math><br/> fk: Count source frequency<br/> m: TRCGRA register setting value<br/> n: TRCGRB register setting value<br/> p: TRCGRC register setting value</p>  <p>(TRCTRIG: Rising edge, active level is "H")</p>  |
| Count start conditions              | <ul style="list-style-type: none"> <li>• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRIG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register.</li> <li>• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRIG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRIG pin</li> </ul>   |
| Count stop conditions               | <ul style="list-style-type: none"> <li>• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before count stops.</li> <li>• The count stops due to a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1. The TRCIOB pin outputs the initial level. The TRC register retains the value before count stops if the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h if the CCLR bit in the TRCCR1 register is set to 1.</li> </ul> |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• Compare match (contents of TRC and TRCGRj registers match)</li> <li>• The TRC register overflows</li> </ul>   |
| TRCIOA/TRCTRIG pin function         | Programmable I/O port or TRCTRIG input   |
| TRCIOB pin function                 | PWM output   |
| TRCIOC and TRCIOD pin functions     | Programmable I/O port  |
| INT0 pin function                   | Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input  |
| Read from timer                     | The count value can be read by reading the TRC register.   |
| Write to timer                      | The TRC register can be written to.  |
| Select functions                    | <ul style="list-style-type: none"> <li>• External trigger and valid edge selection<br/>The edge or edges of the signal input to the TRCTRIG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges</li> <li>• Buffer operation (Refer to <b>18.3.2 Buffer Operation.</b>)</li> <li>• Pulse output forced cutoff signal input (Refer to <b>18.3.4 Forced Cutoff of Pulse Output.</b>)</li> <li>• Digital filter (Refer to <b>18.3.3 Digital Filter.</b>)</li> <li>• A/D trigger generation</li> </ul>   |

j = A, B, or C

### 18.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

| Bit         | b7   | b6   | b5   | b4   | b3  | b2  | b1  | b0  |
|-------------|------|------|------|------|-----|-----|-----|-----|
| Symbol      | CCLR | TCK2 | TCK1 | TCK0 | TOD | TOC | TOB | TOA |
| After Reset | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name                              | Function   | R/W |
|-----|--------|---------------------------------------|--|-----|
| b0  | TOA    | TRCIOA output level select bit (1)    | Disabled in PWM2 mode  | R/W |
| b1  | TOB    | TRCIOB output level select bit (1, 2) | 0: Active level "H"<br>(Initial output "L"<br>"H" output by compare match in the TRCGRC register<br>"L" output by compare match in the TRCGRB register)<br>1: Active level "L"<br>(Initial output "H"<br>"L" output by compare match in the TRCGRC register<br>"H" output by compare match in the TRCGRB register) | R/W |
| b2  | TOC    | TRCIOC output level select bit (1)    | Disabled in PWM2 mode  | R/W |
| b3  | TOD    | TRCIOD output level select bit (1)    |  | R/W |
| b4  | TCK0   | Count source select bit (1)           | b6 b5 b4<br>0 0 0: f1<br>0 0 1: f2<br>0 1 0: f4<br>0 1 1: f8<br>1 0 0: f32<br>1 0 1: TRCLK input rising edge<br>1 1 0: fOCO40M<br>1 1 1: fOCO-F (3)  | R/W |
| b5  | TCK1   |                                       |  | R/W |
| b6  | TCK2   |                                       |  | R/W |
| b7  | CCLR   | TRC counter clear select bit          | 0: Disable clear (free-running operation)<br>1: Clear by compare match in the TRCGRA register  | R/W |

## Notes:

1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

### 18.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

|             |       |       |      |    |    |      |      |      |
|-------------|-------|-------|------|----|----|------|------|------|
| Bit         | b7    | b6    | b5   | b4 | b3 | b2   | b1   | b0   |
| Symbol      | TCEG1 | TCEG0 | CSEL | —  | —  | POLD | POLC | POLB |
| After Reset | 0     | 0     | 0    | 1  | 1  | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | POLB   | PWM mode output level control bit B <sup>(1)</sup>                        | 0: TRCIOD output level selected as “L” active<br>1: TRCIOD output level selected as “H” active  | R/W |
| b1  | POLC   | PWM mode output level control bit C <sup>(1)</sup>                        | 0: TRCIOB output level selected as “L” active<br>1: TRCIOB output level selected as “H” active  | R/W |
| b2  | POLD   | PWM mode output level control bit D <sup>(1)</sup>                        | 0: TRCIOC output level selected as “L” active<br>1: TRCIOC output level selected as “H” active  | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 1. |   | —   |
| b4  | —      |   |   |     |
| b5  | CSEL   | TRC count operation select bit <sup>(2)</sup>                             | 0: Count continues at compare match with the TRCGRA register<br>1: Count stops at compare match with the TRCGRA register                                      | R/W |
| b6  | TCEG0  | TRCTRG input edge select bit <sup>(3)</sup>                               | <sup>b7 b6</sup><br>0 0: Disable the trigger input from the TRCTRG pin<br>0 1: Rising edge selected<br>1 0: Falling edge selected<br>1 1: Both edges selected | R/W |
| b7  | TCEG1  |   |   | R/W |

Notes:

1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **18.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

### 18.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

| Bit         | b7    | b6    | b5 | b4    | b3  | b2  | b1  | b0  |
|-------------|-------|-------|----|-------|-----|-----|-----|-----|
| Symbol      | DFCK1 | DFCK0 | —  | DFTRG | DFD | DFC | DFB | DFA |
| After Reset | 0     | 0     | 0  | 0     | 0   | 0   | 0   | 0   |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | DFA    | TRCIOA pin digital filter function select bit <sup>(1)</sup>              | 0: Function is not used<br>1: Function is used  | R/W |
| b1  | DFB    | TRCIOB pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b2  | DFC    | TRCIOC pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b3  | DFD    | TRCIOD pin digital filter function select bit <sup>(1)</sup>              |   | R/W |
| b4  | DFTRG  | TRCTRГ pin digital filter function select bit <sup>(2)</sup>              |   | R/W |
| b5  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. | —   | —   |
| b6  | DFCK0  | Clock select bits for digital filter function <sup>(1, 2)</sup>           | b7 b6<br>0 0: f32<br>0 1: f8<br>1 0: f1<br>1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register) | R/W |
| b7  | DFCK1  |   |   | R/W |

Notes:

- These bits are enabled for the input capture function.
- These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRГ trigger input enabled).

**Table 18.14 Functions of TRCGRj Register in PWM2 Mode**

| Register              | Setting | Register Function  | PWM2 Output Pin |
|-----------------------|---------|--|-----------------|
| TRCGRA                | —       | General register. Set the PWM period.  | TRCIOB pin      |
| TRCGRB <sup>(1)</sup> | —       | General register. Set the PWM output change point.   |                 |
| TRCGRC <sup>(1)</sup> | BFC = 0 | General register. Set the PWM output change point (wait time after trigger).                       |                 |
| TRCGRD                | BFD = 0 | (Not used in PWM2 mode)  | —               |
| TRCGRD                | BFD = 1 | Buffer register. Set the next PWM output change point. (Refer to <b>18.3.2 Buffer Operation</b> .) | TRCIOB pin      |

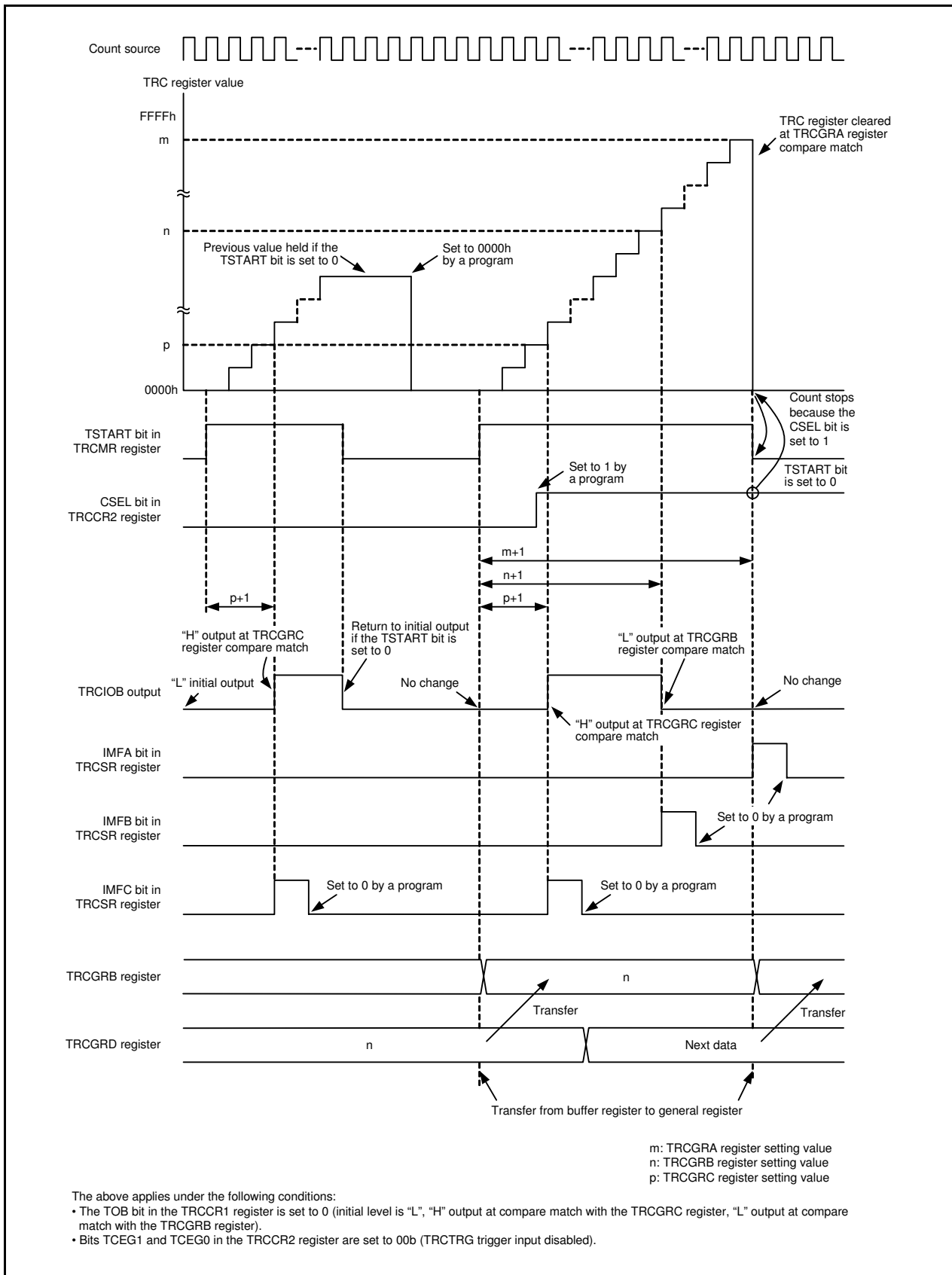
j = A, B, C, or D

BFC, BFD: Bits in TRCMR register

Note:

- Do not set the TRCGRB and TRCGRC registers to the same value.

### 18.7.4 Operating Example



**Figure 18.17 Operating Example of PWM2 Mode (TRCTRГ Trigger Input Disabled)**



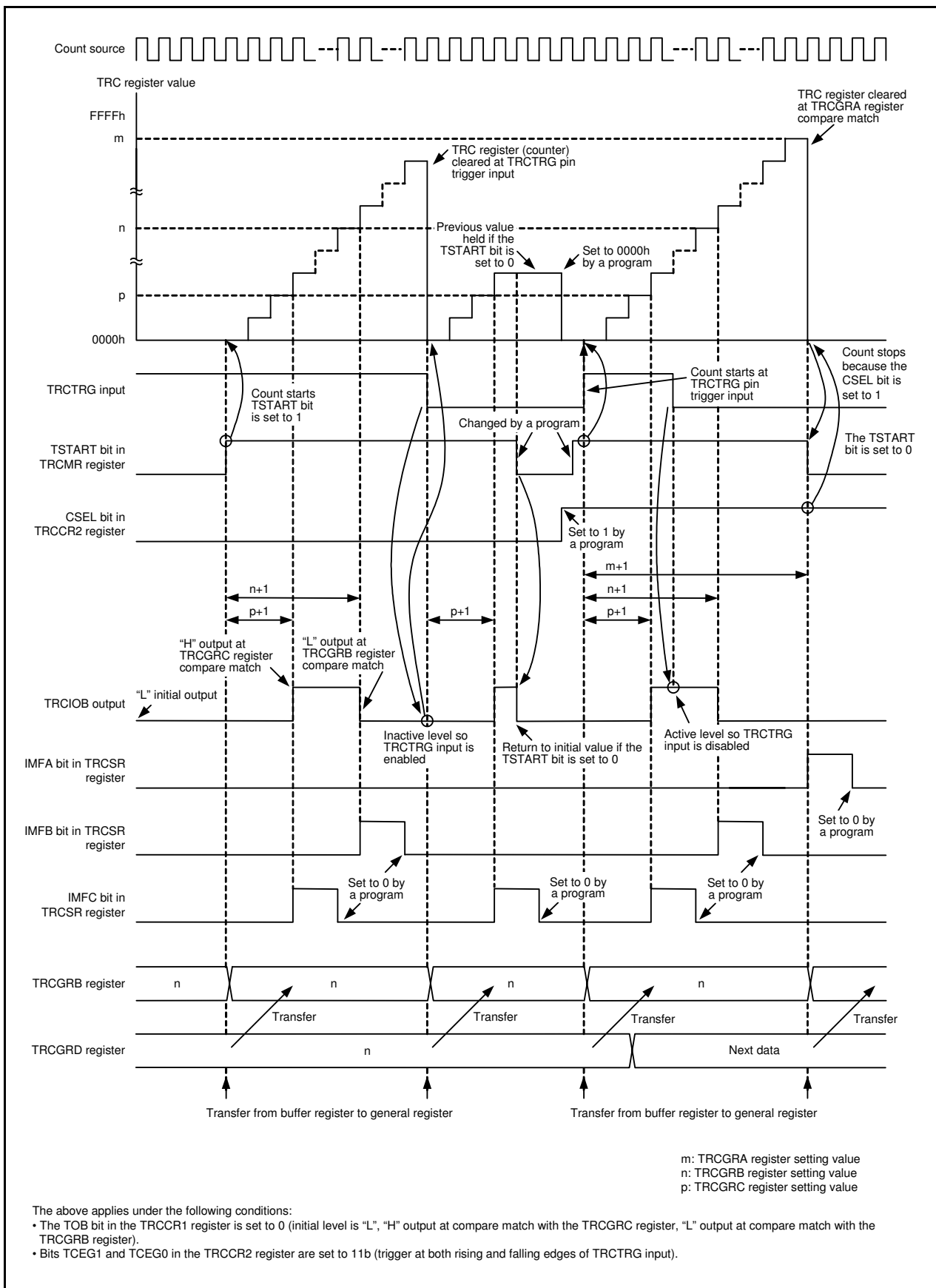
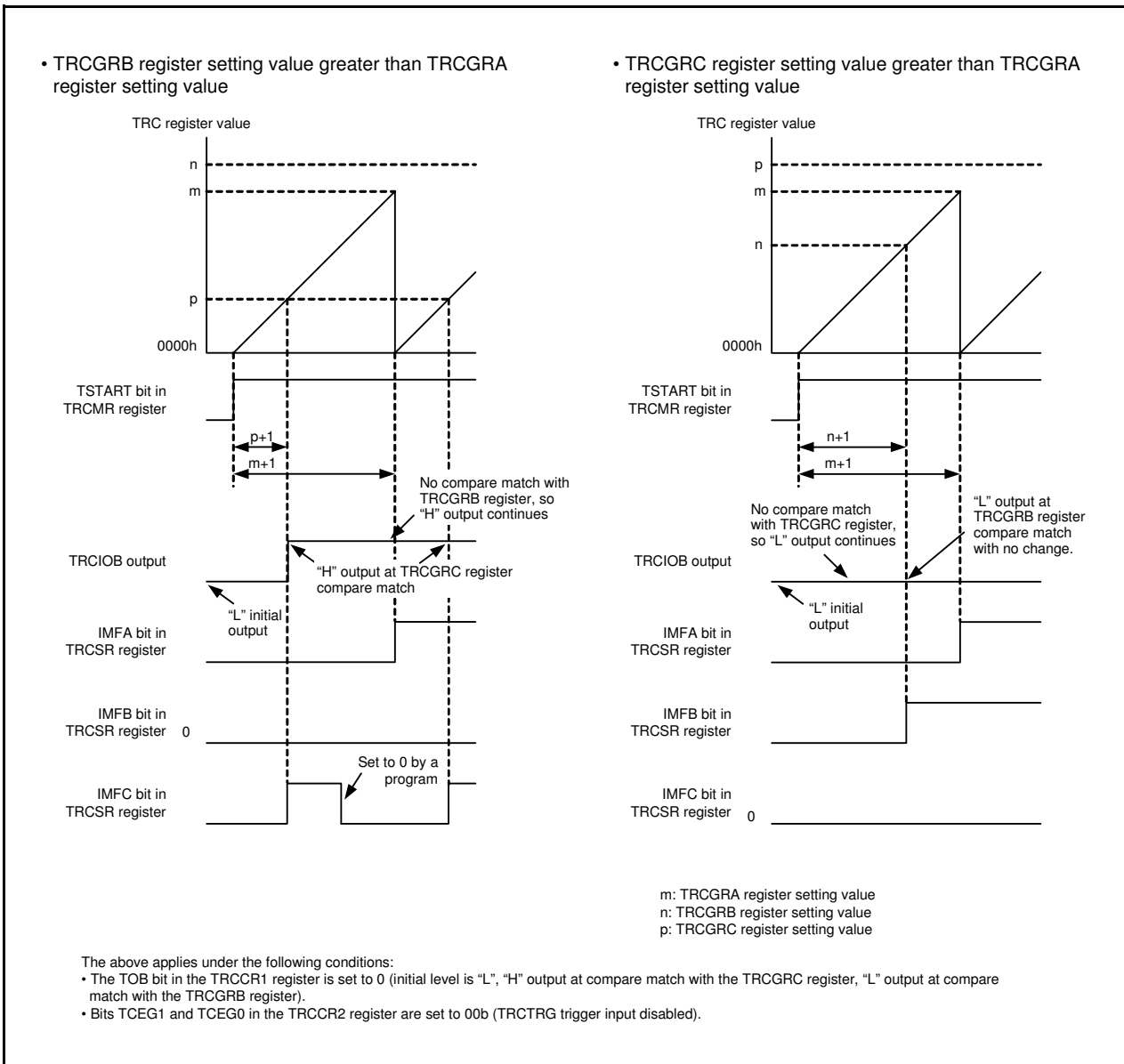


Figure 18.18 Operating Example of PWM2 Mode (TRCTRG Trigger Input Enabled)



**Figure 18.19 Operating Example of PWM2 Mode (Duty 0% and Duty 100%)**

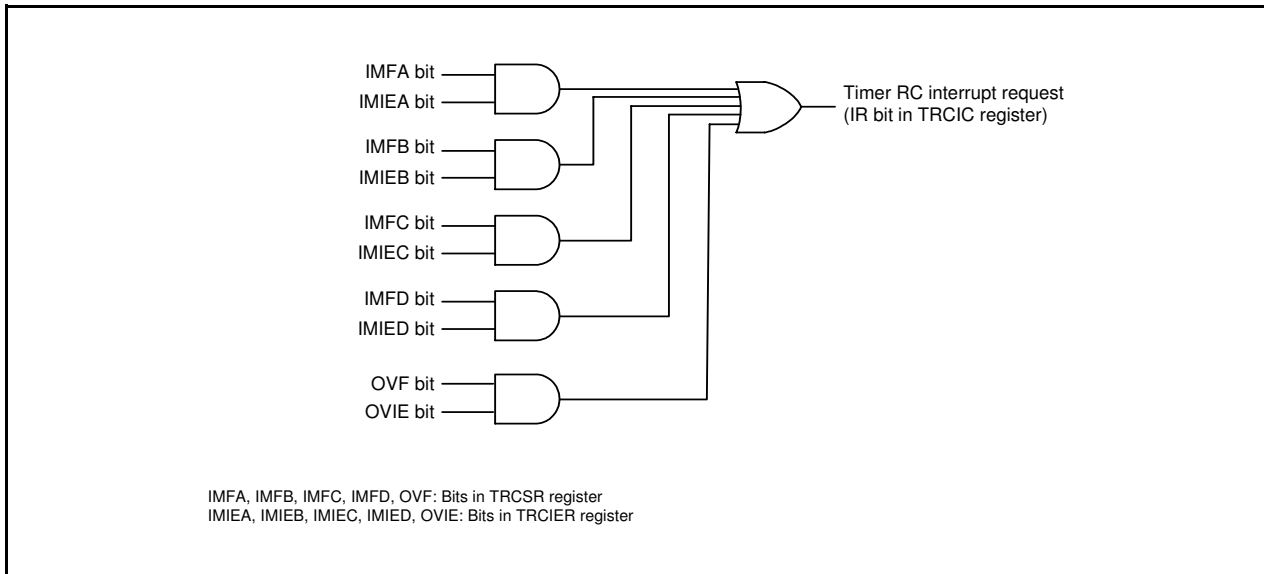
## 18.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.

Table 18.15 lists the Registers Associated with Timer RC Interrupt, and Figure 18.20 is a Timer RC Interrupt Block Diagram.

**Table 18.15 Registers Associated with Timer RC Interrupt**

| Timer RC Status Register | Timer RC Interrupt Enable Register | Timer RC Interrupt Control Register |
|--------------------------|------------------------------------|-------------------------------------|
| TRCSR                    | TRCIER                             | TRCIC                               |



**Figure 18.20 Timer RC Interrupt Block Diagram**

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **18.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **18.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.

Refer to **11.3 Interrupt Control**, for details of the TRCIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

## 18.9 Notes on Timer RC

### 18.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).

When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.

If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.W      #XXXXh, TRC          ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:        MOV.W      TRC,DATA      ;Read

```

### 18.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.B      #XXh, TRCSR        ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:        MOV.B      TRCSR,DATA    ;Read

```

### 18.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

### 18.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- Wait for a minimum of two cycles of f1.
- Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

- (1) Set the TSTART bit in the TRCMR register to 0 (count stops).
- (2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- (3) Wait for a minimum of two cycles of fOCO-F.
- (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

- (1) Set the TSTART bit in the TRCMR register to 0 (count stops).
- (2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- (3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
- (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

### 18.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  - [When the digital filter is not used]  
Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operation Clock**)
  - [When the digital filter is used]  
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Digital Filter Block Diagram**).
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

### 18.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

### 18.9.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

## 19. Timer RE

Timer RE has an 8-bit counter with a 4-bit prescaler.

### 19.1 Overview

Timer RE has the following mode:

- Real-time clock mode      Generate 1-second signal from fC4 and count seconds, minutes, hours, and days of the week.

The count source for timer RE is the operating clock that regulates the timing of timer operations.

### 19.2 Real-Time Clock Mode

In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week. Figure 19.1 shows a Block Diagram of Real-Time Clock Mode and Table 19.1 lists the Real-Time Clock Mode Specifications. Table 19.2 lists the Interrupt Sources, Figure 19.2 shows the Definition of Time Representation and Figure 19.3 shows the Operating Example in Real-Time Clock Mode.

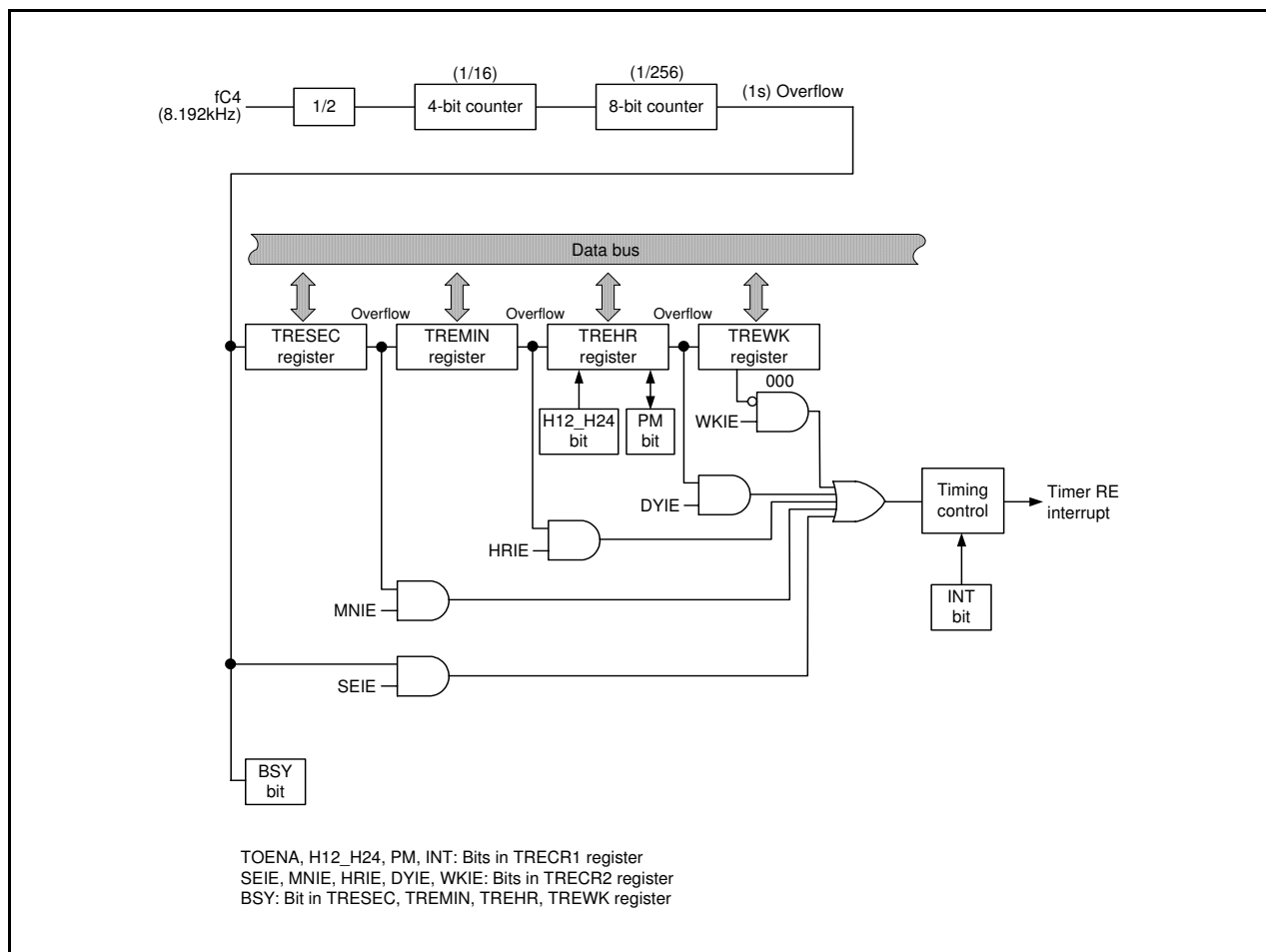


Figure 19.1 Block Diagram of Real-Time Clock Mode

**Table 19.1 Real-Time Clock Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Count source                        | fC4   |
| Count operation                     | Increment   |
| Count start condition               | 1 (count starts) is written to TSTART bit in TRECR1 register  |
| Count stop condition                | 0 (count stops) is written to TSTART bit in TRECR1 register   |
| Interrupt request generation timing | Select any one of the following: <ul style="list-style-type: none"> <li>• Update second data</li> <li>• Update minute data</li> <li>• Update hour data</li> <li>• Update day of week data</li> <li>• When day of week data is set to 000b (Sunday)</li> </ul> |
| Read from timer                     | When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.   |
| Write to timer                      | When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.             |
| Select function                     | 12-hour mode/24-hour mode switch function   |

### 19.2.1 Timer RE Second Data Register (TRESEC) in Real-Time Clock Mode

Address 0118h

|             |     |      |      |      |      |      |      |      |
|-------------|-----|------|------|------|------|------|------|------|
| Bit         | b7  | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | BSY | SC12 | SC11 | SC10 | SC03 | SC02 | SC01 | SC00 |
| After Reset | 0   | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                      | Function   | Setting Range        | R/W |
|-----|--------|-------------------------------|--|----------------------|-----|
| b0  | SC00   | 1st digit of second count bit | Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second. | 0 to 9<br>(BCD code) | R/W |
| b1  | SC01   |                               |  |                      | R/W |
| b2  | SC02   |                               |  |                      | R/W |
| b3  | SC03   |                               |  |                      | R/W |
| b4  | SC10   | 2nd digit of second count bit | When counting 0 to 5, 60 seconds are counted.  | 0 to 5<br>(BCD code) | R/W |
| b5  | SC11   |                               |  |                      | R/W |
| b6  | SC12   |                               |  |                      | R/W |
| b7  | BSY    | Timer RE busy flag            | This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated          |                      | R   |

### 19.2.2 Timer RE Minute Data Register (TREMIN) in Real-Time Clock Mode

Address 0119h

|             |     |      |      |      |      |      |      |      |
|-------------|-----|------|------|------|------|------|------|------|
| Bit         | b7  | b6   | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | BSY | MN12 | MN11 | MN10 | MN03 | MN02 | MN01 | MN00 |
| After Reset | 0   | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                      | Function   | Setting Range        | R/W |
|-----|--------|-------------------------------|--|----------------------|-----|
| b0  | MN00   | 1st digit of minute count bit | Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute. | 0 to 9<br>(BCD code) | R/W |
| b1  | MN01   |                               |  |                      | R/W |
| b2  | MN02   |                               |  |                      | R/W |
| b3  | MN03   |                               |  |                      | R/W |
| b4  | MN10   | 2nd digit of minute count bit | When counting 0 to 5, 60 minutes are counted.  | 0 to 5<br>(BCD code) | R/W |
| b5  | MN11   |                               |  |                      | R/W |
| b6  | MN12   |                               |  |                      | R/W |
| b7  | BSY    | Timer RE busy flag            | This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.         |                      | R   |



### 19.2.3 Timer RE Hour Data Register (TREHR) in Real-Time Clock Mode

Address 011Ah

|             |     |    |      |      |      |      |      |      |
|-------------|-----|----|------|------|------|------|------|------|
| Bit         | b7  | b6 | b5   | b4   | b3   | b2   | b1   | b0   |
| Symbol      | BSY | —  | HR11 | HR10 | HR03 | HR02 | HR01 | HR00 |
| After Reset | 0   | 0  | 0    | 0    | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | Setting Range        | R/W |
|-----|--------|---|--|----------------------|-----|
| b0  | HR00   | 1st digit of hour count bit   | Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.   | 0 to 9<br>(BCD code) | R/W |
| b1  | HR01   |   |  |                      | R/W |
| b2  | HR02   |   |  |                      | R/W |
| b3  | HR03   |   |  |                      | R/W |
| b4  | HR10   | 2nd digit of hour count bit   | Count 0 to 1 when the H12_H24 bit is set to 0 (12-hour mode).<br>Count 0 to 2 when the H12_H24 bit is set to 1 (24-hour mode). | 0 to 2<br>(BCD code) | R/W |
| b5  | HR11   |   |  |                      | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  |                      | —   |
| b7  | BSY    | Timer RE busy flag  | This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.   |                      | R   |

### 19.2.4 Timer RE Day of Week Data Register (TREWK) in Real-Time Clock Mode

Address 011Bh

|             |     |    |    |    |    |     |     |     |
|-------------|-----|----|----|----|----|-----|-----|-----|
| Bit         | b7  | b6 | b5 | b4 | b3 | b2  | b1  | b0  |
| Symbol      | BSY | —  | —  | —  | —  | WK2 | WK1 | WK0 |
| After Reset | 0   | 0  | 0  | 0  | 0  | 0   | 0   | 0   |

| Bit | Symbol | Bit Name  | Function   | R/W |   |
|-----|--------|---|--|-----|---|
| b0  | WK0    | Day of week count bit   | $b_2 b_1 b_0$<br>0 0 0: Sunday<br>0 0 1: Monday<br>0 1 0: Tuesday<br>0 1 1: Wednesday<br>1 0 0: Thursday<br>1 0 1: Friday<br>1 1 0: Saturday<br>1 1 1: Do not set. | R/W |   |
| b1  | WK1    |   |  | R/W |   |
| b2  | WK2    |   |  | R/W |   |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  |     | — |
| b4  | —      |   |  |     |   |
| b5  | —      |   |  |     |   |
| b6  | —      |   |  |     |   |
| b7  | BSY    | Timer RE busy flag  | This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.   | R   |   |

### 19.2.5 Timer RE Control Register 1 (TRECRR1) in Real-Time Clock Mode

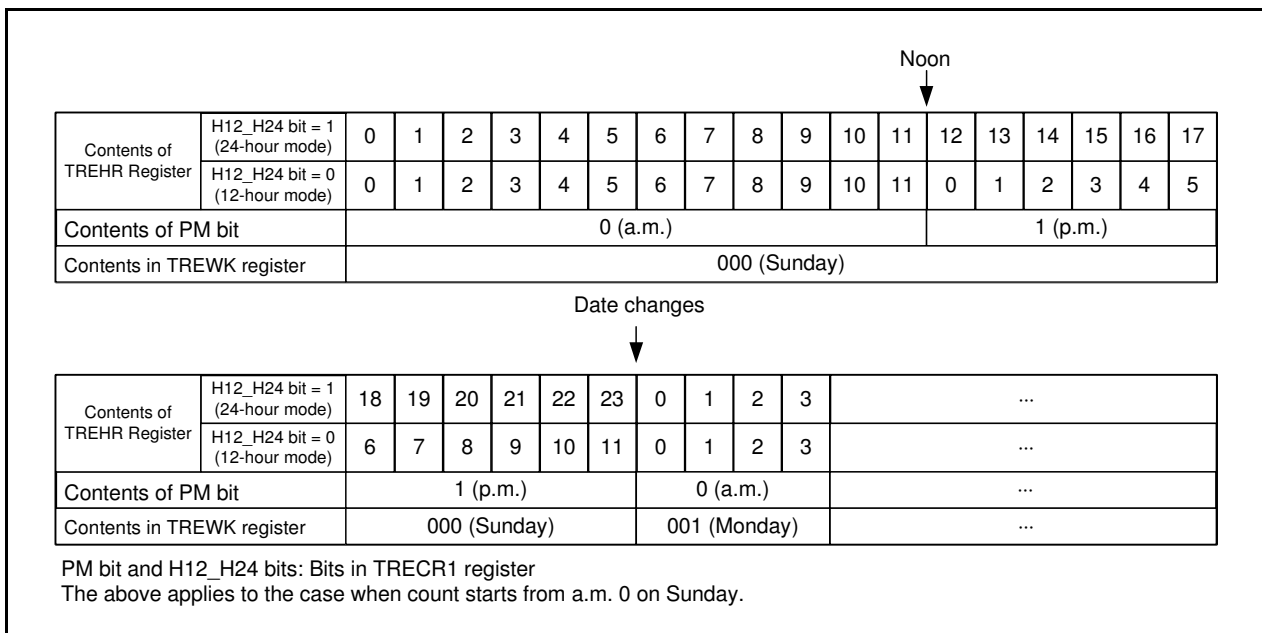
Address 011Ch

| Bit         | b7     | b6      | b5 | b4     | b3  | b2 | b1    | b0 |
|-------------|--------|---------|----|--------|-----|----|-------|----|
| Symbol      | TSTART | H12_H24 | PM | TRERST | INT | —  | TCSTF | —  |
| After Reset | 0      | 0       | 0  | 0      | 0   | 0  | 0     | 0  |

| Bit | Symbol  | Bit Name  | Function  | R/W |
|-----|---------|---|---|-----|
| b0  | —       | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b1  | TCSTF   | Timer RE count status flag  | 0: Count stopped<br>1: Counting   | R   |
| b2  | —       | Reserved bit  | Set to 0.   | R/W |
| b3  | INT     | Interrupt request timing bit  | Set to 1 in real-time clock mode.   | R/W |
| b4  | TRERST  | Timer RE reset bit  | When setting this bit to 0, after setting it to 1, the followings will occur.<br>• Registers TRESEC, TREMIN, TREHR, TREWK, and TRECRR2 are set to 00h.<br>• Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECRR1 register are set to 0.<br>• The 8-bit counter is set to 00h and the 4-bit counter is set to 0h. | R/W |
| b5  | PM      | A.m./p.m. bit   | When the H12_H24 bit is set to 0 (12-hour mode) <sup>(1)</sup><br>0: a.m.<br>1: p.m.<br>When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.  | R/W |
| b6  | H12_H24 | Operating mode select bit   | 0: 12-hour mode<br>1: 24-hour mode  | R/W |
| b7  | TSTART  | Timer RE count start bit  | 0: Count stops<br>1: Count starts   | R/W |

Note:

- This bit is automatically modified while timer RE counts.



**Figure 19.2 Definition of Time Representation**

### 19.2.6 Timer RE Control Register 2 (TREC2) in Real-Time Clock Mode

Address 011Dh

|             |    |    |    |      |      |      |      |      |
|-------------|----|----|----|------|------|------|------|------|
| Bit         | b7 | b6 | b5 | b4   | b3   | b2   | b1   | b0   |
| Symbol      | —  | —  | —  | WKIE | DYIE | HRIE | MNIE | SEIE |
| After Reset | 0  | 0  | 0  | 0    | 0    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | SEIE   | Periodic interrupt triggered every second enable bit <sup>(1)</sup>       | 0: Disable periodic interrupt triggered every second<br>1: Enable periodic interrupt triggered every second | R/W |
| b1  | MNIE   | Periodic interrupt triggered every minute enable bit <sup>(1)</sup>       | 0: Disable periodic interrupt triggered every minute<br>1: Enable periodic interrupt triggered every minute | R/W |
| b2  | HRIE   | Periodic interrupt triggered every hour enable bit <sup>(1)</sup>         | 0: Disable periodic interrupt triggered every hour<br>1: Enable periodic interrupt triggered every hour     | R/W |
| b3  | DYIE   | Periodic interrupt triggered every day enable bit <sup>(1)</sup>          | 0: Disable periodic interrupt triggered every day<br>1: Enable periodic interrupt triggered every day       | R/W |
| b4  | WKIE   | Periodic interrupt triggered every week enable bit <sup>(1)</sup>         | 0: Disable periodic interrupt triggered every week<br>1: Enable periodic interrupt triggered every week     | R/W |
| b5  | —      | Reserved bit  | Set to 0.   | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b7  | —      |   |   |     |

Note:

- Do not set multiple enable bits to 1 (enable interrupt).

**Table 19.2 Interrupt Sources**

| Factor                                    | Interrupt Source  | Interrupt Enable Bit |
|---|---|----------------------|
| Periodic interrupt triggered every week   | Value in TREWK register is set to 000b (Sunday) (1-week period) | WKIE                 |
| Periodic interrupt triggered every day    | TREWK register is updated (1-day period)                        | DYIE                 |
| Periodic interrupt triggered every hour   | TREHR register is updated (1-hour period)                       | HRIE                 |
| Periodic interrupt triggered every minute | TREMIN register is updated (1-minute period)                    | MNIE                 |
| Periodic interrupt triggered every second | TRESEC register is updated (1-second period)                    | SEIE                 |

### 19.2.7 Timer RE Count Source Select Register (TRECSR) in Real-Time Clock Mode

Address 011Eh

|             |    |    |    |    |      |      |      |      |
|-------------|----|----|----|----|------|------|------|------|
| Bit         | b7 | b6 | b5 | b4 | b3   | b2   | b1   | b0   |
| Symbol      | —  | —  | —  | —  | RCS3 | RCS2 | RCS1 | RCS0 |
| After Reset | 0  | 0  | 0  | 0  | 1    | 0    | 0    | 0    |

| Bit | Symbol | Bit Name  | Function                            | R/W |
|-----|--------|---|-------------------------------------|-----|
| b0  | RCS0   | Count source select bit   | Set to 00b in real-time clock mode. | R/W |
| b1  | RCS1   |   |                                     | R/W |
| b2  | RCS2   | 4-bit counter select bit  | Set to 0 in real-time clock mode.   | R/W |
| b3  | RCS3   | Real-time clock mode select bit   | Set to 1 in real-time clock mode.   | R/W |
| b4  | —      | Reserved bits   | Set to 0.                           | R/W |
| b5  | —      |   |                                     |     |
| b6  | —      |   |                                     |     |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |                                     | —   |

### 19.2.8 Operating Example

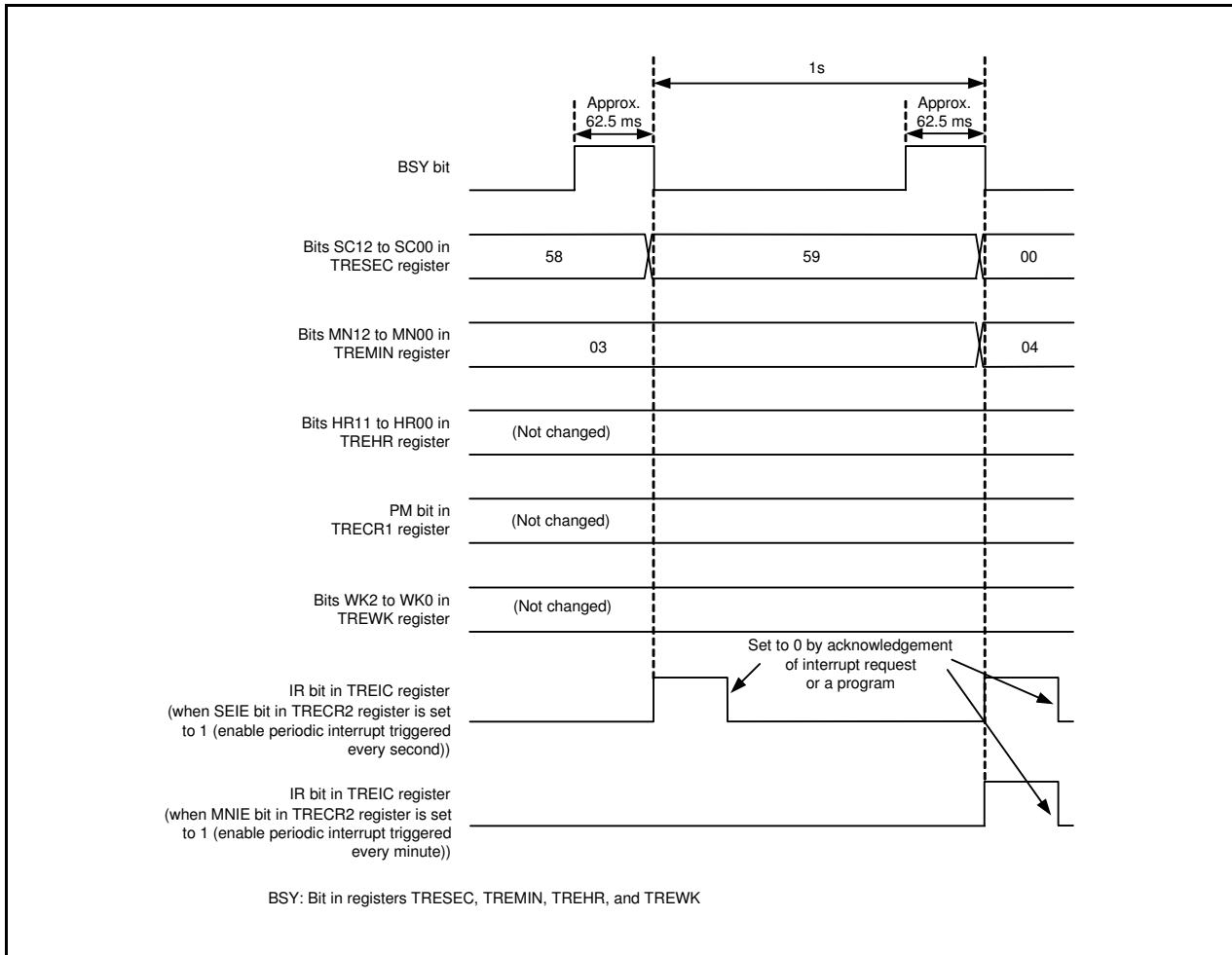


Figure 19.3 Operating Example in Real-Time Clock Mode

## 19.3 Notes on Timer RE

### 19.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TREC1 register.

Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE <sup>(1)</sup> other than the TCSTF bit.

Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:

1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TREC1, TREC2, and TRECSR.

### 19.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TREC2
- Bits H12\_H24, PM, and INT in TREC1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TREC1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TREC2 register.

Figure 19.4 shows a Setting Example in Real-Time Clock Mode.

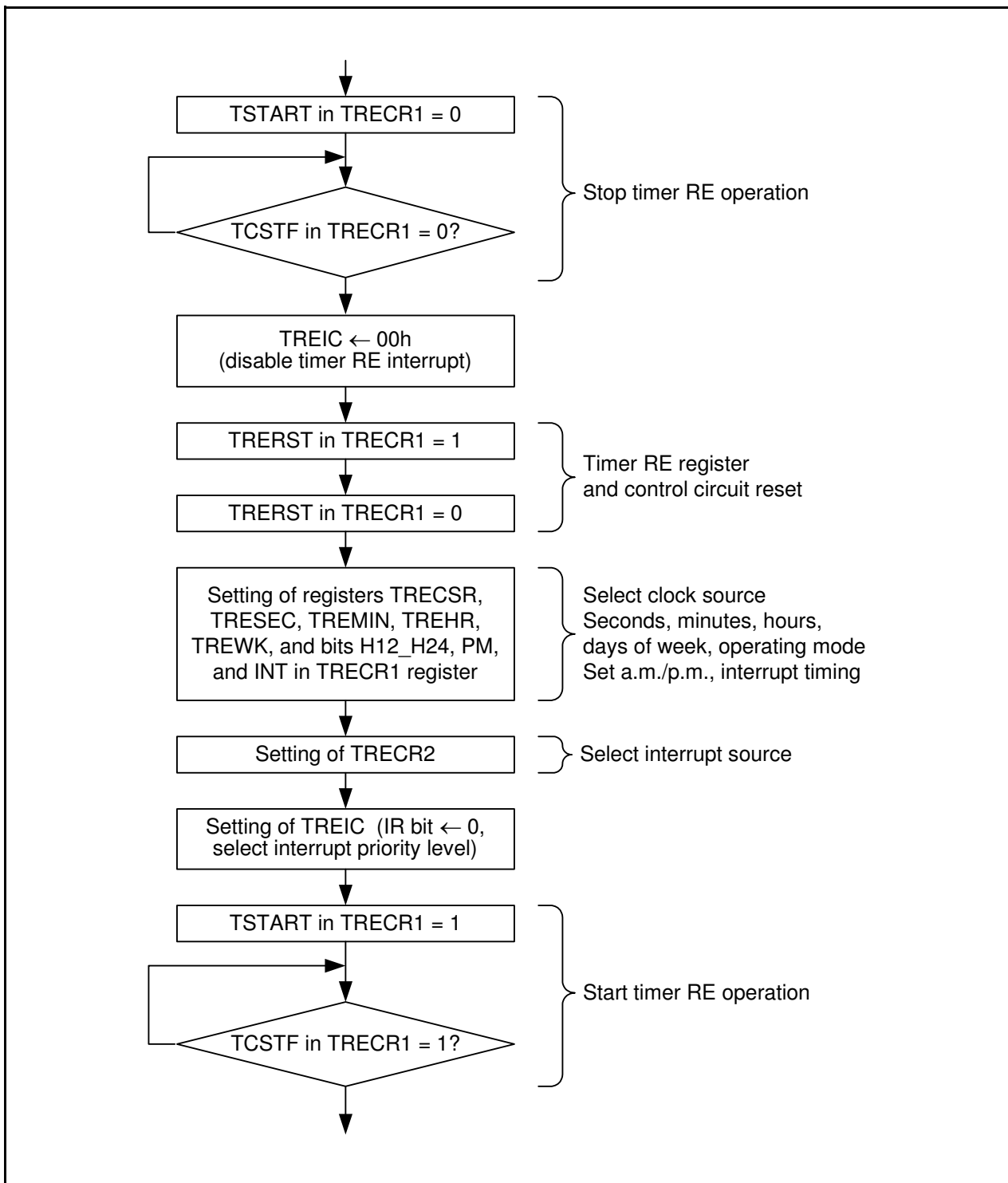


Figure 19.4 Setting Example in Real-Time Clock Mode

### 19.3.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECRI register when the BSY bit is set to 0 (not while data is updated).

Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt

Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register in the timer RE interrupt routine.

- Monitoring with a program 1

Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.

(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).

(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register.

(2) Read the same register as (1) and compare the contents.

(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.



## 20. Serial Interface (UART0)

The serial interface consists of two channels, UART0, UART2. This chapter describes the UART0.

### 20.1 Overview

UART0 has a dedicated timer to generate a transfer clock and operate independently. UART0 supports clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).

Figure 20.1 shows a UART0 Block Diagram. Figure 20.2 shows a Block Diagram of UART0 Transmit/Receive Unit. Table 20.1 lists the Pin Configuration of UART0.

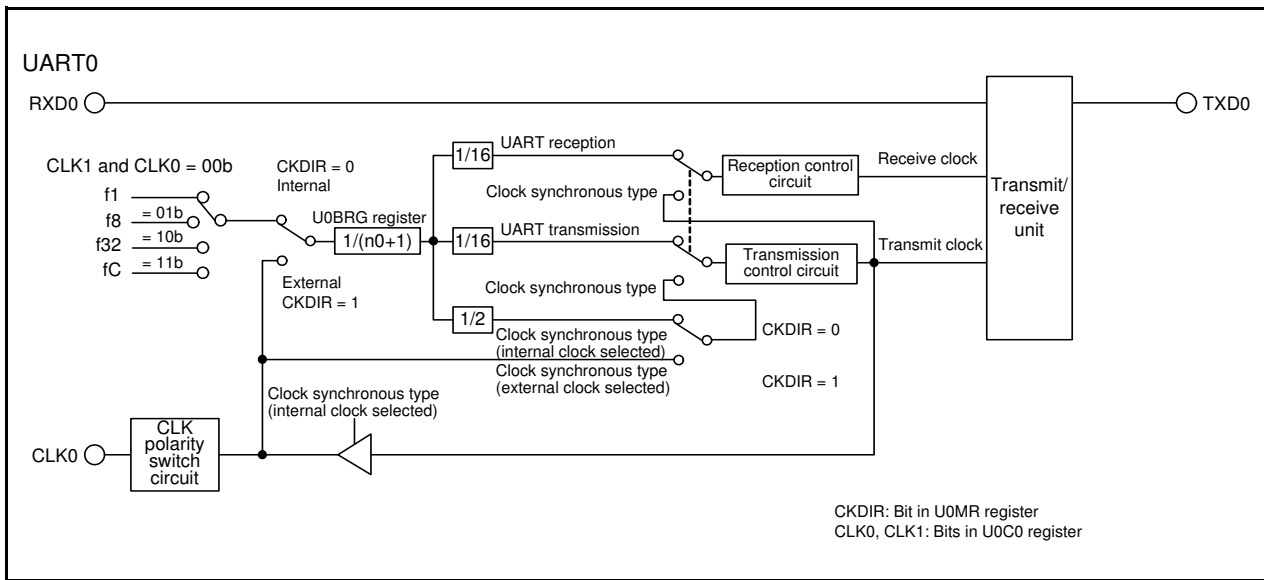


Figure 20.1 UART0 Block Diagram

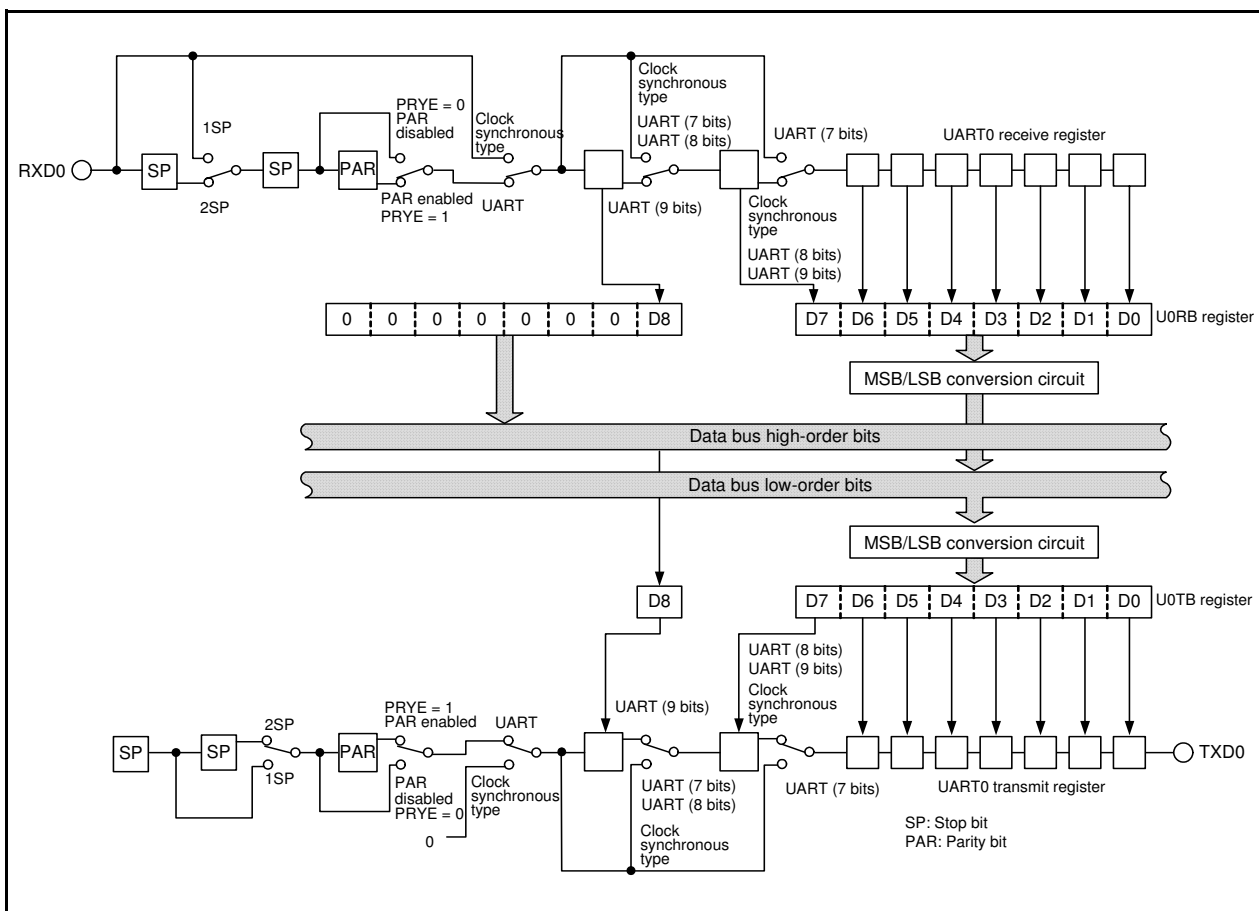


Figure 20.2 Block Diagram of UART0 Transmit/Receive Unit

Table 20.1 Pin Configuration of UART0

| Pin Name | Assigned Pin | I/O    | Function           |
|----------|--------------|--------|--------------------|
| TXD0     | P1_4         | Output | Serial data output |
| RXD0     | P1_5         | Input  | Serial data input  |
| CLK0     | P1_6         | I/O    | Transfer clock I/O |

## 20.2 Registers

### 20.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00A0h

|             |    |      |     |      |       |      |      |      |
|-------------|----|------|-----|------|-------|------|------|------|
| Bit         | b7 | b6   | b5  | b4   | b3    | b2   | b1   | b0   |
| Symbol      | —  | PRYE | PRY | STPS | CKDIR | SMD2 | SMD1 | SMD0 |
| After Reset | 0  | 0    | 0   | 0    | 0     | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                           | Function   | R/W |
|-----|--------|------------------------------------|--|-----|
| b0  | SMD0   | Serial I/O mode select bit         | b2 b1 b0<br>0 0 0: Serial interface disabled<br>0 0 1: Clock synchronous serial I/O mode<br>1 0 0: UART mode, transfer data 7 bits long<br>1 0 1: UART mode, transfer data 8 bits long<br>1 1 0: UART mode, transfer data 9 bits long<br>Other than above: Do not set. | R/W |
| b1  | SMD1   |                                    |  | R/W |
| b2  | SMD2   |                                    |  | R/W |
| b3  | CKDIR  | Internal/external clock select bit | 0: Internal clock<br>1: External clock   | R/W |
| b4  | STPS   | Stop bit length select bit         | 0: One stop bit<br>1: Two stop bits  | R/W |
| b5  | PRY    | Odd/even parity select bit         | Enabled when PRYE = 1<br>0: Odd parity<br>1: Even parity   | R/W |
| b6  | PRYE   | Parity enable bit                  | 0: Parity disabled<br>1: Parity enabled  | R/W |
| b7  | —      | Reserved bit                       | Set to 0.  | R/W |

### 20.2.2 UART0 Bit Rate Register (U0BRG)

Address 00A1h

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit      | Function  | Setting Range | R/W |
|----------|---|---------------|-----|
| b7 to b0 | If the setting value is n, U0BRG divides the count source by n+1. | 00h to FFh    | W   |

Write to the U0BRG register while transmission and reception stop.

Use the MOV instruction to write to this register.

Set bits CLK0 and CLK1 in the U0C0 register before writing to the U0BRG register.

### 20.2.3 UART0 Transmit Buffer Register (U0TB)

Address 00A3h to 00A2h

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

|             |     |     |     |     |     |     |    |    |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | —  |
| After Reset | X   | X   | X   | X   | X   | X   | X  | X  |

| Bit | Symbol | Function  | R/W |
|-----|--------|---|-----|
| b0  | —      | Transmit data   | W   |
| b1  | —      |   |     |
| b2  | —      |   |     |
| b3  | —      |   |     |
| b4  | —      |   |     |
| b5  | —      |   |     |
| b6  | —      |   |     |
| b7  | —      |   |     |
| b8  | —      |   |     |
| b9  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. | —   |
| b10 | —      |   |     |
| b11 | —      |   |     |
| b12 | —      |   |     |
| b13 | —      |   |     |
| b14 | —      |   |     |
| b15 | —      |   |     |

If the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the U0TB register.

Use the MOV instruction to write to this register.

### 20.2.4 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00A4h

| Bit         | b7    | b6    | b5  | b4 | b3    | b2 | b1   | b0   |
|-------------|-------|-------|-----|----|-------|----|------|------|
| Symbol      | UFORM | CKPOL | NCH | —  | TXEPT | —  | CLK1 | CLK0 |
| After Reset | 0     | 0     | 0   | 0  | 1     | 0  | 0    | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | CLK0   | BRG count source select bit <sup>(1)</sup>                                | <sup>b1 b0</sup><br>0 0: f1 selected<br>0 1: f8 selected<br>1 0: f32 selected<br>1 1: fC selected  | R/W |
| b1  | CLK1   |   |  | R/W |
| b2  | —      | Reserved bit  | Set to 0.  | R/W |
| b3  | TXEPT  | Transmit register empty flag  | 0: Data present in the transmit register<br>(transmission in progress)<br>1: No data in the transmit register<br>(transmission completed)  | R   |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b5  | NCH    | Data output select bit  | 0: TXD0 pin set to CMOS output<br>1: TXD0 pin set to N-channel open-drain output   | R/W |
| b6  | CKPOL  | CLK polarity select bit   | 0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock<br>1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock | R/W |
| b7  | UFORM  | Transfer format select bit  | 0: LSB first<br>1: MSB first   | R/W |

Note:

1. If the BRG count source is switched, set the U0BRG register again.

### 20.2.5 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00A5h

| Bit         | b7 | b6 | b5    | b4    | b3 | b2 | b1 | b0 |
|-------------|----|----|-------|-------|----|----|----|----|
| Symbol      | —  | —  | U0RRM | U0IRS | RI | RE | TI | TE |
| After Reset | 0  | 0  | 0     | 0     | 0  | 0  | 1  | 0  |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | TE     | Transmit enable bit   | 0: Transmission disabled<br>1: Transmission enabled                            | R/W |
| b1  | TI     | Transmit buffer empty flag  | 0: Data present in the U0TB register<br>1: No data in the U0TB register        | R   |
| b2  | RE     | Receive enable bit  | 0: Reception disabled<br>1: Reception enabled                                  | R/W |
| b3  | RI     | Receive complete flag <sup>(1)</sup>                                      | 0: No data in the U0RB register<br>1: Data present in the U0RB register        | R   |
| b4  | U0IRS  | UART0 transmit interrupt source select bit                                | 0: Transmission buffer empty (TI = 1)<br>1: Transmission completed (TXEPT = 1) | R/W |
| b5  | U0RRM  | UART0 continuous receive mode enable bit <sup>(2)</sup>                   | 0: Continuous receive mode disabled<br>1: Continuous receive mode enabled      | R/W |
| b6  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b7  | —      |   |  |     |

Notes:

1. The RI bit is set to 0 when the higher byte of the U0RB register is read.
2. In UART mode, set the U0RRM bit to 0 (continuous receive mode disabled).

### 20.2.6 UART0 Receive Buffer Register (U0RB)

Address 00A7h to 00A6h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Symbol      | SUM | PER | FER | OER | —   | —   | —  | —  |
| After Reset | X   | X   | X   | X   | X   | X   | X  | X  |

| Bit | Symbol | Bit Name  | Function                                | R/W                               |
|-----|--------|---|---|-----------------------------------|
| b0  | —      | —   | Receive data (D7 to D0)                 | R                                 |
| b1  | —      |   |   |                                   |
| b2  | —      |   |   |                                   |
| b3  | —      |   |   |                                   |
| b4  | —      |   |   |                                   |
| b5  | —      |   |   |                                   |
| b6  | —      |   |   |                                   |
| b7  | —      |   |   |                                   |
| b8  | —      | —   | Receive data (D8)                       | R                                 |
| b9  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |   | —                                 |
| b10 | —      |   |   |                                   |
| b11 | —      |   |   |                                   |
| b12 | OER    |   |   | Overrun error flag <sup>(1)</sup> |
| b13 | FER    | Framing error flag <sup>(1, 2)</sup>  | 0: No framing error<br>1: Framing error | R                                 |
| b14 | PER    | Parity error flag <sup>(1, 2)</sup>   | 0: No parity error<br>1: Parity error   | R                                 |
| b15 | SUM    | Error sum flag <sup>(1, 2)</sup>  | 0: No error<br>1: Error                 | R                                 |

## Notes:

- Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
  - Bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled), or
  - The RE bit in the U0C1 register is set to 0 (reception disabled)
 The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).  
 Bits PER and FER are also set to 0 when the high-order byte of the U0RB register is read.  
 When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the U0RB register in 16-bit units.

### 20.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

|             |    |    |    |          |    |          |    |          |
|-------------|----|----|----|----------|----|----------|----|----------|
| Bit         | b7 | b6 | b5 | b4       | b3 | b2       | b1 | b0       |
| Symbol      | —  | —  | —  | CLK0SEL0 | —  | RXD0SEL0 | —  | TXD0SEL0 |
| After Reset | 0  | 0  | 0  | 0        | 0  | 0        | 0  | 0        |

| Bit | Symbol   | Bit Name  | Function                                 | R/W |
|-----|----------|---|--|-----|
| b0  | TXD0SEL0 | TXD0 pin select bit   | 0: TXD0 pin not used<br>1: P1_4 assigned | R/W |
| b1  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b2  | RXD0SEL0 | RXD0 pin select bit   | 0: RXD0 pin not used<br>1: P1_5 assigned | R/W |
| b3  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b4  | CLK0SEL0 | CLK0 pin select bit   | 0: CLK0 pin not used<br>1: P1_6 assigned | R/W |
| b5  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b6  | —        |   |  |     |
| b7  | —        |   |  |     |

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.

Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

### 20.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.

Table 20.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 20.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

**Table 20.2 Clock Synchronous Serial I/O Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Transfer data format                | <ul style="list-style-type: none"> <li>Transfer data length: 8 bits</li> </ul>  |
| Transfer clocks                     | <ul style="list-style-type: none"> <li>The CKDIR bit in the U0MR register is set to 0 (internal clock): <math>f_i/(2(n+1))</math><br/> <math>f_i = f_1, f_8, f_{32}, f_C</math> n = setting value in the U0BRG register: 00h to FFh</li> <li>The CKDIR bit is set to 1 (external clock): Input from the CLK0 pin</li> </ul>   |
| Transmit start conditions           | <ul style="list-style-type: none"> <li>To start transmission, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>The TE bit in the U0C1 register is set to 1 (transmission enabled).</li> <li>The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).</li> </ul> </li> </ul>  |
| Receive start conditions            | <ul style="list-style-type: none"> <li>To start reception, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>The RE bit in the U0C1 register is set to 1 (reception enabled).</li> <li>The TE bit in the U0C1 register is set to 1 (transmission enabled).</li> <li>The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).</li> </ul> </li> </ul>   |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>For transmission: One of the following can be selected. <ul style="list-style-type: none"> <li>The U0IRS bit is set to 0 (transmit buffer empty):<br/>When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission).</li> <li>The U0IRS bit is set to 1 (transmission completed):<br/>When data transmission from the UART0 transmit register is completed.</li> </ul> </li> <li>For reception:<br/>When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).</li> </ul> |
| Error detection                     | <ul style="list-style-type: none"> <li>Overrun error <sup>(2)</sup><br/>This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receives the 7th bit of the next unit of data.</li> </ul>   |
| Selectable functions                | <ul style="list-style-type: none"> <li>CLK polarity selection<br/>Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock.</li> <li>LSB first, MSB first selection<br/>Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected.</li> <li>Continuous receive mode selection<br/>Reception is enabled immediately by reading the U0RB register.</li> </ul>  |

Notes:

- When an external clock is selected, the requirements must be met in either of the following states:
  - The external clock is held high when the CKPOL bit in the U0C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
  - The external clock is held low when the CKPOL bit in the U0C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
- If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined. The IR bit in the S0RIC register remains unchanged.



**Table 20.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode<sup>(1)</sup>**

| Register | Bit          | Function  |
|----------|--------------|---|
| U0TB     | b0 to b7     | Set data transmission.                          |
| U0RB     | b0 to b7     | Receive data can be read.                       |
|          | OER          | Overflow error flag                             |
| U0BRG    | b0 to b7     | Set a bit rate.                                 |
| U0MR     | SMD2 to SMD0 | Set to 001b.                                    |
|          | CKDIR        | Select the internal clock or external clock.    |
| U0C0     | CLK1, CLK0   | Select the count source for the U0BRG register. |
|          | TXEPT        | Transmit register empty flag                    |
|          | NCH          | Select TXD0 pin output mode.                    |
|          | CKPOL        | Select the transfer clock polarity.             |
|          | UFORM        | Select LSB first or MSB first.                  |
| U0C1     | TE           | Set to 1 to enable transmission/reception       |
|          | TI           | Transmit buffer empty flag                      |
|          | RE           | Set to 1 to enable reception.                   |
|          | RI           | Receive complete flag                           |
|          | U0IRS        | Select the UART0 transmit interrupt source.     |
|          | U0RRM        | Set to 1 to use continuous receive mode.        |

Note:

1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 20.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.

After UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

**Table 20.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode**

| Pin Name    | Function              | Selection Method  |
|-------------|-----------------------|---|
| TXD0 (P1_4) | Serial data output    | TXD0SEL0 bit in U0SR register = 1<br>For reception only:<br>P1_4 can be used as a port by setting TXD0SEL0 bit = 0.                                     |
| RXD0 (P1_5) | Serial data input     | RXD0SEL0 bit in U0SR register = 1<br>PD1_5 bit in PD1 register = 0<br>For transmission only:<br>P1_5 can be used as a port by setting RXD0SEL0 bit = 0. |
| CLK0 (P1_6) | Transfer clock output | CLK0SEL0 bit in U0SR register = 1<br>CKDIR bit in U0MR register = 0   |
|             | Transfer clock input  | CLK0SEL0 bit in U0SR register = 1<br>CKDIR bit in U0MR register = 1<br>PD1_6 bit in PD1 register = 0  |

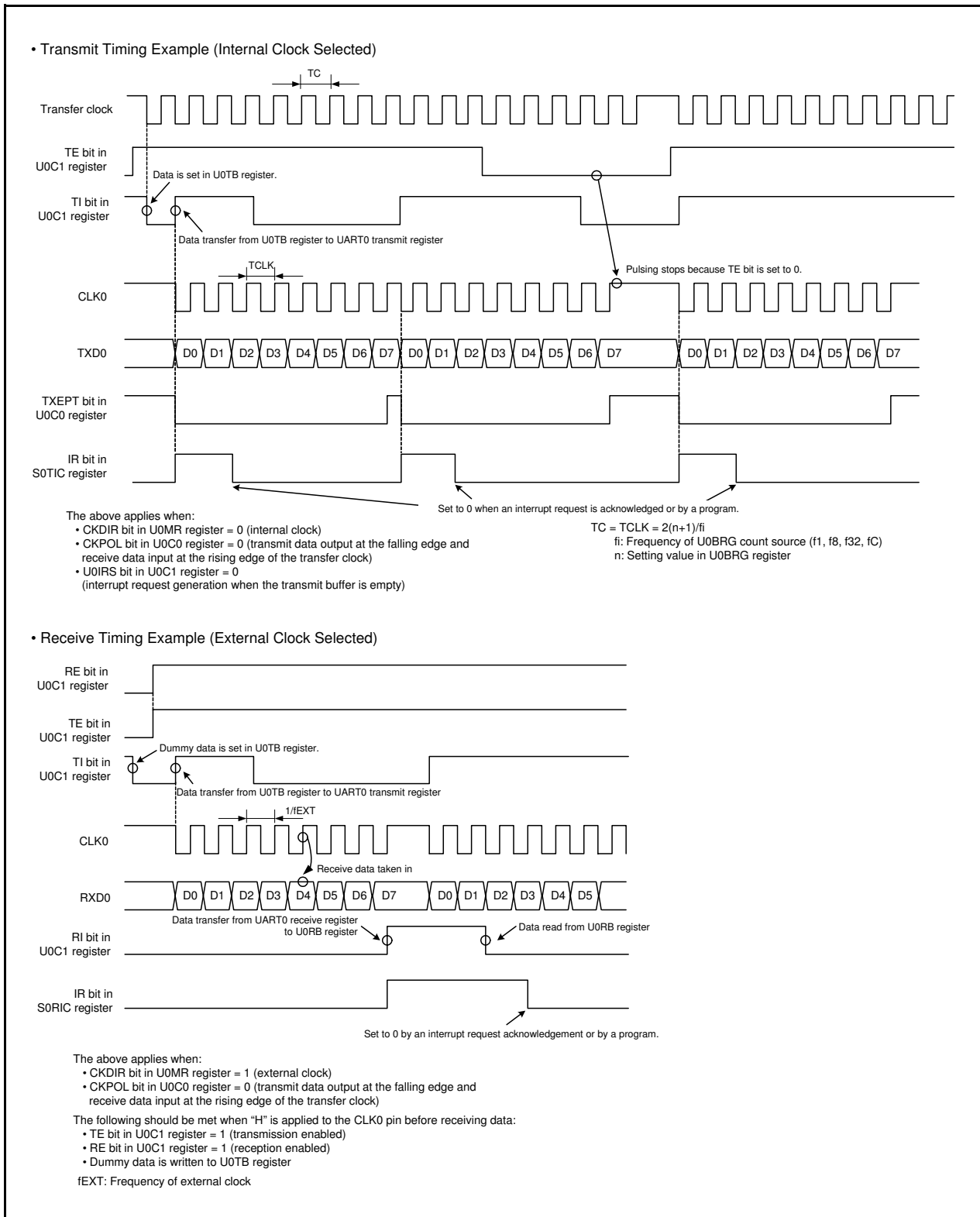


Figure 20.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

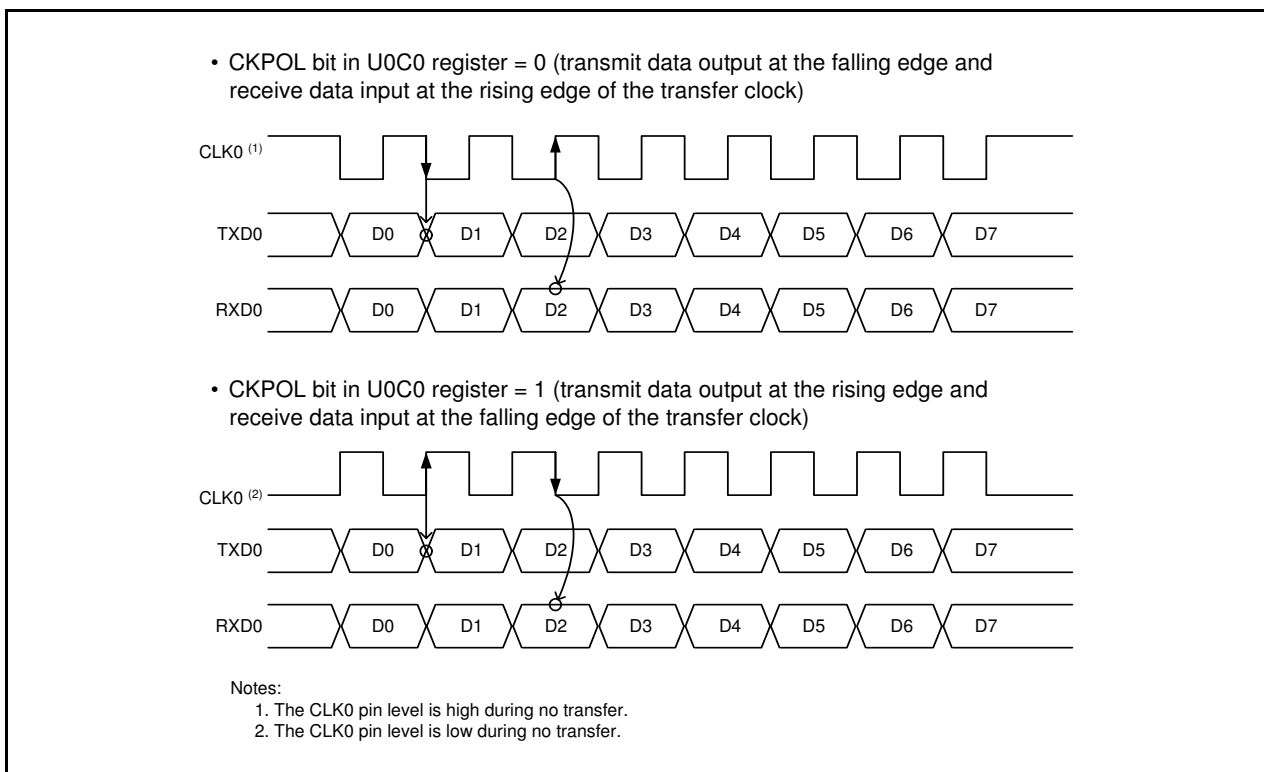
### 20.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

- (1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
- (4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

### 20.3.2 Polarity Select Function

Figure 20.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.



**Figure 20.4** Transfer Clock Polarity

### 20.3.3 LSB First/MSB First Select Function

Figure 20.5 shows the Transfer Format. Use the UFORM bit in the U0C0 register to select the transfer format.

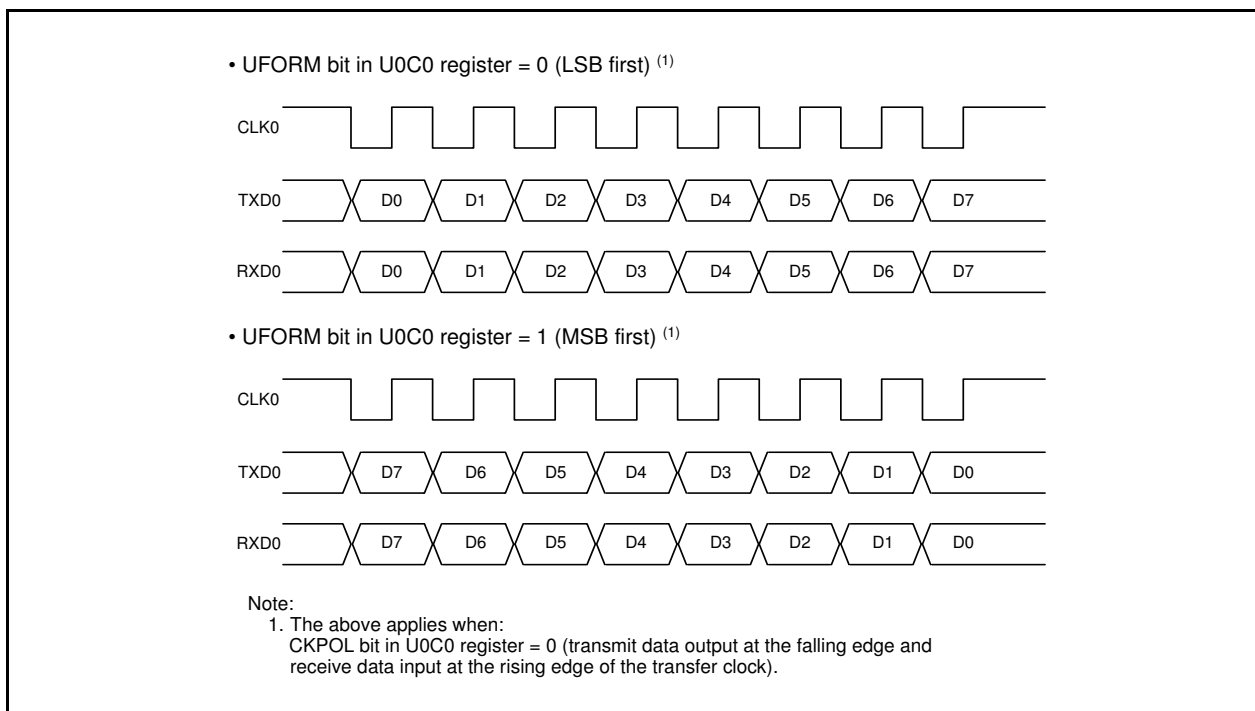


Figure 20.5 Transfer Format

### 20.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). If the U0RRM bit is set to 1, do not write dummy data to the U0TB register by a program.

## 20.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 20.5 lists the UART Mode Specifications. Table 20.6 lists the Registers Used and Settings in UART Mode.

**Table 20.5 UART Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Transfer data formats               | <ul style="list-style-type: none"> <li>• Character bits (transfer data): Selectable among 7, 8 or 9 bits</li> <li>• Start bit: 1 bit</li> <li>• Parity bit: Selectable among odd, even, or none</li> <li>• Stop bits: Selectable among 1 or 2 bits</li> </ul>   |
| Transfer clocks                     | <ul style="list-style-type: none"> <li>• The CKDIR bit in the U0MR register is set to 0 (internal clock): <math>f_j/(16(n+1))</math><br/> <math>f_j = f_1, f_8, f_{32}, f_C</math> <math>n =</math> setting value in the U0BRG register: 00h to FFh</li> <li>• The CKDIR bit is set to 1 (external clock): <math>f_{EXT}/(16(n+1))</math><br/> <math>f_{EXT}</math>: Input from the CLK0 pin,<br/> <math>n =</math> setting value in the U0BRG register: 00h to FFh</li> </ul>  |
| Transmit start conditions           | <ul style="list-style-type: none"> <li>• To start transmission, the following requirements must be met: <ul style="list-style-type: none"> <li>- The TE bit in the U0C1 register is set to 1 (transmission enabled).</li> <li>- The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).</li> </ul> </li> </ul>   |
| Receive start conditions            | <ul style="list-style-type: none"> <li>• To start reception, the following requirements must be met: <ul style="list-style-type: none"> <li>- The RE bit in the U0C1 register is set to 1 (reception enabled).</li> <li>- Start bit detection</li> </ul> </li> </ul>  |
| Interrupt request generation timing | <ul style="list-style-type: none"> <li>• For transmission: One of the following can be selected. <ul style="list-style-type: none"> <li>- The U0IRS bit is set to 0 (transmit buffer empty):<br/> When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission).</li> <li>- The U0IRS bit is set to 1 (transfer completed):<br/> When data transmission from the UART0 transmit register is completed.</li> </ul> </li> <li>• For reception:<br/> When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).</li> </ul>  |
| Error detection                     | <ul style="list-style-type: none"> <li>• Overrun error <sup>(1)</sup><br/> This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receive the bit one before the last stop bit of the next unit of data.</li> <li>• Framing error<br/> This error occurs when the set number of stop bits is not detected. <sup>(2)</sup></li> <li>• Parity error<br/> This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. <sup>(2)</sup></li> <li>• Error sum flag<br/> This flag is set to 1 if an overrun, framing, or parity error occurs.</li> </ul> |

Notes:

1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined. The IR bit in the SORIC register remains unchanged.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

**Table 20.6 Registers Used and Settings in UART Mode**

| Register | Bit             | Function   |
|----------|-----------------|--|
| U0TB     | b0 to b8        | Set transmit data. <sup>(1)</sup>  |
| U0RB     | b0 to b8        | Receive data can be read. <sup>(2)</sup>   |
|          | OER,FER,PER,SUM | Error flag   |
| U0BRG    | b0 to b7        | Set a bit rate.  |
| U0MR     | SMD2 to SMD0    | Set to 100b when transfer data is 7 bits long.<br>Set to 101b when transfer data is 8 bits long.<br>Set to 110b when transfer data is 9 bits long. |
|          | CKDIR           | Select the internal clock or external clock.   |
|          | STPS            | Select the stop bit.   |
|          | PRY, PRYE       | Select whether parity is included and whether odd or even.   |
| U0C0     | CLK0, CLK1      | Select the count source for the U0BRG register.  |
|          | TXEPT           | Transmit register empty flag   |
|          | NCH             | Select TXD0 pin output mode.   |
|          | CKPOL           | Set to 0.  |
|          | UFORM           | Select LSB first or MSB first when transfer data is 8 bits long.<br>Set to 0 when transfer data is 7 bits or 9 bits long.                          |
| U0C1     | TE              | Set to 1 to enable transmission.   |
|          | TI              | Transmit buffer empty flag   |
|          | RE              | Set to 1 to enable reception.  |
|          | RI              | Receive complete flag  |
|          | U0IRS           | Select the UART0 transmit interrupt source.  |
|          | U0RRM           | Set to 0.  |

## Notes:

- The bits used for transmission/receive data are as follows:
  - Bits b0 to b6 when transfer data is 7 bits long
  - Bits b0 to b7 when transfer data is 8 bits long
  - Bits b0 to b8 when transfer data is 9 bits long
- The contents of the following are undefined:
  - Bits 7 and 8 when the transfer data is 7 bits long
  - Bit 8 when the transfer data is 8 bits long

Table 20.7 lists the I/O Pin Functions in UART Mode.

After the UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

**Table 20.7 I/O Pin Functions in UART Mode**

| Pin name    | Function              | Selection Method  |
|-------------|-----------------------|---|
| TXD0 (P1_4) | Serial data output    | TXD0SEL0 bit in U0SR register = 1<br>For reception only:<br>P1_4 can be used as a port by setting TXD0SEL0 bit = 0.                                     |
| RXD0 (P1_5) | Serial data input     | RXD0SEL0 bit in U0SR register = 1<br>PD1_5 bit in PD1 register = 0<br>For transmission only:<br>P1_5 can be used as a port by setting RXD0SEL0 bit = 0. |
| CLK0 (P1_6) | Programmable I/O port | CLK0SEL0 bit in U0SR register = 0 (CLK0 pin not used)   |
|             | Transfer clock input  | CLK0SEL0 bit in U0SR register = 1<br>CKDIR bit in U0MR register = 1<br>PD1_6 bit in PD1 register = 0  |

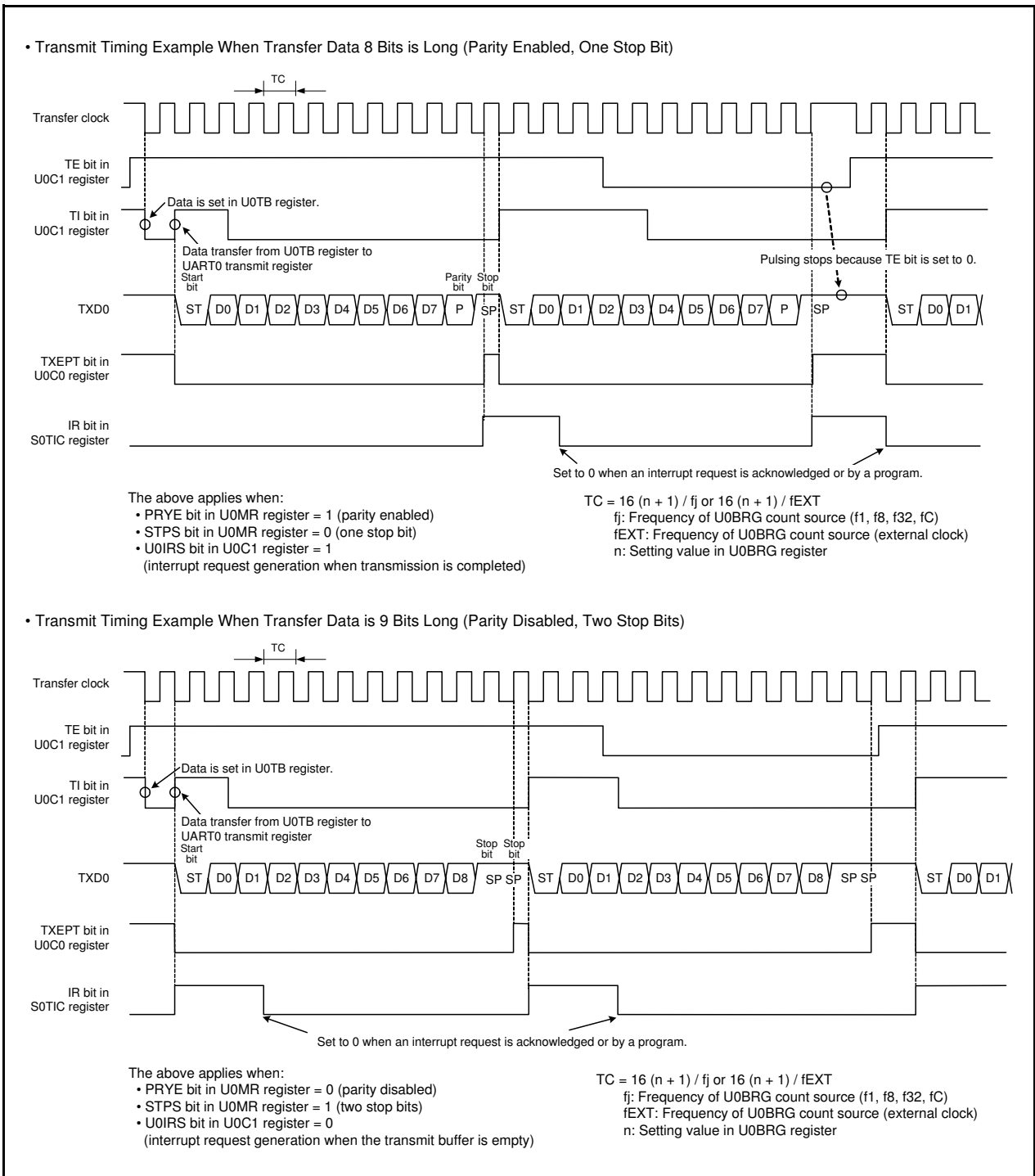


Figure 20.6 Transmit Timing in UART Mode



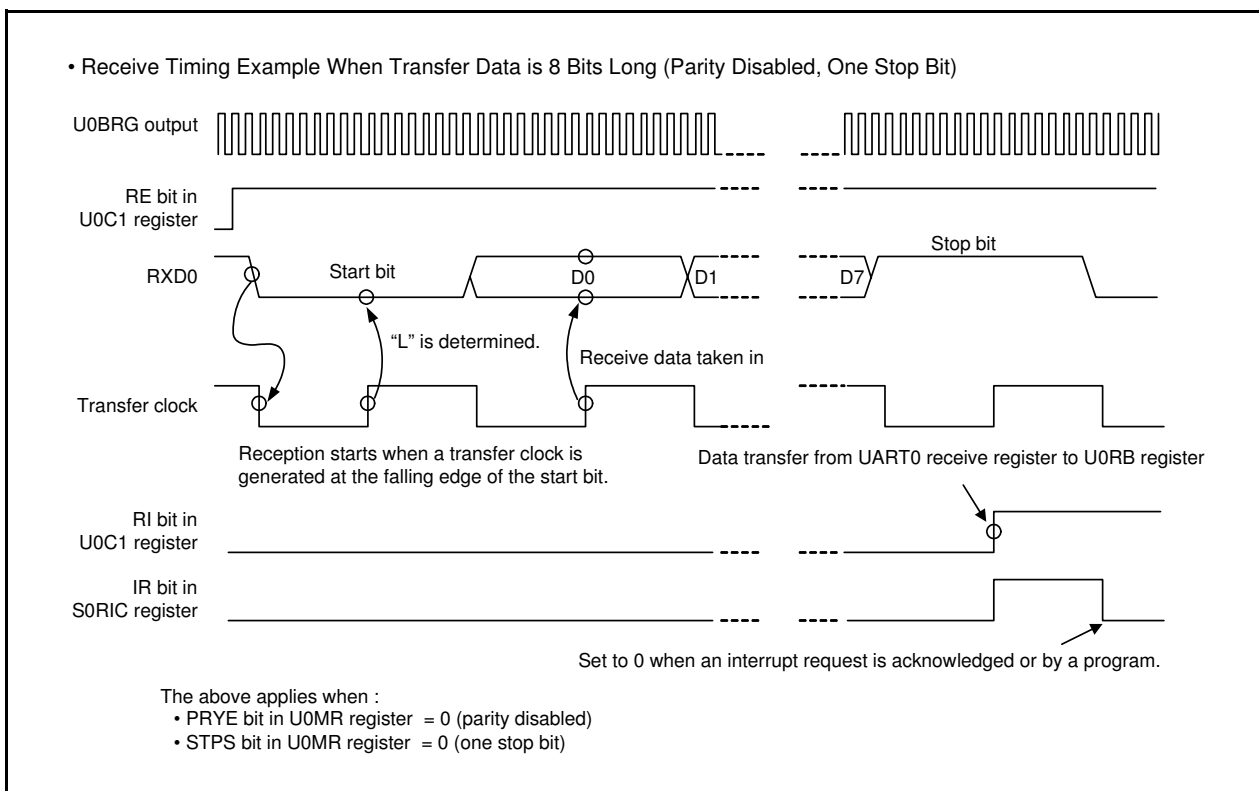


Figure 20.7 Receive Timing in UART Mode

### 20.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U0BRG register and divided by 16.

|  |  |
|--|--|
| UART mode  |  |
| • Internal clock selected  |  |
| $\text{Setting value in U0BRG register} = \frac{f_j}{\text{Bit Rate} \times 16} - 1$   |  |
| f <sub>j</sub> : Count source frequency of U0BRG register (f <sub>1</sub> , f <sub>8</sub> , f <sub>32</sub> , or f <sub>C</sub> ) |  |
| • External clock selected  |  |
| $\text{Setting value in U0BRG register} = \frac{f_{\text{EXT}}}{\text{Bit Rate} \times 16} - 1$                                    |  |
| f <sub>EXT</sub> : Count source frequency of U0BRG register (external clock)   |  |

**Figure 20.8 Formula for Calculating Setting Value in U0BRG Register**

**Table 20.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**

| Bit Rate (bps) | U0BRG Count Source | System Clock = 20 MHz |                   |                   | System Clock = 18.432 MHz <sup>(1)</sup> |                   |                   | System Clock = 8 MHz |                   |                   |
|----------------|--------------------|-----------------------|-------------------|-------------------|--|-------------------|-------------------|----------------------|-------------------|-------------------|
|                |                    | U0BRG Setting Value   | Actual Time (bps) | Setting Error (%) | U0BRG Setting Value                      | Actual Time (bps) | Setting Error (%) | U0BRG Setting Value  | Actual Time (bps) | Setting Error (%) |
| 1200           | f8                 | 129 (81h)             | 1201.92           | 0.16              | 119 (77h)                                | 1200.00           | 0.00              | 51 (33h)             | 1201.92           | 0.16              |
| 2400           | f8                 | 64 (40h)              | 2403.85           | 0.16              | 59 (3Bh)                                 | 2400.00           | 0.00              | 25 (19h)             | 2403.85           | 0.16              |
| 4800           | f8                 | 32 (20h)              | 4734.85           | -1.36             | 29 (1Dh)                                 | 4800.00           | 0.00              | 12 (0Ch)             | 4807.69           | 0.16              |
| 9600           | f1                 | 129 (81h)             | 9615.38           | 0.16              | 119 (77h)                                | 9600.00           | 0.00              | 51 (33h)             | 9615.38           | 0.16              |
| 14400          | f1                 | 86 (56h)              | 14367.82          | -0.22             | 79 (4Fh)                                 | 14400.00          | 0.00              | 34 (22h)             | 14285.71          | -0.79             |
| 19200          | f1                 | 64 (40h)              | 19230.77          | 0.16              | 59 (3Bh)                                 | 19200.00          | 0.00              | 25 (19h)             | 19230.77          | 0.16              |
| 28800          | f1                 | 42 (2Ah)              | 29069.77          | 0.94              | 39 (27h)                                 | 28800.00          | 0.00              | 16 (10h)             | 29411.76          | 2.12              |
| 38400          | f1                 | 32 (20h)              | 37878.79          | -1.36             | 29 (1Dh)                                 | 38400.00          | 0.00              | 12 (0Ch)             | 38461.54          | 0.16              |
| 57600          | f1                 | 21 (15h)              | 56818.18          | -1.36             | 19 (13h)                                 | 57600.00          | 0.00              | 8 (08h)              | 55555.56          | -3.55             |
| 115200         | f1                 | 10 (0Ah)              | 113636.36         | -1.36             | 9 (09h)                                  | 115200.00         | 0.00              | –                    | –                 | –                 |

Note:

- For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register. This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **26. Electrical Characteristics**.

### 20.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

- (1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
- (4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

## 20.5 Notes on Serial Interface (UART0)

- When reading data from the UORB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.

When the high-order byte of the UORB register is read, bits PER and FER in the UORB register and the RI bit in the UOC1 register are set to 0.

To check receive errors, read the UORB register and then use the read data.

Program example to read the receive buffer register:

```
MOV.W    00A6H,R0    ; Read the UORB register
```

- When writing data to the UOTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

Program example to write to the transmit buffer register:

```
MOV.B    #XXH,00A3H  ; Write to the high-order byte of the UOTB register
```

```
MOV.B    #XXH,00A2H  ; Write to the low-order byte of the UOTB register
```

## 21. Serial Interface (UART2)

The serial interface consists of two channels, UART0 and UART2. This chapter describes the UART2.

### 21.1 Overview

UART2 has a dedicated timer to generate a transfer clock.

Figure 21.1 shows a UART2 Block Diagram. Figure 21.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 21.1 lists the Pin Configuration of UART2.

UART2 has the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I<sup>2</sup>C mode)
- Multiprocessor communication function

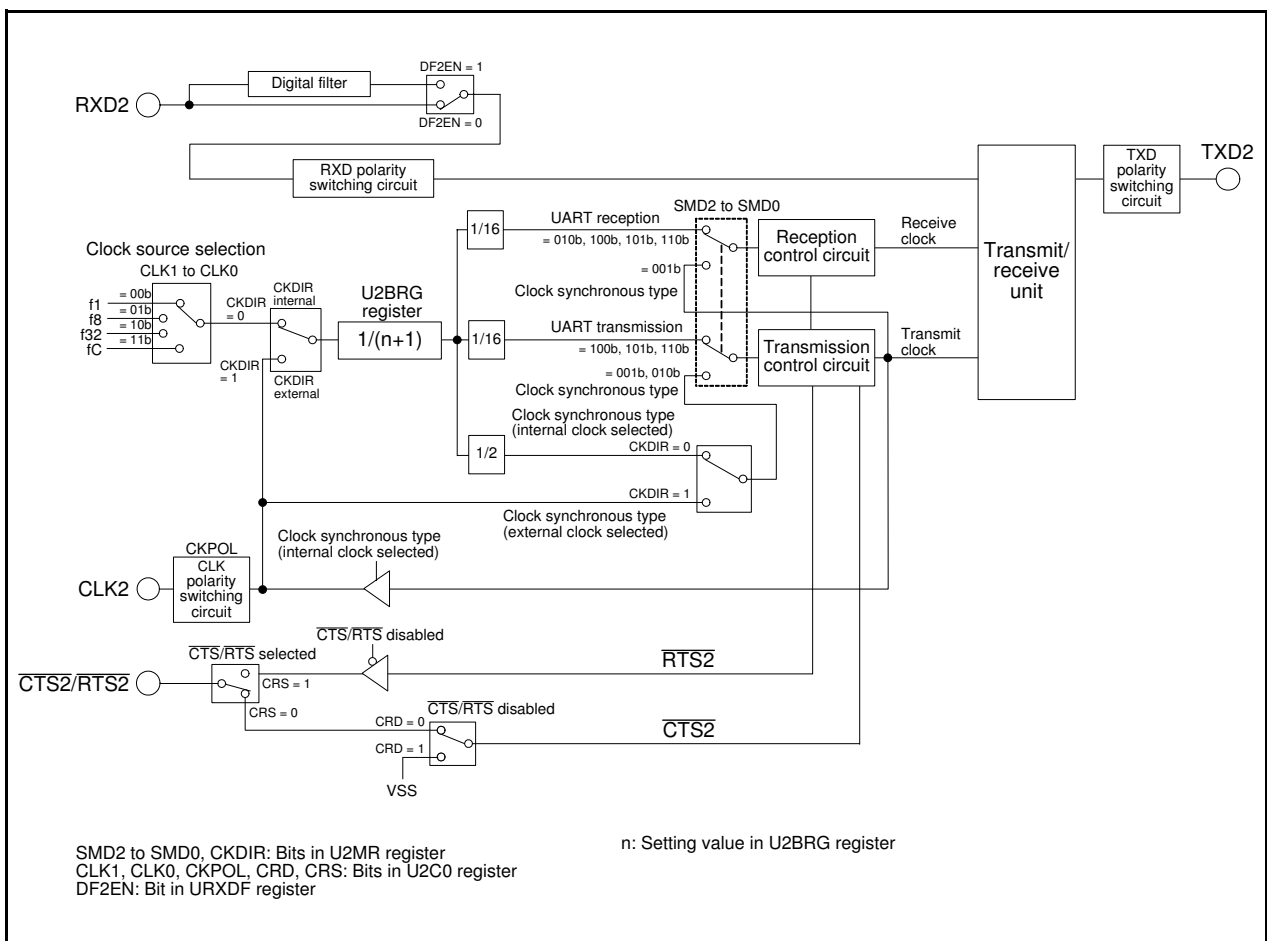


Figure 21.1 UART2 Block Diagram

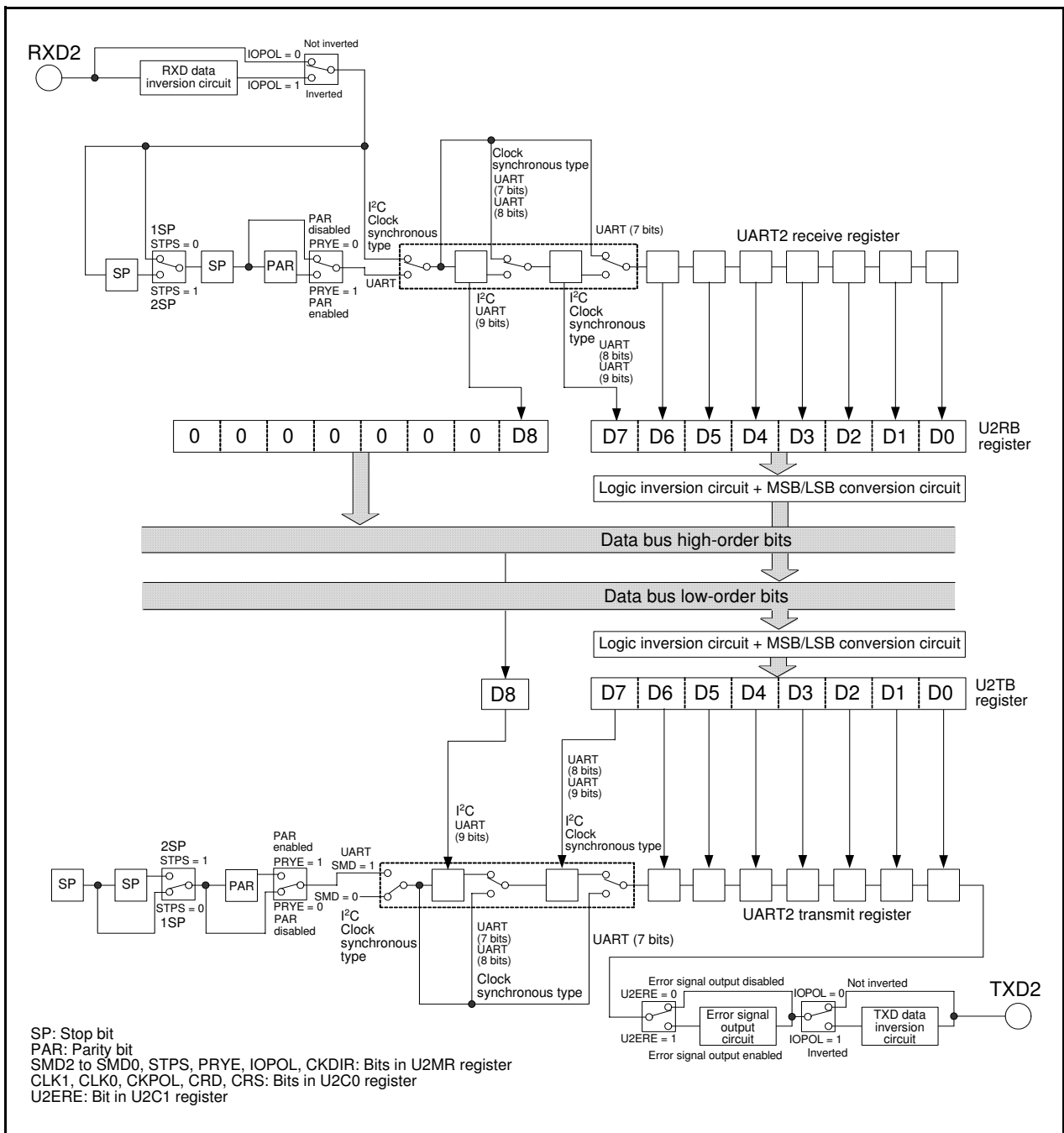


Figure 21.2 Block Diagram of UART2 Transmit/Receive Unit

Table 21.1 Pin Configuration of UART2

| Pin Name | Assigned Pin        | I/O    | Function                        |
|----------|---------------------|--------|---------------------------------|
| TXD2     | P3_4 or P3_7        | Output | Serial data output              |
| RXD2     | P3_4, P3_7, or P4_5 | Input  | Serial data input               |
| CLK2     | P3_5                | I/O    | Transfer clock I/O              |
| CTS2     | P3_3                | Input  | Transmit control input          |
| RTS2     | P3_3                | Output | Receive control input           |
| SCL2     | P3_4, P3_7, or P4_5 | I/O    | I <sup>2</sup> C mode clock I/O |
| SDA2     | P3_4 or P3_7        | I/O    | I <sup>2</sup> C mode data I/O  |

## 21.2 Registers

### 21.2.1 UART2 Transmit/Receive Mode Register (U2MR)

Address 00A8h

|             |       |      |     |      |       |      |      |      |
|-------------|-------|------|-----|------|-------|------|------|------|
| Bit         | b7    | b6   | b5  | b4   | b3    | b2   | b1   | b0   |
| Symbol      | IOPOL | PRYE | PRY | STPS | CKDIR | SMD2 | SMD1 | SMD0 |
| After Reset | 0     | 0    | 0   | 0    | 0     | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                           | Function   | R/W |
|-----|--------|------------------------------------|--|-----|
| b0  | SMD0   | Serial I/O mode select bit         | b2 b1 b0<br>0 0 0: Serial interface disabled<br>0 0 1: Clock synchronous serial I/O mode<br>0 1 0: I <sup>2</sup> C mode<br>1 0 0: UART mode, transfer data 7 bits long<br>1 0 1: UART mode, transfer data 8 bits long<br>1 1 0: UART mode, transfer data 9 bits long<br>Other than above: Do not set. | R/W |
| b1  | SMD1   |                                    |  | R/W |
| b2  | SMD2   |                                    |  | R/W |
| b3  | CKDIR  | Internal/external clock select bit | 0: Internal clock<br>1: External clock   | R/W |
| b4  | STPS   | Stop bit length select bit         | 0: One stop bit<br>1: Two stop bits  | R/W |
| b5  | PRY    | Odd/even parity select bit         | Enabled when PRYE = 1<br>0: Odd parity<br>1: Even parity   | R/W |
| b6  | PRYE   | Parity enable bit                  | 0: Parity disabled<br>1: Parity enabled  | R/W |
| b7  | IOPOL  | TXD, RXD I/O polarity switch bit   | 0: Not inverted<br>1: Inverted   | R/W |

### 21.2.2 UART2 Bit Rate Register (U2BRG)

Address 00A9h

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit      | Function  | Setting Range | R/W |
|----------|---|---------------|-----|
| b7 to b0 | If the setting value is n, U2BRG divides the count source by n+1. | 00h to FFh    | W   |

Write to the U2BRG register while transmission and reception stop.

Use the MOV instruction to write to this register.

Set bits CLK1 to CLK0 in the U2C0 register before writing to the U2BRG register.

### 21.2.3 UART2 Transmit Buffer Register (U2TB)

Address 00ABh to 00AAh

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

|             |     |     |     |     |     |     |    |      |
|-------------|-----|-----|-----|-----|-----|-----|----|------|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8   |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | MPTB |
| After Reset | X   | X   | X   | X   | X   | X   | X  | X    |

| Bit | Symbol | Function   | R/W |
|-----|--------|--|-----|
| b0  | —      | Transmit data (D7 to D0)   | W   |
| b1  | —      |  |     |
| b2  | —      |  |     |
| b3  | —      |  |     |
| b4  | —      |  |     |
| b5  | —      |  |     |
| b6  | —      |  |     |
| b7  | —      |  |     |
| b8  | MPTB   | Transmit data (D8) <sup>(1)</sup><br>[When the multiprocessor communication function is not used]<br>Transmit data (D8)<br>[When the multiprocessor communication function is used]<br>• To transfer an ID, set the MPTB bit to 1.<br>• To transfer data, set the MPTB bit to 0. | W   |
| b9  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0.  | —   |
| b10 | —      |  |     |
| b11 | —      |  |     |
| b12 | —      |  |     |
| b13 | —      |  |     |
| b14 | —      |  |     |
| b15 | —      |  |     |

Note:

1. Set bits b0 to b7 after setting the MPTB bit.



### 21.2.4 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 00ACh

|             |       |       |     |     |       |     |      |      |
|-------------|-------|-------|-----|-----|-------|-----|------|------|
| Bit         | b7    | b6    | b5  | b4  | b3    | b2  | b1   | b0   |
| Symbol      | UFORM | CKPOL | NCH | CRD | TXEPT | CRS | CLK1 | CLK0 |
| After Reset | 0     | 0     | 0   | 0   | 1     | 0   | 0    | 0    |

| Bit | Symbol | Bit Name                          | Function   | R/W |
|-----|--------|-----------------------------------|--|-----|
| b0  | CLK0   | U2BRG count source select bit (1) | b1 b0<br>0 0: f1 selected<br>0 1: f8 selected<br>1 0: f32 selected<br>1 1: fC selected   | R/W |
| b1  | CLK1   |                                   |  | R/W |
| b2  | CRS    | CTS/RTS function select bit       | Enabled when CRD = 0<br>0: CTS function selected<br>1: RTS function selected   | R/W |
| b3  | TXEPT  | Transmit register empty flag      | 0: Data present in the transmit register (transmission in progress)<br>1: No data in the transmit register (transmission completed)  | R   |
| b4  | CRD    | CTS/RTS disable bit               | 0: CTS/RTS function enabled<br>1: CTS/RTS function disabled  | R/W |
| b5  | NCH    | Data output select bit            | 0: Pins TXD2/SDA2, SCL2 set to CMOS output<br>1: Pins TXD2/SDA2, SCL2 set to N-channel open-drain output   | R/W |
| b6  | CKPOL  | CLK polarity select bit           | 0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock<br>1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock | R/W |
| b7  | UFORM  | Transfer format select bit (2)    | 0: LSB first<br>1: MSB first   | R/W |

Notes:

- If bits CLK1 to CLK0 are switched, set the U2BRG register again.
- The UFORM bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), or set to 101b (UART mode, transfer data 8 bits long).  
Set the UFORM bit to 1 when bits SMD2 to SMD0 are set to 010b (I<sup>2</sup>C mode), and to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, transfer data 7 bits long) or 110b (UART mode, transfer data 9 bits long).

### 21.2.5 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 00ADh

|             |       |       |       |       |    |    |    |    |
|-------------|-------|-------|-------|-------|----|----|----|----|
| Bit         | b7    | b6    | b5    | b4    | b3 | b2 | b1 | b0 |
| Symbol      | U2ERE | U2LCH | U2RRM | U2IRS | RI | RE | TI | TE |
| After Reset | 0     | 0     | 0     | 0     | 0  | 0  | 1  | 0  |

| Bit | Symbol | Bit Name                                   | Function   | R/W |
|-----|--------|--|--|-----|
| b0  | TE     | Transmit enable bit                        | 0: Transmission disabled<br>1: Transmission enabled                        | R/W |
| b1  | TI     | Transmit buffer empty flag                 | 0: Data present in the U2TB register<br>1: No data in the U2TB register    | R   |
| b2  | RE     | Receive enable bit                         | 0: Reception disabled<br>1: Reception enabled                              | R/W |
| b3  | RI     | Receive complete flag                      | 0: No data in the U2RB register<br>1: Data present in the U2RB register    | R   |
| b4  | U2IRS  | UART2 transmit interrupt source select bit | 0: Transmit buffer empty (TI = 1)<br>1: Transmission completed (TXEPT = 1) | R/W |
| b5  | U2RRM  | UART2 continuous receive mode enable bit   | 0: Continuous receive mode disabled<br>1: Continuous receive mode enabled  | R/W |
| b6  | U2LCH  | Data logic select bit <sup>(1)</sup>       | 0: Not inverted<br>1: Inverted   | R/W |
| b7  | U2ERE  | Error signal output enable bit             | 0: Output disabled<br>1: Output enabled                                    | R/W |

Note:

- The U2LCH bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set the U2LCH bit to 0 when bits SMD2 to SMD0 are set to 010b (I<sup>2</sup>C mode) or 110b (UART mode, transfer data 9 bits long).

### 21.2.6 UART2 Receive Buffer Register (U2RB)

Address 00AFh to 00AEh

| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-------------|----|----|----|----|----|----|----|----|
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8   |
|-------------|-----|-----|-----|-----|-----|-----|----|------|
| Symbol      | SUM | PER | FER | OER | —   | —   | —  | MPRB |
| After Reset | X   | X   | X   | X   | X   | X   | X  | X    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | —      | —   | Receive data (D7 to D0)   | R   |
| b1  | —      |   |   |     |
| b2  | —      |   |   |     |
| b3  | —      |   |   |     |
| b4  | —      |   |   |     |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      |   |   |     |
| b8  | MPRB   | —   | Receive data (D8) <sup>(1)</sup><br>[When the multiprocessor communication function is not used]<br>Receive data (D8)<br>[When the multiprocessor communication function is used]<br>• When the MPRB bit is set to 0, received D0 to D7 are data fields.<br>• When the MPRB bit is set to 1, received D0 to D7 are ID fields. | R   |
| b9  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |   | —   |
| b10 | —      |   |   | —   |
| b11 | —      | Reserved bit  | Set to 0.   | R/W |
| b12 | OER    | Overrun error flag <sup>(1)</sup>   | 0: No overrun error<br>1: Overrun error   | R   |
| b13 | FER    | Framing error flag <sup>(1, 2)</sup>  | 0: No framing error<br>1: Framing error   | R   |
| b14 | PER    | Parity error flag <sup>(1, 2)</sup>   | 0: No parity error<br>1: Parity error   | R   |
| b15 | SUM    | Error sum flag <sup>(1, 2)</sup>  | 0: No error<br>1: Error   | R   |

## Notes:

- When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 by reading the lower byte of the U2RB register.  
When setting bits SMD2 to SMD0 in the U2MR register to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- These error flags are disabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or to 010b (I<sup>2</sup>C mode). When read, the content is undefined.

### 21.2.7 UART2 Digital Filter Function Select Register (URXDF)

Address 00B0h

| Bit         | b7 | b6 | b5 | b4 | b3 | b2    | b1 | b0 |
|-------------|----|----|----|----|----|-------|----|----|
| Symbol      | —  | —  | —  | —  | —  | DF2EN | —  | —  |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0     | 0  | 0  |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b1  | —      |   |   |     |
| b2  | DF2EN  | RXD2 digital filter enable bit <sup>(1)</sup>                             | 0: RXD2 digital filter disabled<br>1: RXD2 digital filter enabled | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | —      |   |   |     |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      |   |   |     |

Note:

- The RXD2 digital filter can be used only in clock asynchronous serial I/O (UART) mode. When bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or 010b (I<sup>2</sup>C mode), set the DF2EN bit to 0 (RXD2 digital filter disabled).

### 21.2.8 UART2 Special Mode Register 5 (U2SMR5)

Address 00BBh

| Bit         | b7 | b6 | b5 | b4   | b3 | b2 | b1 | b0 |
|-------------|----|----|----|------|----|----|----|----|
| Symbol      | —  | —  | —  | MPIE | —  | —  | —  | MP |
| After Reset | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | MP     | Multiprocessor communication enable bit                                   | 0: Multiprocessor communication disabled<br>1: Multiprocessor communication enabled <sup>(1)</sup>  | R/W |
| b1  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b2  | —      |   |   |     |
| b3  | —      |   |   |     |
| b4  | MPIE   | Multiprocessor communication control bit                                  | This bit is enabled when the MP bit is set to 1 (multiprocessor communication enabled).<br>When the MPIE bit is set to 1, the following will result: <ul style="list-style-type: none"> <li>Receive data in which the multiprocessor bit is 0 is ignored. Setting of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 is disabled.</li> <li>On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and receive operation other than multiprocessor communication is performed.</li> </ul> | R/W |
| b5  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b6  | —      |   |   |     |
| b7  | —      | Reserved bit  | Set to 0.   | R/W |

Note:

- When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled. If bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the MP bit to 0 (multiprocessor communication disabled).

### 21.2.9 UART2 Special Mode Register 4 (U2SMR4)

Address 00BCh

| Bit         | b7   | b6    | b5   | b4   | b3      | b2     | b1      | b0     |
|-------------|------|-------|------|------|---------|--------|---------|--------|
| Symbol      | SWC9 | SCLHI | ACKC | ACKD | STSPSEL | STPREQ | RSTAREQ | STAREQ |
| After Reset | 0    | 0     | 0    | 0    | 0       | 0      | 0       | 0      |

| Bit | Symbol  | Bit Name                                      | Function   | R/W |
|-----|---------|---|--|-----|
| b0  | STAREQ  | Start condition generate bit <sup>(1)</sup>   | 0: Clear<br>1: Start   | R/W |
| b1  | RSTAREQ | Restart condition generate bit <sup>(1)</sup> | 0: Clear<br>1: Start   | R/W |
| b2  | STPREQ  | Stop condition generate bit <sup>(1)</sup>    | 0: Clear<br>1: Start   | R/W |
| b3  | STSPSEL | SCL, SDA output select bit                    | 0: Start and stop conditions not output<br>1: Start and stop conditions output | R/W |
| b4  | ACKD    | ACK data bit                                  | 0: ACK<br>1: NACK  | R/W |
| b5  | ACKC    | ACK data output enable bit                    | 0: Serial interface data output<br>1: ACK data output                          | R/W |
| b6  | SCLHI   | SCL output stop enable bit                    | 0: Disabled<br>1: Enabled  | R/W |
| b7  | SWC9    | SCL wait bit 3                                | 0: SCL "L" hold disabled<br>1: SCL "L" hold enabled                            | R/W |

Note:

1. This bit is set to 0 when each condition is generated.

### 21.2.10 UART2 Special Mode Register 3 (U2SMR3)

Address 00BDh

| Bit         | b7  | b6  | b5  | b4 | b3   | b2 | b1   | b0 |
|-------------|-----|-----|-----|----|------|----|------|----|
| Symbol      | DL2 | DL1 | DL0 | —  | NODC | —  | CKPH | —  |
| After Reset | 0   | 0   | 0   | X  | 0    | X  | 0    | X  |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |  | —   |
| b1  | CKPH   | Clock phase set bit   | 0: No clock delay<br>1: With clock delay   | R/W |
| b2  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |  | —   |
| b3  | NODC   | Clock output select bit   | 0: CLK2 set to CMOS output<br>1: CLK2 set to N-channel open-drain output   | R/W |
| b4  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |  | —   |
| b5  | DL0    | SDA2 digital delay setup bit <sup>(1, 2)</sup>                                    | <sup>b7 b6 b5</sup><br>0 0 0: No delay<br>0 0 1: 1 to 2 cycle(s) of U2BRG count source<br>0 1 0: 2 to 3 cycles of U2BRG count source<br>0 1 1: 3 to 4 cycles of U2BRG count source<br>1 0 0: 4 to 5 cycles of U2BRG count source<br>1 0 1: 5 to 6 cycles of U2BRG count source<br>1 1 0: 6 to 7 cycles of U2BRG count source<br>1 1 1: 7 to 8 cycles of U2BRG count source | R/W |
| b6  | DL1    |   |  | R/W |
| b7  | DL2    |   |  | R/W |

Notes:

1. Bits DL2 to DL0 are used to generate a delay in SDA2 output digitally in I<sup>2</sup>C mode. In other than I<sup>2</sup>C mode, set these bits to 000b (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. When an external clock is used, the amount of delay increases by about 100 ns.

### 21.2.11 UART2 Special Mode Register 2 (U2SMR2)

Address 00BEh

|             |    |      |      |      |    |     |     |       |
|-------------|----|------|------|------|----|-----|-----|-------|
| Bit         | b7 | b6   | b5   | b4   | b3 | b2  | b1  | b0    |
| Symbol      | —  | SDHI | SWC2 | STAC | —  | SWC | CSC | IICM2 |
| After Reset | X  | 0    | 0    | 0    | 0  | 0   | 0   | 0     |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | IICM2  | I <sup>2</sup> C mode select bit 2  | Refer to <b>Table 21.12 I<sup>2</sup>C Mode Functions.</b> | R/W |
| b1  | CSC    | Clock synchronization bit   | 0: Disabled<br>1: Enabled                                  | R/W |
| b2  | SWC    | SCL wait output bit   | 0: Disabled<br>1: Enabled                                  | R/W |
| b3  | —      | Reserved bit  | Set to 0.  | R/W |
| b4  | STAC   | UART2 initialization bit  | 0: Disabled<br>1: Enabled                                  | R/W |
| b5  | SWC2   | SCL wait output bit 2   | 0: Transfer clock<br>1: "L" output                         | R/W |
| b6  | SDHI   | SDA output disable bit  | 0: Enabled<br>1: Disabled (high-impedance)                 | R/W |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |  | —   |

### 21.2.12 UART2 Special Mode Register (U2SMR)

Address 00BFh

|             |    |    |    |    |    |     |    |      |
|-------------|----|----|----|----|----|-----|----|------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2  | b1 | b0   |
| Symbol      | —  | —  | —  | —  | —  | BBS | —  | IICM |
| After Reset | X  | 0  | 0  | 0  | 0  | 0   | 0  | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | IICM   | I <sup>2</sup> C mode select bit  | 0: Other than I <sup>2</sup> C mode<br>1: I <sup>2</sup> C mode  | R/W |
| b1  | —      | Reserved bit  | Set to 0.  | R/W |
| b2  | BBS    | Bus busy flag <sup>(1)</sup>  | 0: Stop condition detected<br>1: Start condition detected (busy) | R/W |
| b3  | —      | Reserved bits   | Set to 0.  | R/W |
| b4  | —      |   |  |     |
| b5  | —      |   |  |     |
| b6  | —      |   |  |     |
| b7  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is undefined. |  | —   |

Note:

1. The BBS bit is set to 0 by writing 0 by a program (Writing 1 has no effect).

### 21.2.13 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

| Bit         | b7 | b6 | b5       | b4       | b3 | b2 | b1       | b0       |
|-------------|----|----|----------|----------|----|----|----------|----------|
| Symbol      | —  | —  | RXD2SEL1 | RXD2SEL0 | —  | —  | TXD2SEL1 | TXD2SEL0 |
| After Reset | 0  | 0  | 0        | 0        | 0  | 0  | 0        | 0        |

| Bit | Symbol   | Bit Name  | Function  | R/W |
|-----|----------|---|---|-----|
| b0  | TXD2SEL0 | TXD2/SDA2 pin select bit  | <sup>b1 b0</sup><br>0 0: TXD2/SDA2 pin not used<br>0 1: P3_7 assigned<br>1 0: P3_4 assigned<br>1 1: Do not set.   | R/W |
| b1  | TXD2SEL1 |   |   | R/W |
| b2  | —        | Reserved bit  | Set to 0.   | R/W |
| b3  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | RXD2SEL0 | RXD2/SCL2 pin select bit  | <sup>b5 b4</sup><br>0 0: RXD2/SCL2 pin not used<br>0 1: P3_4 assigned<br>1 0: P3_7 assigned<br>1 1: P4_5 assigned | R/W |
| b5  | RXD2SEL1 |   |   | R/W |
| b6  | —        | Reserved bit  | Set to 0.   | R/W |
| b7  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.

Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

### 21.2.14 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

| Bit         | b7 | b6 | b5 | b4       | b3 | b2 | b1 | b0       |
|-------------|----|----|----|----------|----|----|----|----------|
| Symbol      | —  | —  | —  | CTS2SEL0 | —  | —  | —  | CLK2SEL0 |
| After Reset | 0  | 0  | 0  | 0        | 0  | 0  | 0  | 0        |

| Bit | Symbol   | Bit Name  | Function                                      | R/W |
|-----|----------|---|---|-----|
| b0  | CLK2SEL0 | CLK2 pin select bit   | 0: CLK2 pin not used<br>1: P3_5 assigned      | R/W |
| b1  | —        | Reserved bit  | Set to 0.                                     | R/W |
| b2  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b3  | —        |   |   |     |
| b4  | CTS2SEL0 | CTS2/RTS2 pin select bit  | 0: CTS2/RTS2 pin not used<br>1: P3_3 assigned | R/W |
| b5  | —        | Reserved bit  | Set to 0.                                     | R/W |
| b6  | —        | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b7  | —        |   |   |     |

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.

Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

### 21.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.

Table 21.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 21.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

**Table 21.2 Clock Synchronous Serial I/O Mode Specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Transfer data format                | Transfer data length: 8 bits   |
| Transfer clock                      | <ul style="list-style-type: none"> <li>The CKDIR bit in the U2MR register is set to 0 (internal clock): <math>f_j / (2(n+1))</math><br/> <math>f_j = f_1, f_8, f_{32}, f_C</math> n = setting value in the U2BRG register: 00h to FFh</li> <li>The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin</li> </ul>  |
| Transmit/receive control            | Selectable from the $\overline{CTS}$ function, $\overline{RTS}$ function, or $\overline{CTS}/\overline{RTS}$ function disabled.  |
| Transmit start conditions           | To start transmission, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>The TE bit in the U2C1 register is set to 1 (transmission enabled)</li> <li>The TI bit in the U2C1 register is set to 0 (data present in the U2TB register)</li> <li>If the <math>\overline{CTS}</math> function is selected, input to the CTS2 pin = "L".</li> </ul>   |
| Receive start conditions            | To start reception, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>The RE bit in the U2C1 register is set to 1 (reception enabled).</li> <li>The TE bit in the U2C1 register is set to 1 (transmission enabled).</li> <li>The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).</li> </ul>   |
| Interrupt request generation timing | For transmission, one of the following conditions can be selected. <ul style="list-style-type: none"> <li>The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty):<br/>When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission).</li> <li>The U2IRS bit is set to 1 (transmission completed):<br/>When data transmission from the UART2 transmit register is completed.</li> </ul> For reception <ul style="list-style-type: none"> <li>When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).</li> </ul> |
| Error detection                     | Overrun error <sup>(2)</sup><br>This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.   |
| Selectable functions                | <ul style="list-style-type: none"> <li>CLK polarity selection<br/>Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock.</li> <li>LSB first, MSB first selection<br/>Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected.</li> <li>Continuous receive mode selection<br/>Reception is enabled immediately by reading the U2RB register.</li> <li>Serial data logic switching<br/>This function inverts the logic value of the transmit/receive data.</li> </ul>   |

Notes:

- When an external clock is selected, the requirements must be met in either of the following states:
  - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
  - The external clock is held low when the CKPOL bit in the U2C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
- If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register does not change to 1 (interrupt requested).



**Table 21.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode**

| Register | Bit          | Function   |
|----------|--------------|--|
| U2TB (1) | b0 to b7     | Set transmit data.   |
| U2RB (1) | b0 to b7     | Receive data can be read.  |
|          | OER          | Overrun error flag   |
| U2BRG    | b0 to b7     | Set a bit rate.  |
| U2MR (1) | SMD2 to SMD0 | Set to 001b.   |
|          | CKDIR        | Select the internal clock or external clock.                                       |
|          | IOPOL        | Set to 0.  |
| U2C0     | CLK1, CLK0   | Select the count source for the U2BRG register.                                    |
|          | CRS          | Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions. |
|          | TXEPT        | Transmit register empty flag   |
|          | CRD          | Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function. |
|          | NCH          | Select TXD2 pin output mode.   |
|          | CKPOL        | Select the transfer clock polarity.  |
|          | UFORM        | Select LSB first or MSB first.   |
| U2C1     | TE           | Set to 1 to enable transmission/reception.   |
|          | TI           | Transmit buffer empty flag   |
|          | RE           | Set to 1 to enable reception.  |
|          | RI           | Receive complete flag  |
|          | U2IRS        | Select the source of UART2 transmit interrupt.                                     |
|          | U2RRM        | Set to 1 to use continuous receive mode.   |
|          | U2LCH        | Set to 1 to use inverted data logic.   |
|          | U2ERE        | Set to 0.  |
| U2SMR    | b0 to b7     | Set to 0.  |
| U2SMR2   | b0 to b7     | Set to 0.  |
| U2SMR3   | b0 to b2     | Set to 0.  |
|          | NODC         | Select clock output mode.  |
|          | b4 to b7     | Set to 0.  |
| U2SMR4   | b0 to b7     | Set to 0.  |
| URXDF    | DF2EN        | Set to 0.  |
| U2SMR5   | MP           | Set to 0.  |

Note:

1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 21.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).

Note that for a period from when UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs a “H” level. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)

Figure 21.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

**Table 21.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)**

| Pin Name                      | Function              | Selection Method   |
|-------------------------------|-----------------------|--|
| TXD2<br>(P3_4 or P3_7)        | Serial data output    | <ul style="list-style-type: none"> <li>• TXD2 (P3_4)<br/>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P3_4)</li> <li>• TXD2 (P3_7)<br/>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P3_7)</li> <li>• For reception only:<br/>P3_4 and P3_7 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.</li> </ul>   |
| RXD2<br>(P3_4, P3_7, or P4_5) | Serial data input     | <ul style="list-style-type: none"> <li>• RXD2 (P3_4)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P3_4)<br/>PD3_4 bit in PD3 register = 0</li> <li>• RXD2 (P3_7)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P3_7)<br/>PD3_7 bit in PD3 register = 0</li> <li>• RXD2 (P4_5)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P4_5)<br/>PD4_5 bit in PD4 register = 0</li> <li>• For transmission only:<br/>P3_4, P3_7, and P4_5 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.</li> </ul> |
| CLK2 (P3_5)                   | Transfer clock output | CLK2SEL0 bit in U2SR1 register = 1<br>CKDIR bit in U2MR register = 0   |
|                               | Transfer clock input  | CLK2SEL0 bit in U2SR1 register = 1<br>CKDIR bit in U2MR register = 1<br>PD3_5 bit in PD3 register = 0  |
| CTS2/RTS2<br>(P3_3)           | CTS input             | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 0<br>PD3_3 bit in PD3 register = 0  |
|                               | RTS output            | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 1   |
|                               | I/O port              | CTS2SEL0 bit in U2SR1 register = 0   |

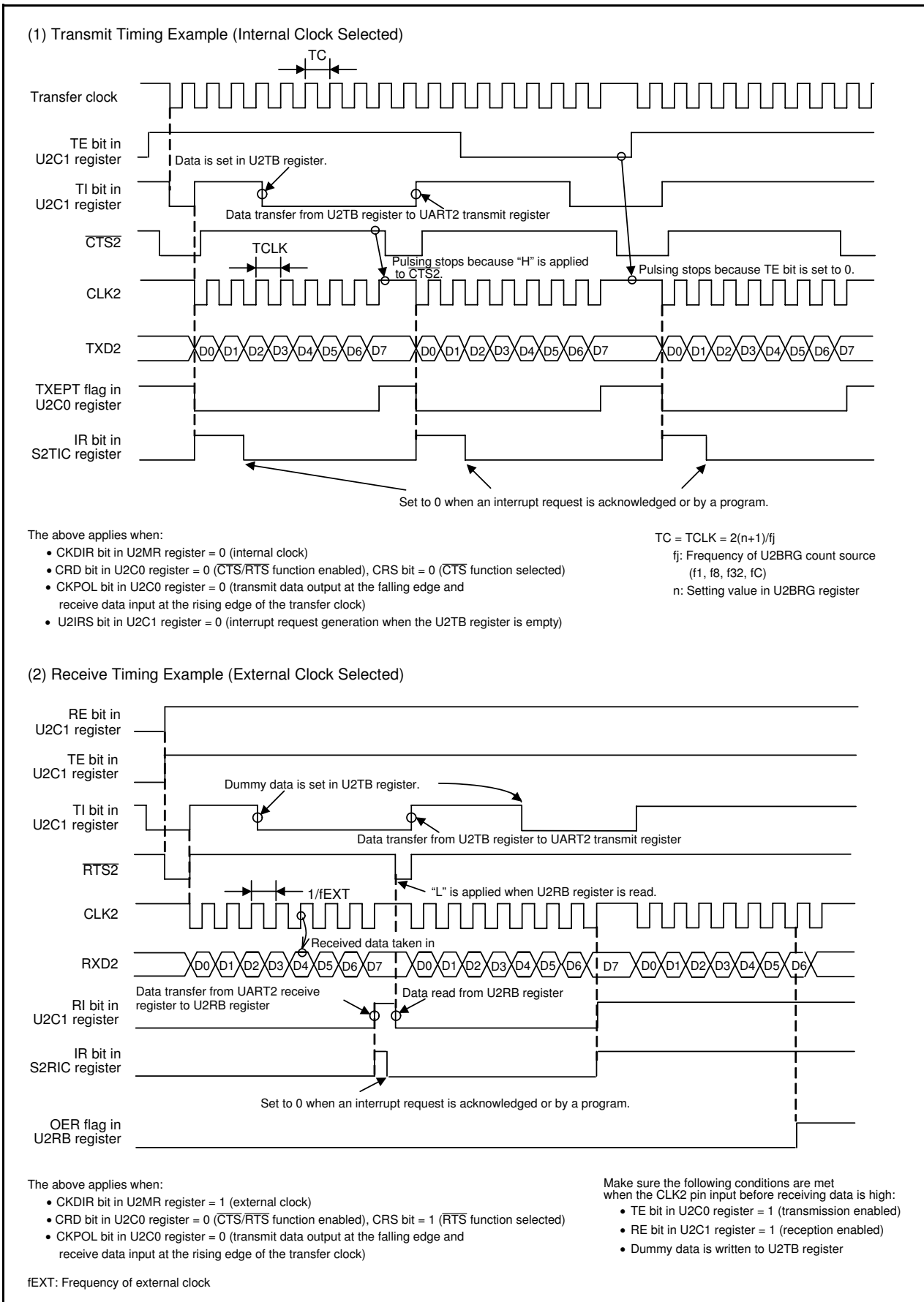


Figure 21.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

### 21.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

- (1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
- (4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

### 21.3.2 CLK Polarity Select Function

Use the CKPOL bit in the U2C0 register to select the transfer clock polarity. Figure 21.4 shows the Transfer Clock Polarity.

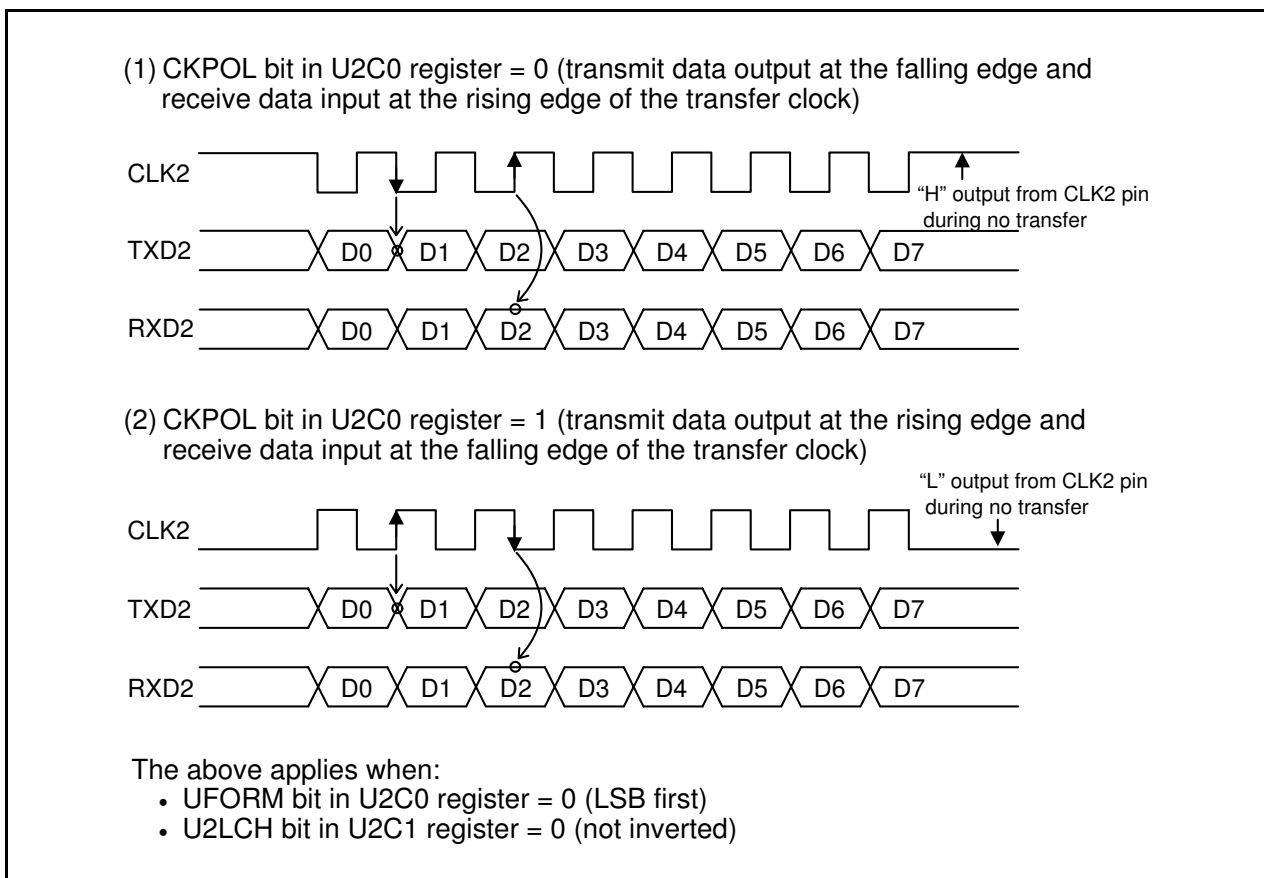


Figure 21.4 Transfer Clock Polarity

### 21.3.3 LSB First/MSB First Select Function

Use the UFORM bit in the U2C0 register to select the transfer format. Figure 21.5 shows the Transfer Format.

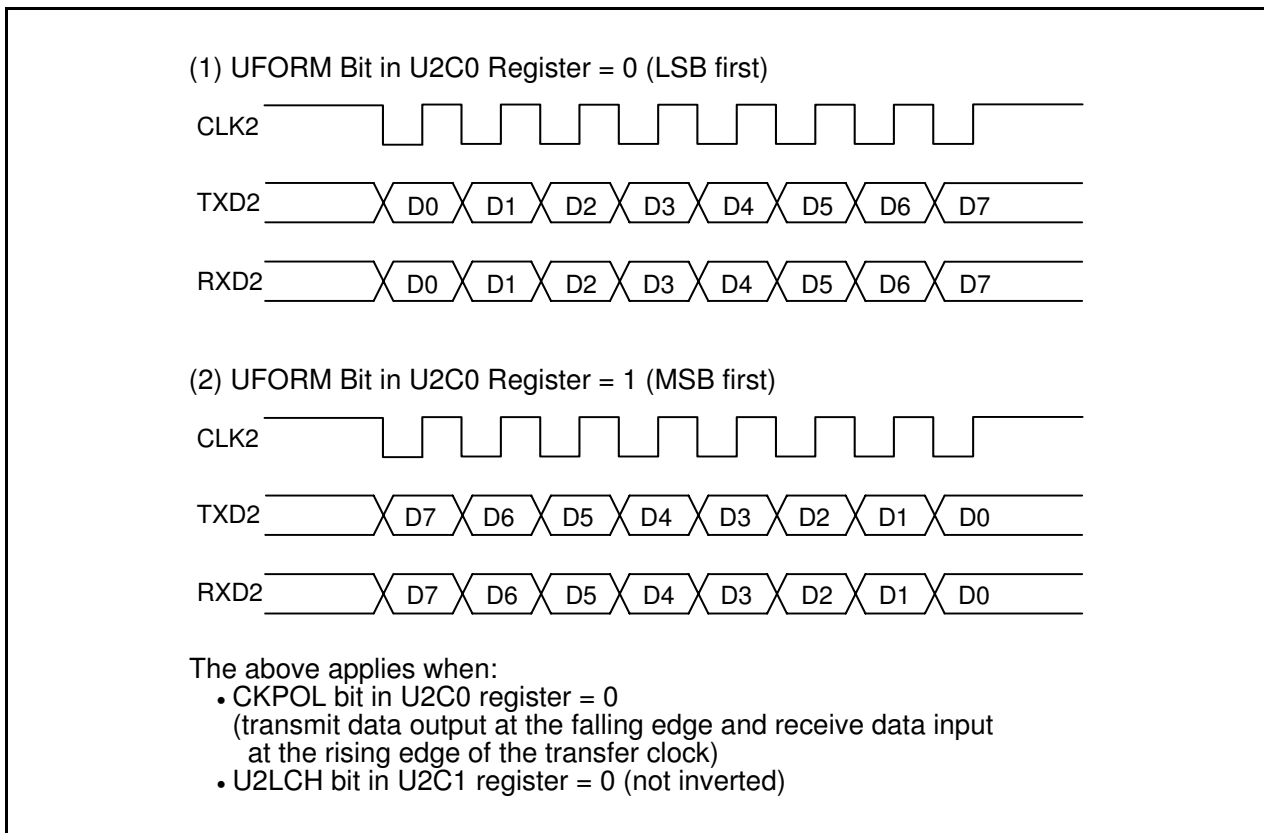


Figure 21.5 Transfer Format

### 21.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data present in the U2TB register) by reading the U2RB register. If the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

### 21.3.5 Serial Data Logic Switching Function

If the U2LCH bit in the U2C1 register is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.6 shows the Serial Data Logic Switching.

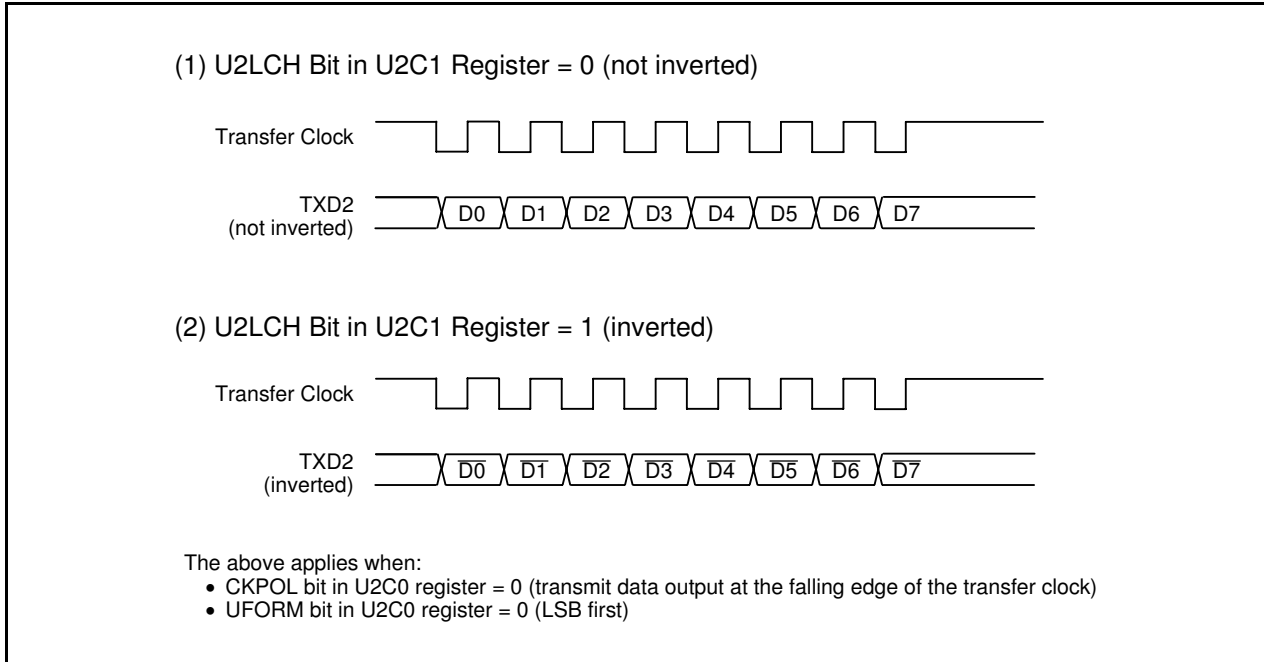


Figure 21.6 Serial Data Logic Switching

### 21.3.6 $\overline{\text{CTS}}$ / $\overline{\text{RTS}}$ Function

The  $\overline{\text{CTS}}$  function is used to start transmit and receive operation when “L” is applied to the  $\overline{\text{CTS2/RTS2}}$  pin. Transmit and receive operation begins when the  $\overline{\text{CTS2/RTS2}}$  pin is held low. If the “L” signal is switched to “H” during a transmit or receive operation, the operation stops before the next data.

For the  $\overline{\text{RTS}}$  function, the  $\overline{\text{CTS2/RTS2}}$  pin outputs “L” when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ( $\overline{\text{CTS/RTS}}$  function disabled)  
The  $\overline{\text{CTS2/RTS2}}$  pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ( $\overline{\text{CTS}}$  function selected)  
The  $\overline{\text{CTS2/RTS2}}$  pin operates as the  $\overline{\text{CTS}}$  function.
- The CRD bit = 0, CRS bit = 1 ( $\overline{\text{RTS}}$  function selected)  
The  $\overline{\text{CTS2/RTS2}}$  pin operates as the  $\overline{\text{RTS}}$  function.

## 21.4 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired bit rate and transfer data format. Table 21.5 lists the UART Mode Specifications. Table 21.6 lists the Registers Used and Settings in UART Mode.

**Table 21.5 UART Mode Specifications**

| Item                                | Specification   |
|-------------------------------------|---|
| Transfer data format                | <ul style="list-style-type: none"> <li>Character bits (transfer data): Selectable from 7, 8, or 9 bits</li> <li>Start bit: 1 bit</li> <li>Parity bit: Selectable from odd, even, or none</li> <li>Stop bits: Selectable from 1 bit or 2 bits</li> </ul>   |
| Transfer clock                      | <ul style="list-style-type: none"> <li>The CKDIR bit in the U2MR register is set to 0 (internal clock): <math>f_j / (16(n + 1))</math><br/> <math>f_j = f_1, f_8, f_{32}, f_C</math> n = setting value in the U2BRG register: 00h to FFh</li> <li>The CKDIR bit is set to 1 (external clock): <math>f_{EXT} / (16(n + 1))</math><br/> <math>f_{EXT}</math>: Input from CLK2 pin n: Setting value in the U2BRG register: 00h to FFh</li> </ul>   |
| Transmit/receive control            | Selectable from the $\overline{CTS}$ function, $\overline{RTS}$ function, or $\overline{CTS}/\overline{RTS}$ function disabled.   |
| Transmit start conditions           | To start transmission, the following requirements must be met: <ul style="list-style-type: none"> <li>The TE bit in the U2C1 register is set to 1 (transmission enabled).</li> <li>The T1 bit in the U2C1 register is set to 0 (data present in the U2TB register).</li> <li>If the <math>\overline{CTS}</math> function is selected, input to the <math>\overline{CTS2}</math> pin = "L".</li> </ul>   |
| Receive start conditions            | To start reception, the following requirements must be met: <ul style="list-style-type: none"> <li>The RE bit in the U2C1 register is set to 1 (reception enabled).</li> <li>Start bit detection</li> </ul>   |
| Interrupt request generation timing | For transmission, one of the following conditions can be selected. <ul style="list-style-type: none"> <li>The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty):<br/>When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission).</li> <li>The U2IRS bit is set to 1 (transmission completed):<br/>When data transmission from the UART2 transmit register is completed.</li> </ul> For reception <ul style="list-style-type: none"> <li>When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).</li> </ul>  |
| Error detection                     | <ul style="list-style-type: none"> <li>Overrun error <sup>(1)</sup><br/>This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data.</li> <li>Framing error <sup>(2)</sup><br/>This error occurs when the set number of stop bits is not detected.</li> <li>Parity error <sup>(2)</sup><br/>This error occurs when if parity is enabled, the number of 1's in the parity and character bits does not match the set number of 1's.</li> <li>Error sum flag<br/>This flag is set to 1 if an overrun, framing, or parity error occurs.</li> </ul> |
| Selectable functions                | <ul style="list-style-type: none"> <li>LSB first, MSB first selection<br/>Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected.</li> <li>Serial data logic switching<br/>This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted.</li> <li>TXD, RXD I/O polarity switching<br/>This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted.</li> <li>RXD2 digital filter selection<br/>The RXD2 input signal can be enabled or disabled.</li> </ul>   |

Notes:

- If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.
- The framing error flag and the parity error flag are set to 1 when data is transferred from the UART2 receive register to the U2RB register.

**Table 21.6 Registers Used and Settings in UART Mode**

| Register | Bit                | Function   |
|----------|--------------------|--|
| U2TB     | b0 to b8           | Set transmit data. (1)   |
| U2RB     | b0 to b8           | Receive data can be read. (1, 2)   |
|          | OER, FER, PER, SUM | Error flag   |
| U2BRG    | b0 to b7           | Set a bit rate.  |
| U2MR     | SMD2 to SMD0       | Set to 100b when transfer data is 7 bits long.<br>Set to 101b when transfer data is 8 bits long.<br>Set to 110b when transfer data is 9 bits long. |
|          | CKDIR              | Select the internal clock or external clock.   |
|          | STPS               | Select the stop bit.   |
|          | PRY, PRYE          | Select whether parity is included and whether odd or even.   |
|          | IOPOL              | Select the TXD/RXD I/O polarity.   |
| U2C0     | CLK0, CLK1         | Select the count source for the U2BRG register.  |
|          | CRS                | Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions.  |
|          | TXEPT              | Transmit register empty flag   |
|          | CRD                | Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.   |
|          | NCH                | Select TXD2 pin output mode.   |
|          | CKPOL              | Set to 0.  |
|          | UFORM              | Select LSB first or MSB first when transfer data is 8 bits long.<br>Set to 0 when transfer data is 7 or 9 bits long.                               |
| U2C1     | TE                 | Set to 1 to enable transmission.   |
|          | TI                 | Transmit buffer empty flag   |
|          | RE                 | Set to 1 to enable reception.  |
|          | RI                 | Receive complete flag  |
|          | U2IRS              | Select the UART2 transmit interrupt source.  |
|          | U2RRM              | Set to 0.  |
|          | U2LCH              | Set to 1 to use inverted data logic.   |
|          | U2ERE              | Set to 0.  |
| U2SMR    | b0 to b7           | Set to 0.  |
| U2SMR2   | b0 to b7           | Set to 0.  |
| U2SMR3   | b0 to b7           | Set to 0.  |
| U2SMR4   | b0 to b7           | Set to 0.  |
| URXDF    | DF2EN              | Select the digital filter disabled or enabled.   |
| U2SMR5   | MP                 | Set to 0.  |

## Notes:

- The bits used for transmit/receive data are as follows:
  - Bits b0 to b6 when transfer data is 7 bits long
  - Bits b0 to b7 when transfer data is 8 bits long
  - Bits b0 to b8 when transfer data is 9 bits long
- The contents of the following are undefined:
  - Bits b7 and b8 when transfer data is 7 bits long
  - Bit b8 when transfer data is 8 bits long



Table 21.7 lists the I/O Pin Functions in UART Mode.

Note that for a period from when the UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs “H”. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)

Figure 21.7 shows the Transmit Timing in UART Mode. Figure 21.8 shows the Receive Timing in UART Mode.

**Table 21.7 I/O Pin Functions in UART Mode**

| Pin Name                      | Function             | Selection Method  |
|-------------------------------|----------------------|---|
| TXD2<br>(P3_4 or P3_7)        | Serial data output   | <ul style="list-style-type: none"> <li>• When TXD2 (P3_4)<br/>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 10b (P3_4)</li> <li>• When TXD2 (P3_7)<br/>Bits TXD2SEL1 to TXD2SEL0 in U2SR0 register = 01b (P3_7)</li> <li>• For reception only:<br/>P3_4 and P3_7 can be used as ports by setting TXD2SEL1 to TXD2SEL0 to 00b.</li> </ul>  |
| RXD2<br>(P3_4, P3_7, or P4_5) | Serial data input    | <ul style="list-style-type: none"> <li>• When RXD2 (P3_4)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 01b (P3_4)<br/>PD3_4 bit in PD3 register = 0</li> <li>• When RXD2 (P3_7)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 10b (P3_7)<br/>PD3_7 bit in PD3 register = 0</li> <li>• When RXD2 (P4_5)<br/>Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P4_5)<br/>PD4_5 bit in PD4 register = 0</li> <li>• For transmission only:<br/>P3_4, P3_7, and P4_5 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.</li> </ul> |
| CLK2 (P3_5)                   | I/O port             | CLK2SEL0 bit in U2SR1 register = 0  |
|                               | Transfer clock input | CLK2SEL0 bit in U2SR1 register = 1<br>CKDIR bit in U2MR register = 1<br>PD3_5 bit in PD3 register = 0   |
| CTS2/RTS2<br>(P3_3)           | CTS input            | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 0<br>PD3_3 bit in PD3 register = 0   |
|                               | RTS output           | CTS2SEL0 bit in U2SR1 register = 1<br>CRD bit in U2C0 register = 0<br>CRS bit in U2C0 register = 1  |
|                               | I/O port             | CTS2SEL0 bit in U2SR1 register = 0  |

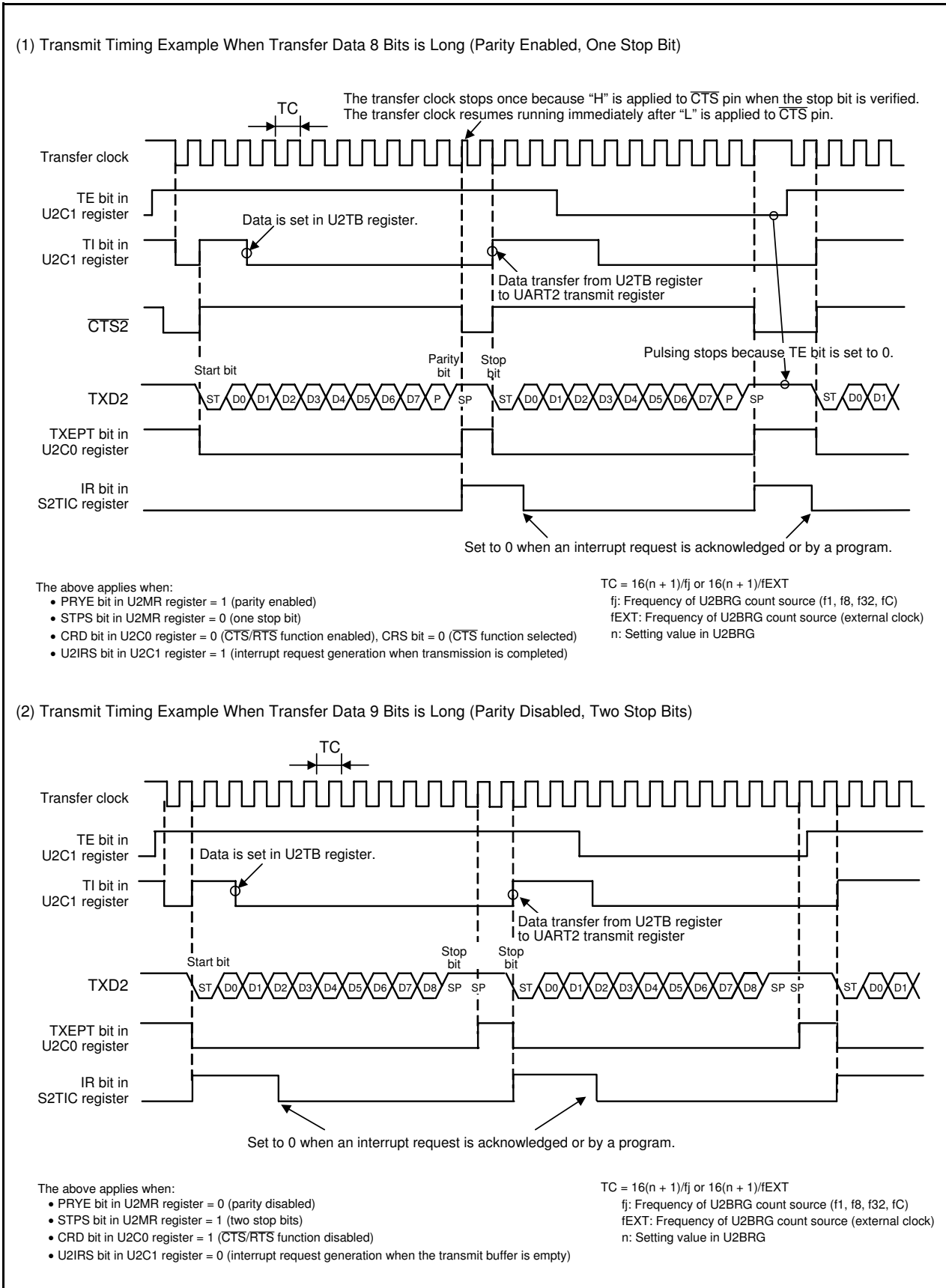
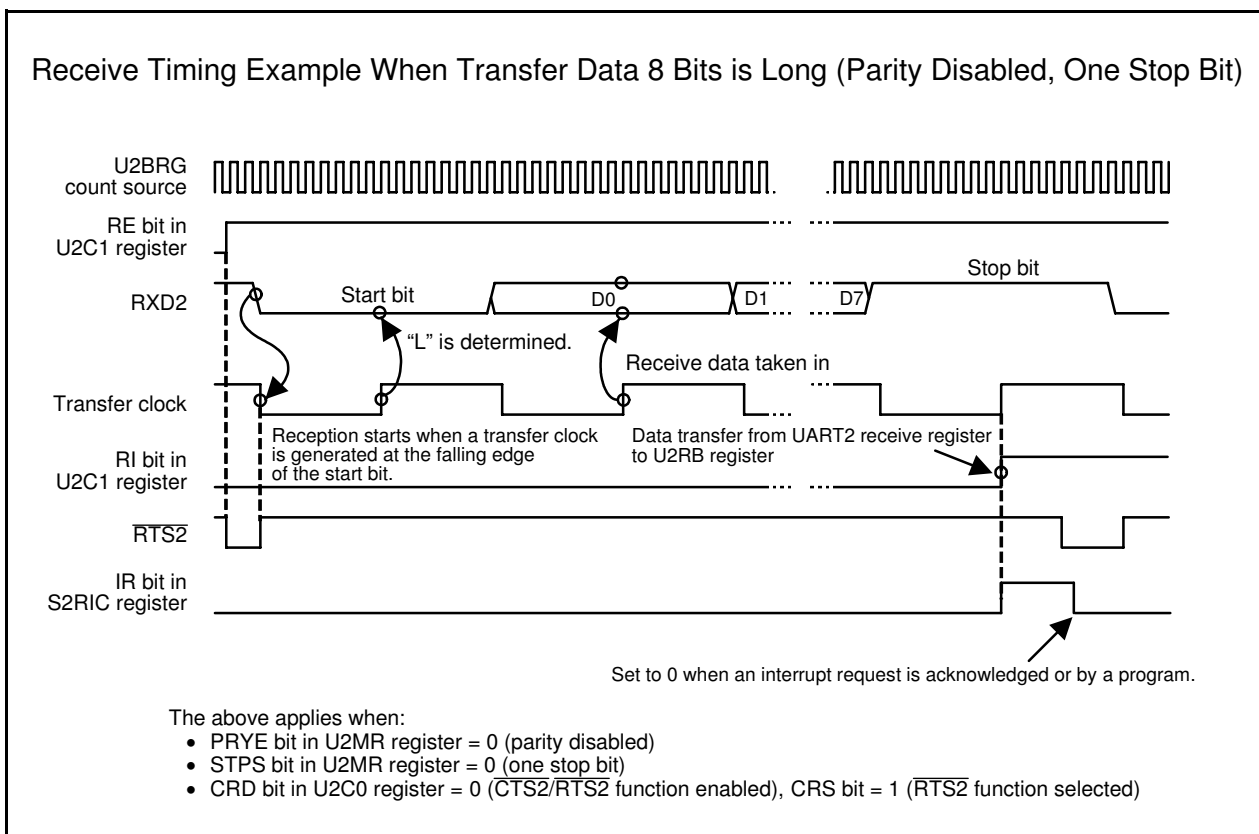


Figure 21.7 Transmit Timing in UART Mode



**Figure 21.8 Receive Timing in UART Mode**

### 21.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Table 21.8 lists the Bit Rate Setting Example in UART Mode (Internal Clock Selected).

**Table 21.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**

| Bit Rate (bps) | U2BRG Count Source | System Clock = 20 MHz |                   |                   | System Clock = 18.432 MHz <sup>(1)</sup> |                   |                   | System Clock = 8 MHz |                   |                   |
|----------------|--------------------|-----------------------|-------------------|-------------------|--|-------------------|-------------------|----------------------|-------------------|-------------------|
|                |                    | U2BRG Setting Value   | Actual Time (bps) | Setting Error (%) | U2BRG Setting Value                      | Actual Time (bps) | Setting Error (%) | U2BRG Setting Value  | Actual Time (bps) | Setting Error (%) |
| 1200           | f8                 | 129 (81h)             | 1201.92           | 0.16              | 119 (77h)                                | 1200.00           | 0.00              | 51 (33h)             | 1201.92           | 0.16              |
| 2400           | f8                 | 64 (40h)              | 2403.85           | 0.16              | 59 (3Bh)                                 | 2400.00           | 0.00              | 25 (19h)             | 2403.85           | 0.16              |
| 4800           | f8                 | 32 (20h)              | 4734.85           | -1.36             | 29 (1Dh)                                 | 4800.00           | 0.00              | 12 (0Ch)             | 4807.69           | 0.16              |
| 9600           | f1                 | 129 (81h)             | 9615.38           | 0.16              | 119 (77h)                                | 9600.00           | 0.00              | 51 (33h)             | 9615.38           | 0.16              |
| 14400          | f1                 | 86 (56h)              | 14367.82          | -0.22             | 79 (4Fh)                                 | 14400.00          | 0.00              | 34 (22h)             | 14285.71          | -0.79             |
| 19200          | f1                 | 64 (40h)              | 19230.77          | 0.16              | 59 (3Bh)                                 | 19200.00          | 0.00              | 25 (19h)             | 19230.77          | 0.16              |
| 28800          | f1                 | 42 (2Ah)              | 29069.77          | 0.94              | 39 (27h)                                 | 28800.00          | 0.00              | 16 (10h)             | 29411.76          | 2.12              |
| 38400          | f1                 | 32 (20h)              | 37878.79          | -1.36             | 29 (1Dh)                                 | 38400.00          | 0.00              | 12 (0Ch)             | 38461.54          | 0.16              |
| 57600          | f1                 | 21 (15h)              | 56818.18          | -1.36             | 19 (13h)                                 | 57600.00          | 0.00              | 8 (08h)              | 55555.56          | -3.55             |
| 115200         | f1                 | 10 (0Ah)              | 113636.36         | -1.36             | 9 (09h)                                  | 115200.00         | 0.00              | -                    | -                 | -                 |

Note:

1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register. This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **26. Electrical Characteristics**.

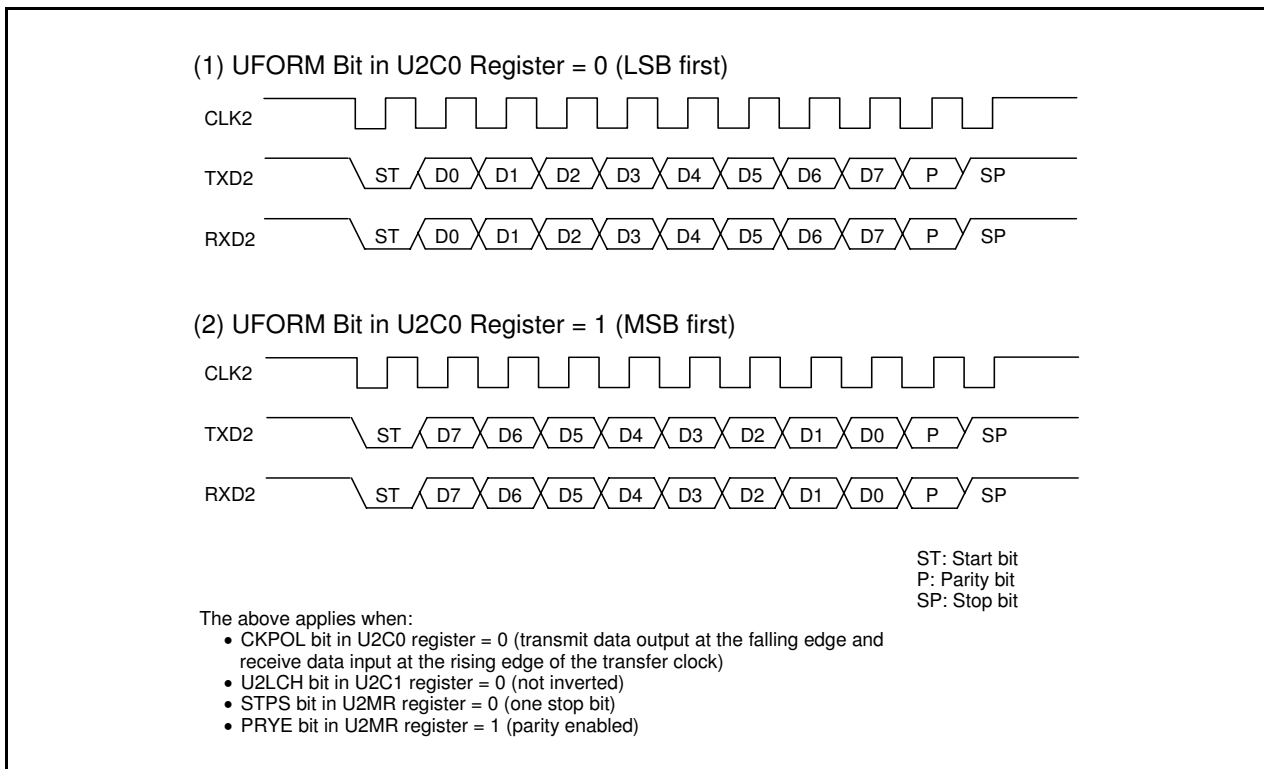
### 21.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

- (1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
- (2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
- (3) Set bits SMD2 to SMD0 in the U2MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
- (4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

### 21.4.3 LSB First/MSB First Select Function

As shown in Figure 21.9, use the UFORM bit in the U2C0 register to select the transfer format. This function is enabled when transfer data is 8 bits long. Figure 21.9 shows the Transfer Format.



**Figure 21.9** Transfer Format

### 21.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.10 shows the Serial Data Logic Switching.

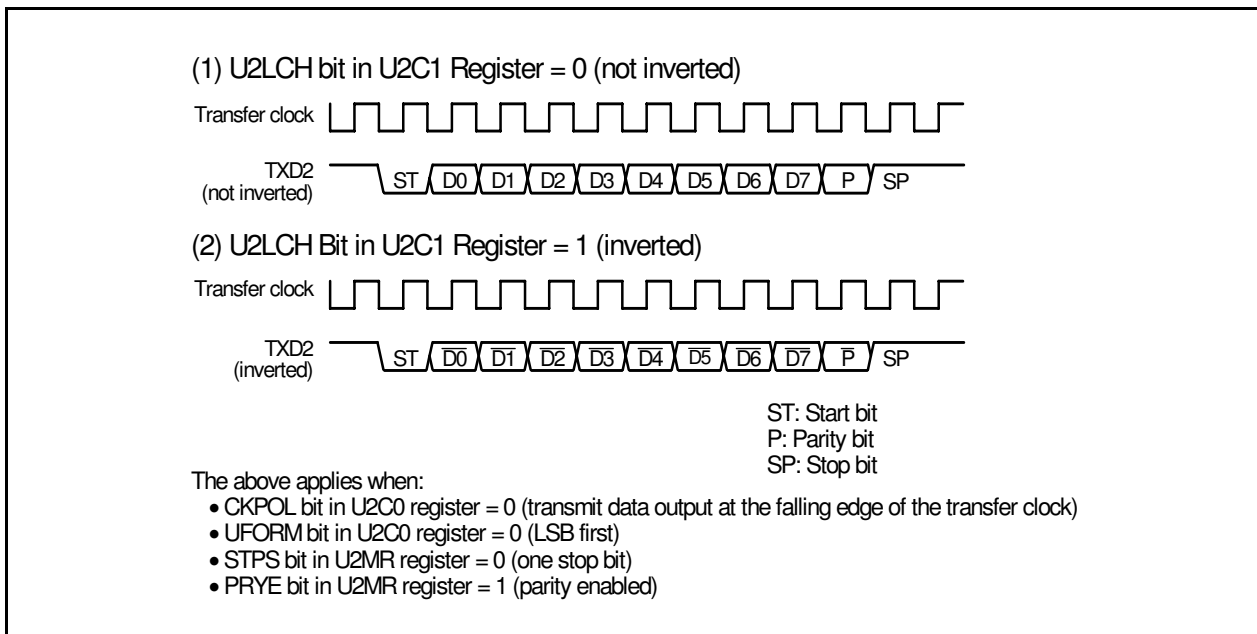


Figure 21.10 Serial Data Logic Switching

### 21.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 21.11 shows the TXD and RXD I/O Inversion.

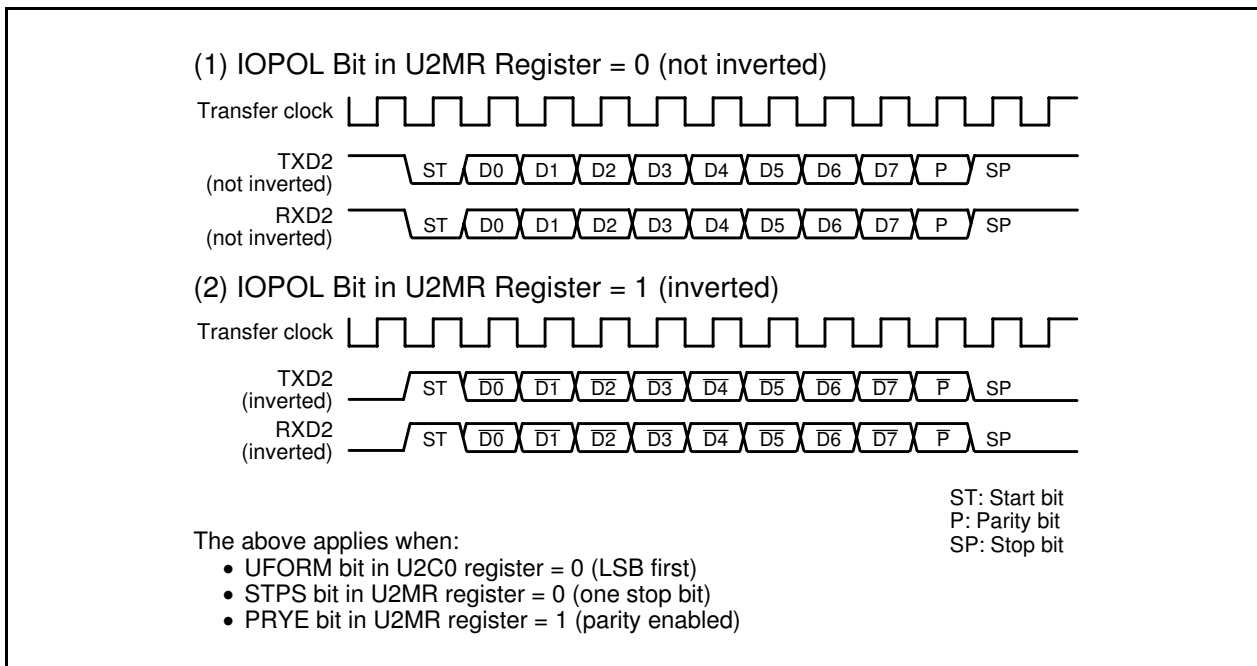


Figure 21.11 TXD and RXD I/O Inversion

### 21.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The  $\overline{\text{CTS}}$  function is used to start transmit operation when “L” is applied to the  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin. Transmit operation begins when the  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin is held low. If the “L” signal is switched to “H” during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.

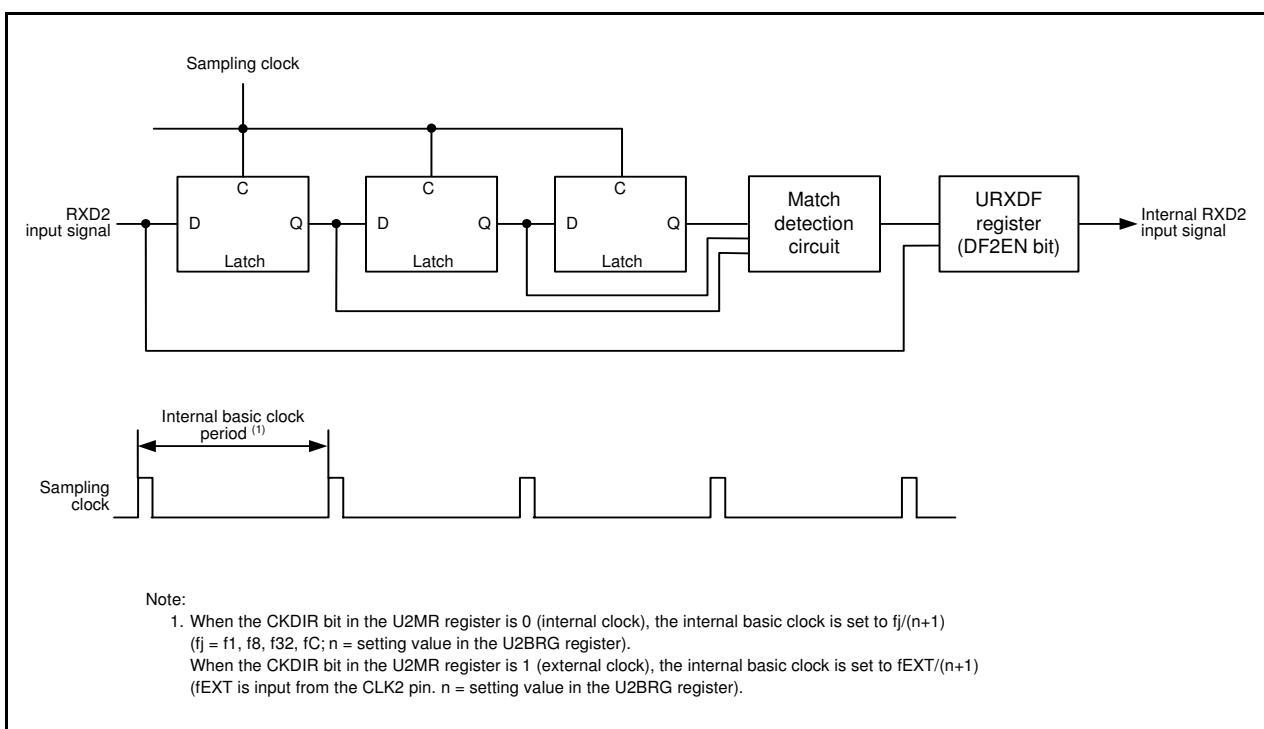
When the  $\overline{\text{RTS}}$  function is used, the  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin outputs “L” when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ( $\overline{\text{CTS}}/\overline{\text{RTS}}$  function disabled)  
The  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ( $\overline{\text{CTS}}$  function selected)  
The  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin operates as the  $\overline{\text{CTS}}$  function.
- The CRD bit = 0, CRS bit = 1 ( $\overline{\text{RTS}}$  function selected)  
The  $\overline{\text{CTS2}}/\overline{\text{RTS2}}$  pin operates as the  $\overline{\text{RTS}}$  function.

### 21.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filter enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.

In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise. Figure 21.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



**Figure 21.12** Block Diagram of RXD2 Digital Filter Circuit

## 21.5 Special Mode 1 (I<sup>2</sup>C Mode)

I<sup>2</sup>C mode is provided for use as a simplified I<sup>2</sup>C interface compatible mode. Table 21.9 lists the I<sup>2</sup>C Mode Specifications. Tables 21.10 and 21.11 list the registers used in I<sup>2</sup>C mode and the settings. Table 21.12 lists the I<sup>2</sup>C Mode Functions, Figure 21.13 shows an I<sup>2</sup>C Mode Block Diagram, and Figure 21.14 shows the Transfer to U2RB Register and Interrupt Timing.

As shown in Table 21.12, the MCU is placed in I<sup>2</sup>C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

**Table 21.9 I<sup>2</sup>C Mode Specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Transfer data format                | Transfer data length: 8 bits   |
| Transfer clock                      | <ul style="list-style-type: none"> <li>• Master mode<br/>The CKDIR bit in the U2MR register is set to 0 (internal clock): <math>f_j / (2(n+1))</math><br/><math>f_j = f_1, f_8, f_{32}, f_C</math> n = setting value in the U2BRG register: 00h to FFh</li> <li>• Slave mode<br/>The CKDIR bit is set to 1 (external clock): Input from the SCL2 pin</li> </ul>            |
| Transmit start conditions           | To start transmission, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>• The TE bit in the U2C1 register is set to 1 (transmission enabled).</li> <li>• The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).</li> </ul>  |
| Receive start conditions            | To start reception, the following requirements must be met: <sup>(1)</sup> <ul style="list-style-type: none"> <li>• The RE bit in the U2C1 register is set to 1 (reception enabled).</li> <li>• The TE bit in the U2C1 register is set to 1 (transmission enabled).</li> <li>• The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).</li> </ul> |
| Interrupt request generation timing | Start/stop condition detection, no acknowledgement detection, or acknowledgement detection   |
| Error detection                     | Overrun error <sup>(2)</sup><br>This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 8th bit of the next unit of data.   |
| Selectable functions                | <ul style="list-style-type: none"> <li>• SDA2 digital delay<br/>No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected.</li> <li>• Clock phase setting<br/>With or without clock delay can be selected.</li> </ul>  |

Notes:

1. When an external clock is selected, the requirements must be met while the external clock is held high.
2. If an overrun error occurs, the received data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.

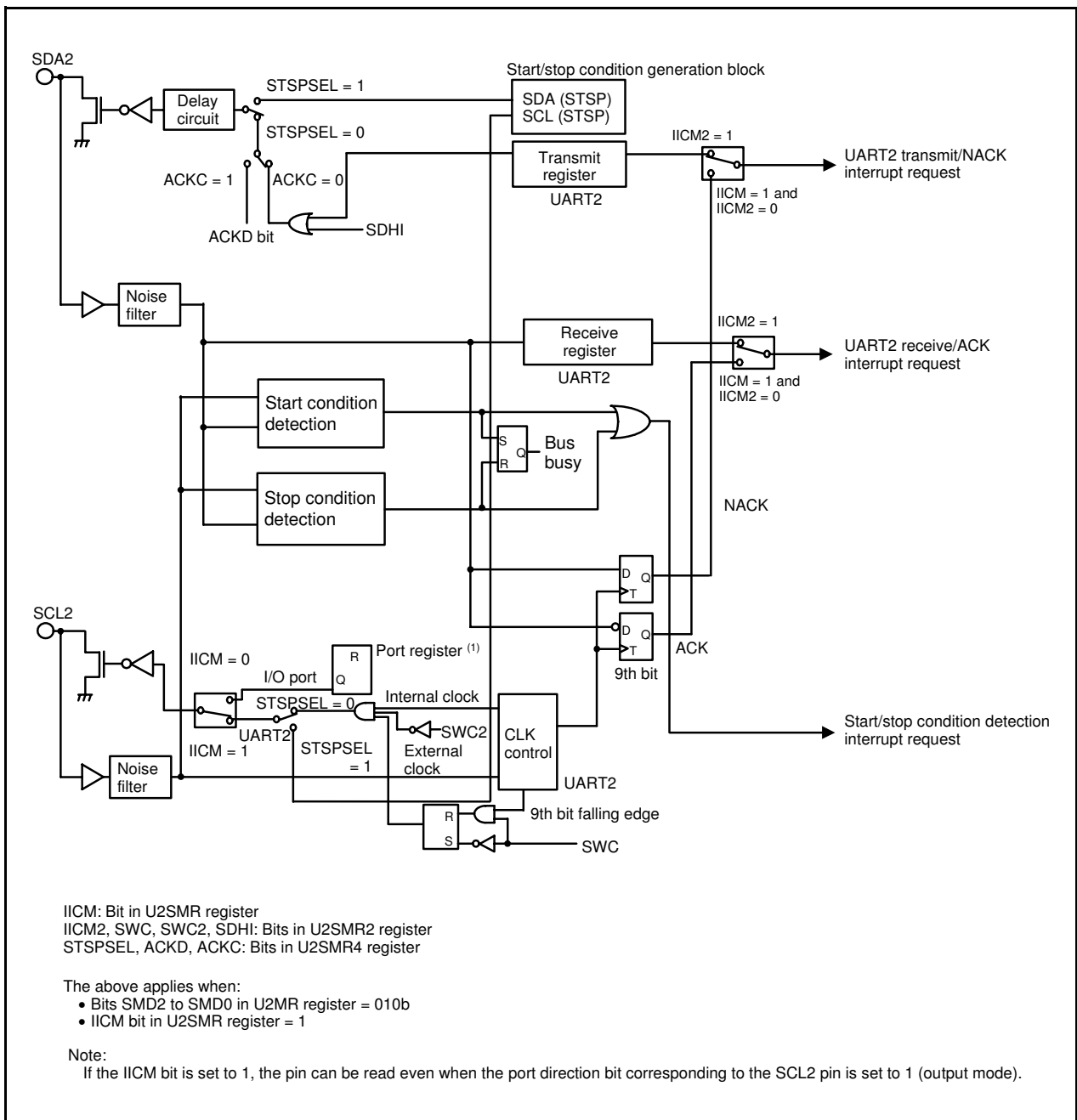


Figure 21.13 I2C Mode Block Diagram



**Table 21.10 Registers Used and Settings in I<sup>2</sup>C Mode (1)**

| Register | Bit                 | Function   |  |
|----------|---------------------|--|--|
|          |                     | Master   | Slave  |
| U2TB (1) | b0 to b7            | Set transmit data.   | Set transmit data.   |
| U2RB (1) | b0 to b7            | Receive data can be read.  | Receive data can be read.  |
|          | b8                  | ACK or NACK is set in this bit.  | ACK or NACK is set in this bit.  |
|          | OER                 | Overrun error flag   | Overrun error flag   |
| U2BRG    | b0 to b7            | Set a bit rate.  | Disabled   |
| U2MR (1) | SMD2 to SMD0        | Set to 010b.   | Set to 010b.   |
|          | CKDIR               | Set to 0.  | Set to 1.  |
|          | IOPOL               | Set to 0.  | Set to 0.  |
| U2C0     | CLK1, CLK0          | Select the count source for the U2BRG register.                              | Disabled   |
|          | CRS                 | Disabled because CRD = 1.  | Disabled because CRD = 1.  |
|          | TXEPT               | Transmit register empty flag   | Transmit register empty flag   |
|          | CRD                 | Set to 1.  | Set to 1.  |
|          | NCH                 | Set to 1.  | Set to 1.  |
|          | CKPOL               | Set to 0.  | Set to 0.  |
|          | UFORM               | Set to 1.  | Set to 1.  |
| U2C1     | TE                  | Set to 1 to enable transmission.   | Set to 1 to enable transmission.   |
|          | TI                  | Transmit buffer empty flag   | Transmit buffer empty flag   |
|          | RE                  | Set to 1 to enable reception.  | Set to 1 to enable reception.  |
|          | RI                  | Receive complete flag  | Receive complete flag  |
|          | U2IRS               | Set to 1.  | Set to 1.  |
|          | U2RRM, U2LCH, U2ERE | Set to 0.  | Set to 0.  |
| U2SMR    | IICM                | Set to 1.  | Set to 1.  |
|          | BBS                 | Bus busy flag  | Bus busy flag  |
|          | b3 to b7            | Set to 0.  | Set to 0.  |
| U2SMR2   | IICM2               | Refer to <b>Table 21.12 I<sup>2</sup>C Mode Functions.</b>                   | Refer to <b>Table 21.12 I<sup>2</sup>C Mode Functions.</b>                   |
|          | CSC                 | Set to 1 to enable clock synchronization.                                    | Set to 0.  |
|          | SWC                 | Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock. | Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock. |
|          | STAC                | Set to 0.  | Set to 1 to initialize UART2 at start condition detection                    |
|          | SWC2                | Set to 1 to forcibly pull SCL2 low.  | Set to 1 to forcibly pull SCL2 output low.                                   |
|          | SDHI                | Set to 1 to disable SDA2 output.   | Set to 1 to disable SDA2 output.   |
|          | b7                  | Set to 0.  | Set to 0.  |

Note:

1. Set the bits not listed in this table to 0 when writing to the above registers in I<sup>2</sup>C mode.

**Table 21.11 Registers Used and Settings in I<sup>2</sup>C Mode (2)**

| Register | Bit                  | Function  |  |
|----------|----------------------|---|--|
|          |                      | Master  | Slave  |
| U2SMR3   | b0, b2, b4, and NODC | Set to 0.   | Set to 0.  |
|          | CKPH                 | Refer to <b>Table 21.12 I<sup>2</sup>C Mode Functions.</b>      | Refer to <b>Table 21.12 I<sup>2</sup>C Mode Functions.</b>             |
|          | DL2 to DL0           | Set the amount of SDA2 digital delay.                           | Set the amount of SDA2 digital delay.                                  |
| U2SMR4   | STAREQ               | Set to 1 to generate a start condition.                         | Set to 0.  |
|          | RSTAREQ              | Set to 1 to generate a restart condition.                       | Set to 0.  |
|          | STPREQ               | Set to 1 to generate a stop condition.                          | Set to 0.  |
|          | STSPSEL              | Set to 1 to output each condition.                              | Set to 0.  |
|          | ACKD                 | Select ACK or NACK.   | Select ACK or NACK.  |
|          | ACKC                 | Set to 1 to output ACK data.                                    | Set to 1 to output ACK data.   |
|          | SCLHI                | Set to 1 to stop SCL2 output when a stop condition is detected. | Set to 0.  |
|          | SWC9                 | Set to 0.   | Set to 1 to hold SCL2 low at the falling edge of the 9th bit of clock. |
| URXDF    | DF2EN                | Set to 0.   | Set to 0.  |
| U2SMR5   | MP                   | Set to 0.   | Set to 0.  |

Table 21.12 I<sup>2</sup>C Mode Functions

| Function   | Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)                               | I <sup>2</sup> C Mode (SMD2 to SMD0 = 010b, IICM = 1)   |  |  |   |
|--|---|---|--|--|---|
|  |   | IICM2 = 0 (NACK/ACK interrupt)  |  | IICM2 = 1 (UART transmit/receive interrupt)                |   |
|  |   | CKPH = 0 (No Clock Delay)   | CKPH = 1 (With Clock Delay)  | CKPH = 0 (No Clock Delay)                                  | CKPH = 1 (With Clock Delay)   |
| Source of UART2 bus collision interrupt <sup>(1, 5)</sup>                        | –   | Start condition detection or stop condition detection<br>(Refer to <b>Table 21.13 STSPSEL Bit Functions</b> ) |  |  |   |
| Source of UART2 transmit/NACK2 <sup>(1, 6)</sup>                                 | UART2 transmission<br>Transmission started or completed (selectable by U2IRS bit)               | No acknowledgment detection (NACK)<br>Rising edge of SCL2 9th bit   | UART2 transmission<br>Rising edge of SCL2 9th bit  | UART2 transmission<br>Falling edge of SCL2 next to 9th bit |   |
| Source of UART2 receive/ACK2 <sup>(1, 6)</sup>                                   | UART2 reception<br>When 8th bit received<br>CKPOL = 0 (rising edge)<br>CKPOL = 1 (falling edge) | Acknowledgment detection (ACK)<br>Rising edge of SCL2 9th bit   | UART2 reception<br>Falling edge of SCL2 9th bit  |  |   |
| Timing for transferring data from UART reception shift register to U2RB register | CKPOL = 0 (rising edge)<br>CKPOL = 1 (falling edge)   | Rising edge of SCL2 9th bit   | Falling edge of SCL2 9th bit   | Falling and rising edges of SCL2 9th bit                   |   |
| UART2 transmission output delay  | No delay  | With delay  |  |  |   |
| TXD2/SDA2 functions  | TXD2 output   | SDA2 I/O  |  |  |   |
| RXD2/SCL2 functions  | RXD2 input  | SCL2 I/O  |  |  |   |
| CLK2 functions   | CLK2 input or output port selected  | – (Cannot be used in I <sup>2</sup> C mode.)  |  |  |   |
| Noise filter width   | 15 ns   | 200 ns  |  |  |   |
| Read of RXD2 and SCL2 pin levels   | Possible when the corresponding port direction bit = 0  | Possible regardless of the content of the corresponding port direction bit.                                   |  |  |   |
| Initial value of TXD2 and SDA2 outputs   | CKPOL = 0 (“H”)<br>CKPOL = 1 (“L”)  | The value set in the port register before setting I <sup>2</sup> C mode. <sup>(2)</sup>                       |  |  |   |
| Initial and end values of SCL2   | –   | “H”   | “L”  | “H”  | “L”   |
| Storage of receive data  | 1st to 8th bits of the received data are stored in bits b0 to b7 in the U2RB register.          | 1st to 8th bits of the received data are stored in bits b7 to b0 in the U2RB register.                        | 1st to 7th bits of the received data are stored in bits b6 to b0 in the U2RB register. 8th bit is stored in bit b8 in the U2RB register. |  |   |
| Read of receive data   | The U2RB register status is read.   |   |  |  | 1st to 8th bits are stored in bits b7 to b0 in the U2RB register. <sup>(3)</sup><br>Bits b6 to b0 in the U2RB register are read as bits b7 to b1. Bit b8 in the U2RB register is read as bit b0. <sup>(4)</sup> |

## Notes:

1. If the source of any interrupt is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to 1 (interrupt requested). (Refer to **11.8 Notes on Interrupts**.)  
If one of the bits listed below is changed, the interrupt source, the interrupt timing, and others change. Therefore, always be sure to set the IR bit to 0 (interrupt not requested) after changing these bits.  
Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, and the CKPH bit in the U2SMR3 register.
2. Set the initial value of SDA2 output while bits SMD2 to SMD0 in the U2MR register are 000b (serial interface disabled).
3. Second data transfer to the U2RB register (rising edge of SCL2 9th bit)
4. First data transfer to the U2RB register (falling edge of SCL2 9th bit)
5. Refer to **Figure 21.16 STSPSEL Bit Functions**.
6. Refer to **Figure 21.14 Transfer to U2RB Register and Interrupt Timing**.

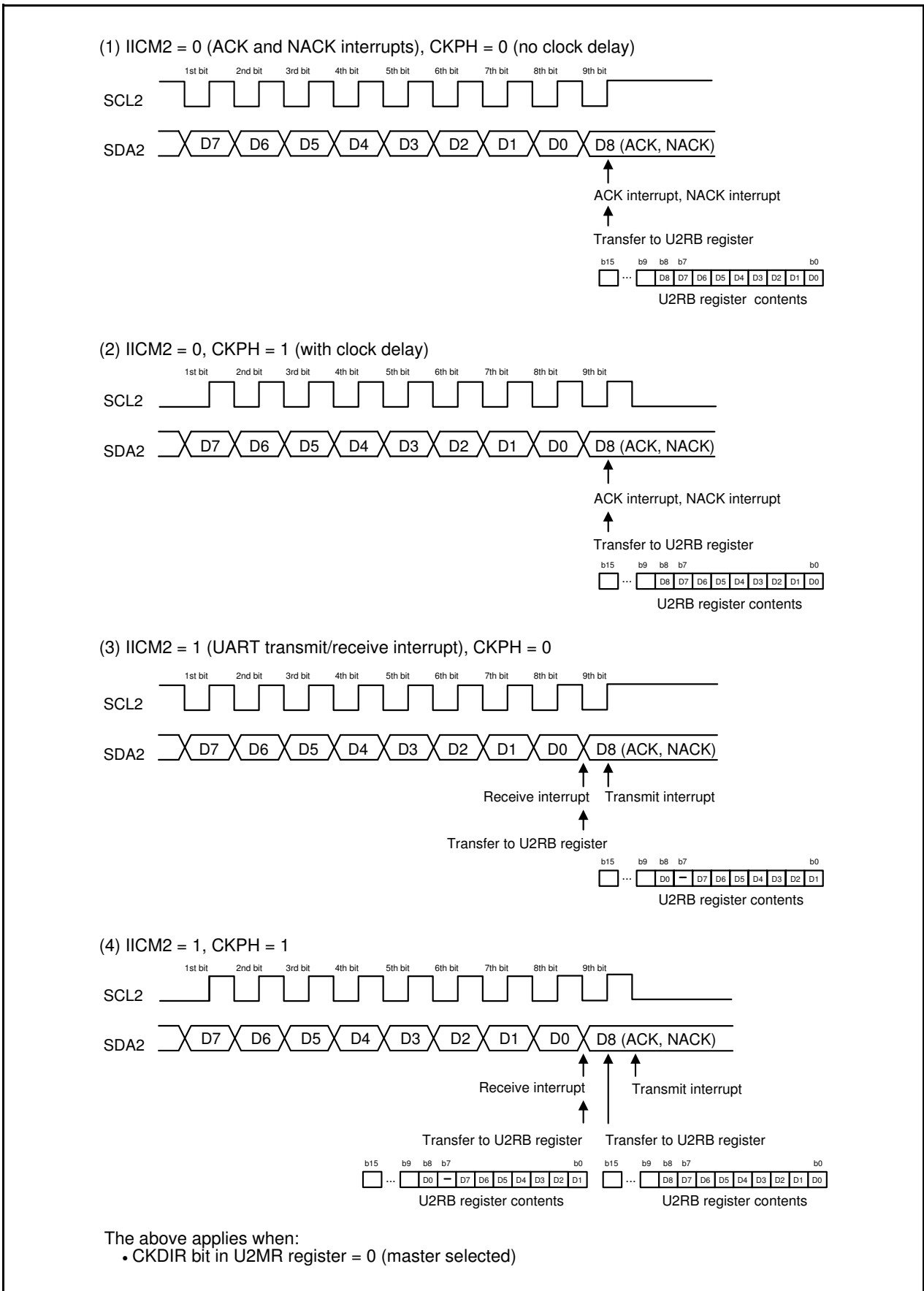


Figure 21.14 Transfer to U2RB Register and Interrupt Timing

### 21.5.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.

A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.

Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.

Figure 21.15 shows the Detection of Start and Stop Conditions.

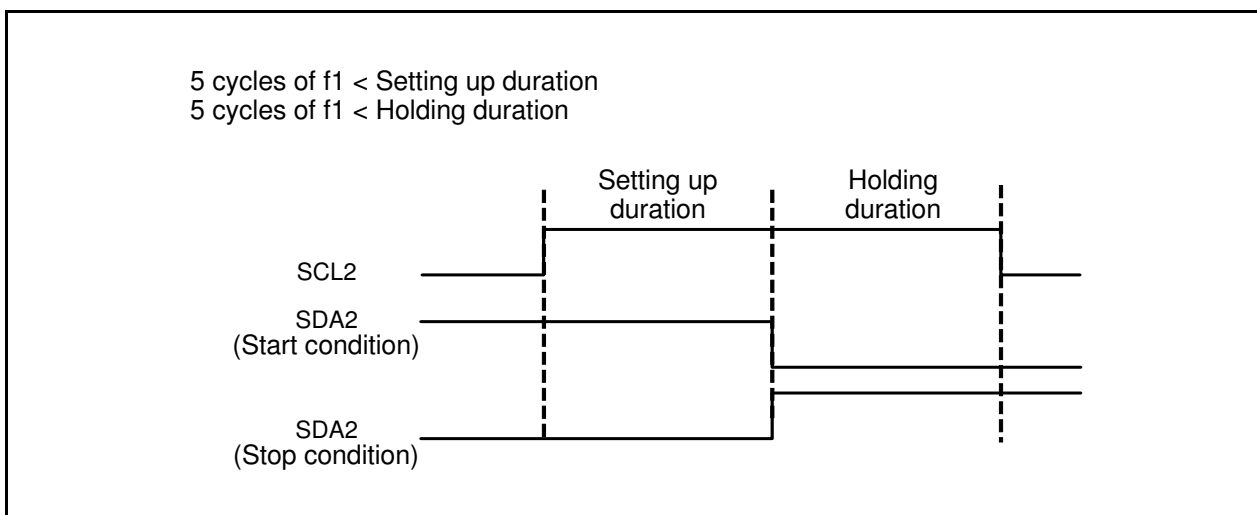


Figure 21.15 Detection of Start and Stop Conditions

### 21.5.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).

A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).

A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is as follows:

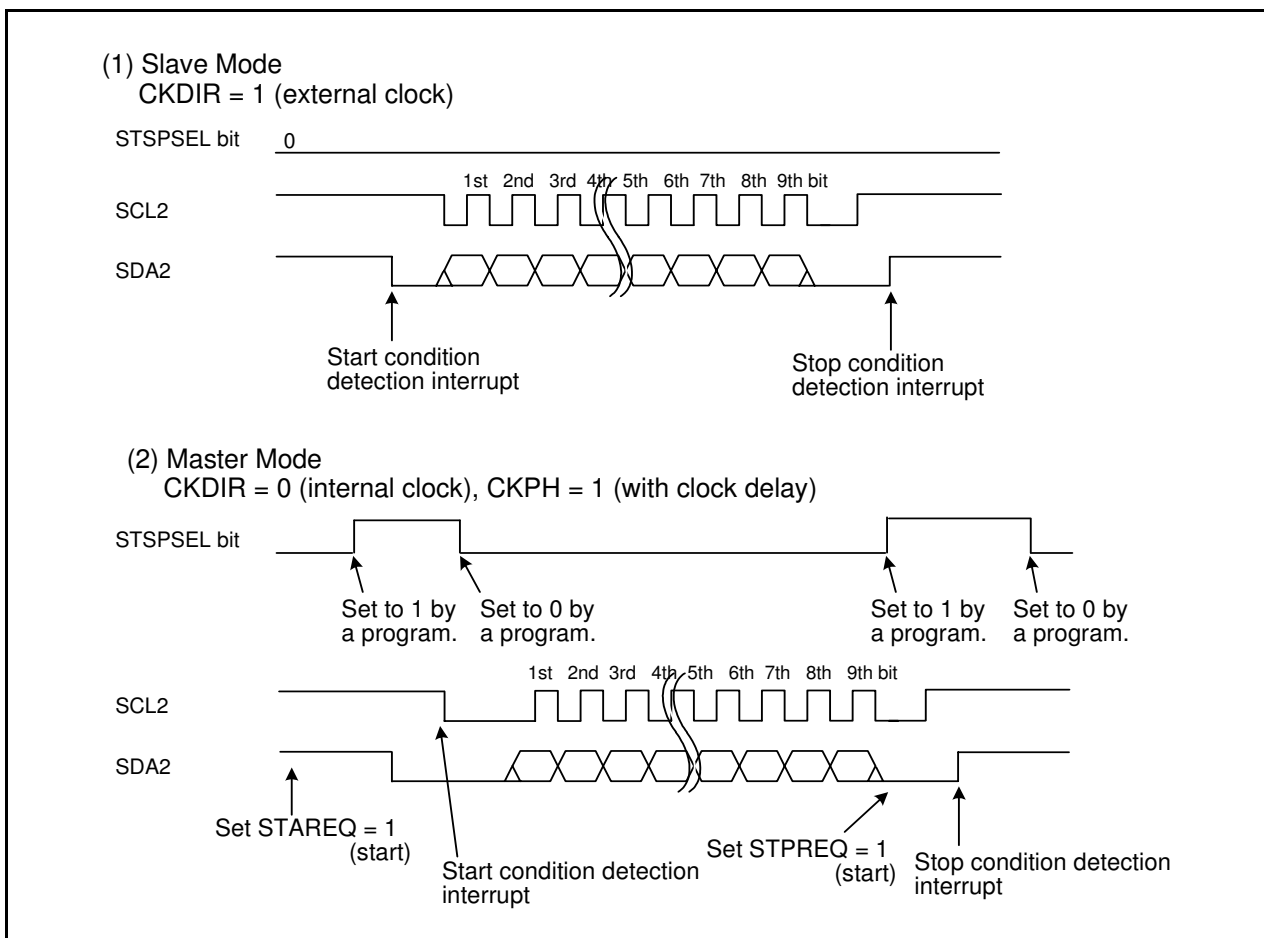
(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).

(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).

Table 21.13 lists the STSPSEL Bit Functions. Figure 21.16 shows the STSPSEL Bit Functions.

**Table 21.13 STSPSEL Bit Functions**

| Function   | STSPSEL = 0   | STSPSEL = 1   |
|--|---|---|
| Output of pins SCL2 and SDA2                             | Output of transfer clock and data<br>Output of start/stop conditions is accomplished by a program using ports (not automatically generated in hardware) | Output of start/stop conditions according to bits STAREQ, RSTAREQ, and STPREQ |
| Start/stop condition interrupt request generation timing | Detection of start/stop conditions  | Completion of start/stop condition generation                                 |



**Figure 21.16 STSPSEL Bit Functions**

### 21.5.3 Transfer Clock

The transfer clock is used to transmit and receive data as is shown in **Figure 21.14 Transfer to U2RB Register and Interrupt Timing**.

The CSC bit in the U2SMR2 register is used to synchronize an internally generated clock (internal SCL2) and an external clock supplied to the SCL2 pin. When the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCL2 pin is detected while the internal SCL2 is high, the internal SCL2 goes low. The value in the U2BRG register is reloaded and counting of the low-level intervals starts. If the internal SCL2 changes state from low to high while the SCL2 pin is low, counting stops. If the SCL2 pin goes high, counting restarts. In this way, the UART2 transfer clock is equivalent to AND of the internal SCL2 and the clock signal applied to the SCL2 pin. The transfer clock works from a half cycle before the falling edge of the internal SCL2 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transfer clock.

The SWC bit in the U2SMR2 register determines whether the SCL2 pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the U2SMR4 register is set to 1 (enabled), SCL2 output is turned off (placed in the high-impedance state) when a stop condition is detected.

Setting the SWC2 bit in the U2SMR2 register to 1 (“L” output) makes it possible to forcibly output a low-level signal from the SCL2 pin even while sending or receiving data. Setting the SWC2 bit to 0 (transfer clock) allows the transfer clock to be output from or supplied to the SCL2 pin, instead of outputting a low-level signal. If the SWC9 bit in the U2SMR4 register is set to 1 (SCL “L” hold enabled) when the CKPH bit in the U2SMR3 register is 1, the SCL2 pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL “L” hold disabled) frees the SCL2 pin from low-level output.

### 21.5.4 SDA Output

The data written to bits b7 to b0 (D7 to D0) in the U2TB register is output in descending order from D7.

The 9th bit (D8) is ACK or NACK.

Set the initial value of SDA2 transmit output when IICM is set to 1 (I<sup>2</sup>C mode) and bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled).

Bits DL2 to DL0 in the U2SMR3 register allow addition of no delays or a delay of 2 to 8 U2BRG count source clock cycles to the SDA2 output.

Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in the high-impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transfer clock.

### 21.5.5 SDA Input

When the IICM2 bit is set to 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits b7 to b0 in the U2RB register. The 9th bit (D8) is ACK or NACK.

When the IICM2 bit is set to 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits b6 to b0 in the U2RB register and the 8th bit (D0) is stored in bit b8 in the U2RB register. Even when the IICM2 bit is set to 1, if the CKPH bit is 1, the same data as when the IICM2 bit is 0 can be read by reading the U2RB register after the rising edge of 9th bit of the clock.

### 21.5.6 ACK and NACK

If the STSPSEL bit in the U2SMR4 register is set to 0 (start and stop conditions not output) and the ACKC bit in the U2SMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the U2SMR4 register is output from the SDA2 pin.

If the IICM2 bit is set to 0, a NACK interrupt request is generated if the SDA2 pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDA2 pin is low at the rising edge of the 9th bit of the transmit clock.

### 21.5.7 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the U2TB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCL2 pin is pulled low at the falling edge of the 9th clock pulse.

Note that when UART2 transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transfer clock to start UART2 transmission/reception with this setting.



## 21.6 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by asynchronous serial communication, in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 21.17 shows an Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A).

The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.

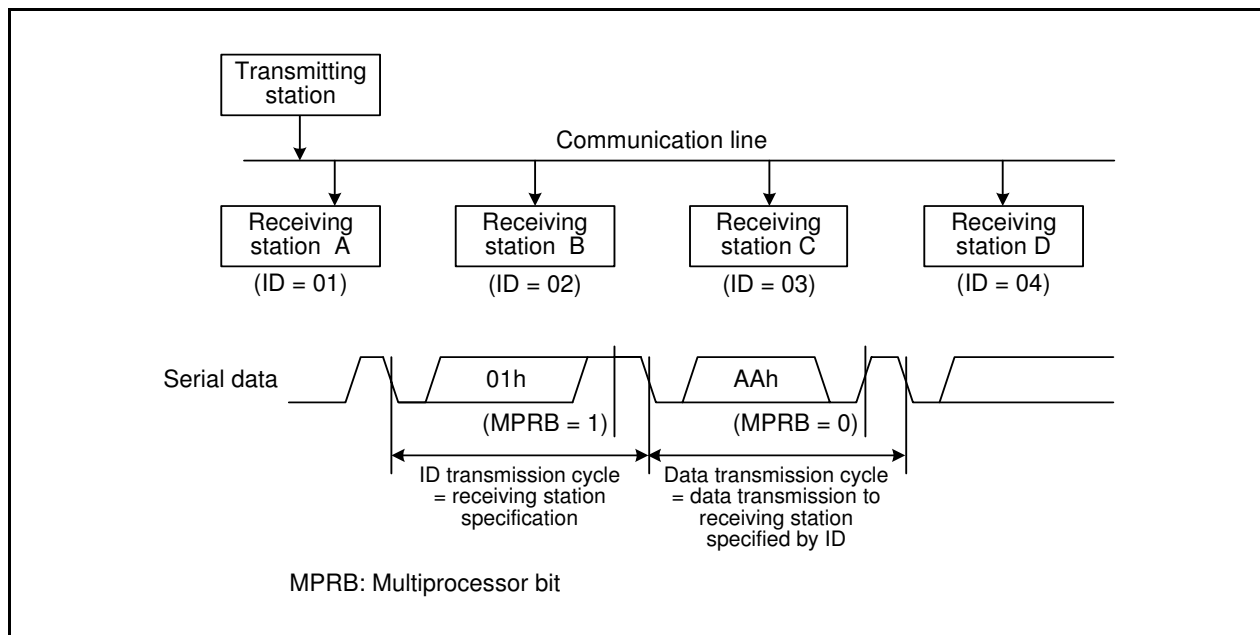
When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal asynchronous mode (UART mode). The clock used for multiprocessor communication is the same as that in normal asynchronous mode (UART mode).

Figure 21.18 shows a Block Diagram of Multiprocessor Communication Function.

Table 21.14 lists the Registers and Settings in Multiprocessor Communication Function.



**Figure 21.17 Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A)**

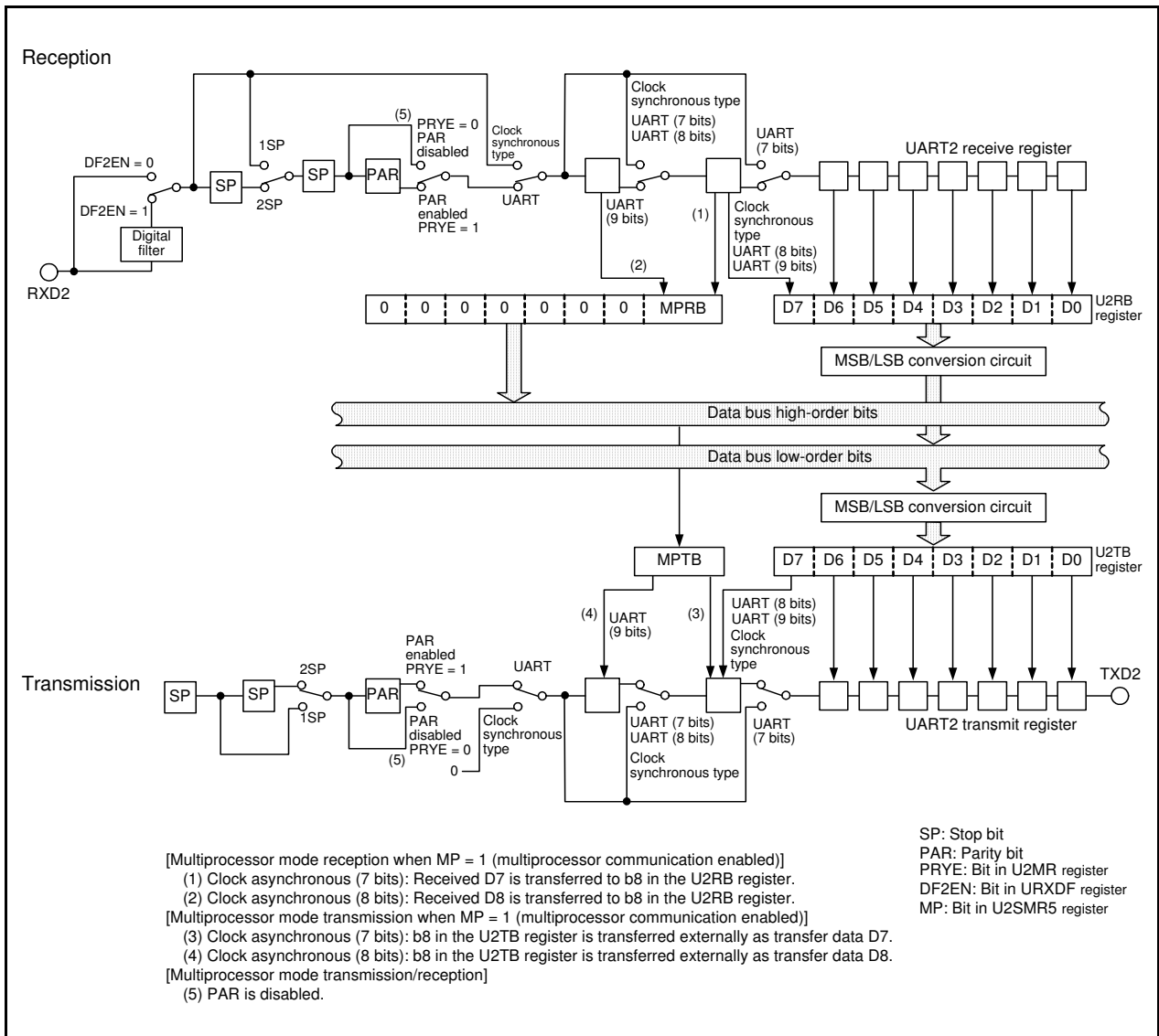


Figure 21.18 Block Diagram of Multiprocessor Communication Function

**Table 21.14 Registers and Settings in Multiprocessor Communication Function**

| Register | Bit           | Function   |
|----------|---------------|--|
| U2TB (1) | b0 to b7      | Set transmit data.   |
|          | MPTB          | Set to 0 or 1.   |
| U2RB (2) | b0 to b7      | Receive data can be read.  |
|          | MPRB          | Multiprocessor bit   |
|          | OER, FER, SUM | Error flag   |
| U2BRG    | b0 to b7      | Set the transfer rate.   |
| U2MR     | SMD2 to SMD0  | Set to 100b when transfer data is 7 bits long.                       |
|          |               | Set to 101b when transfer data is 8 bits long.                       |
|          | CKDIR         | Select the internal clock or external clock.                         |
|          | STPS          | Select the stop bit.   |
|          | PRY, PRYE     | Parity detection function disabled                                   |
|          | IOPOL         | Set to 0.  |
| U2C0     | CLK0, CLK1    | Select the U2BRG count source.                                       |
|          | CRS           | $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function disabled |
|          | TXEPT         | Transmit register empty flag   |
|          | CRD           | Set to 0.  |
|          | NCH           | Select TXD2 pin output mode.   |
|          | CKPOL         | Set to 0.  |
|          | UFORM         | Set to 0.  |
| U2C1     | TE            | Set to 1 to enable transmission.                                     |
|          | TI            | Transmit buffer empty flag   |
|          | RE            | Set to 1 to enable reception.  |
|          | RI            | Receive complete flag  |
|          | U2IRS         | Select the UART2 transmit interrupt source.                          |
|          | U2LCH         | Set to 0.  |
|          | U2ERE         | Set to 0.  |
| U2SMR    | b0 to b7      | Set to 0.  |
| U2SMR2   | b0 to b7      | Set to 0.  |
| U2SMR3   | b0 to b7      | Set to 0.  |
| U2SMR4   | b0 to b7      | Set to 0.  |
| U2SMR5   | MP            | Set to 1.  |
|          | MPIE          | Set to 1.  |
| URXDF    | DF2EN         | Select the digital filter enabled or disabled.                       |

## Notes:

1. Set the MPTB bit to 1 when the ID data frame is transmitted. Set this bit to 0 when the data frame is transmitted.
2. If the MPRB bit is set to 1, received D7 to D0 are ID fields. If the MPRB bit is set to 0, received D7 to D0 are data fields.

### 21.6.1 Multiprocessor Transmission

Figure 21.19 shows a Sample Flowchart of Multiprocessor Data Transmission. Set the MPBT bit in the U2TB register to 1 for ID transmission cycles. Set the MPBT bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode).

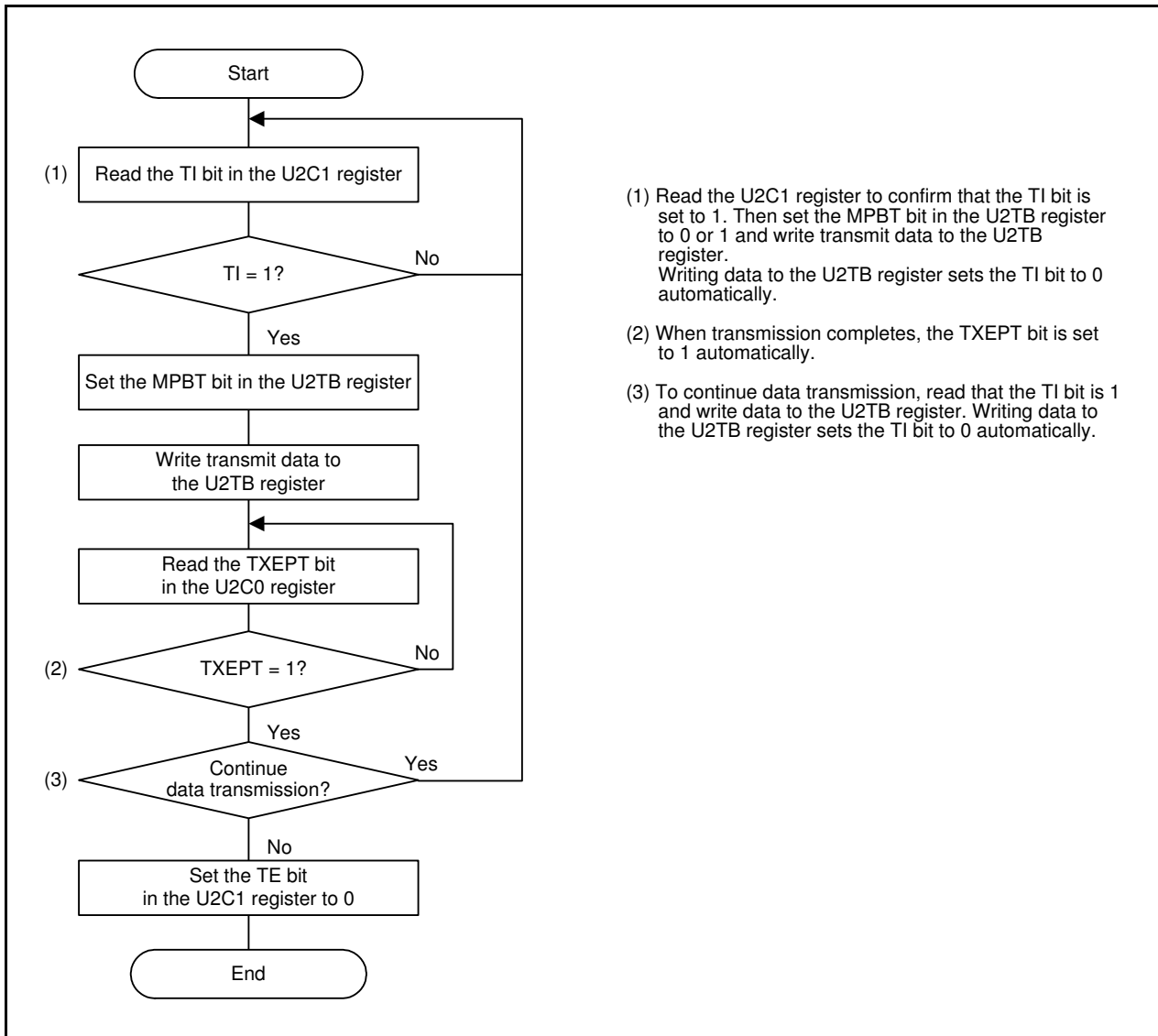
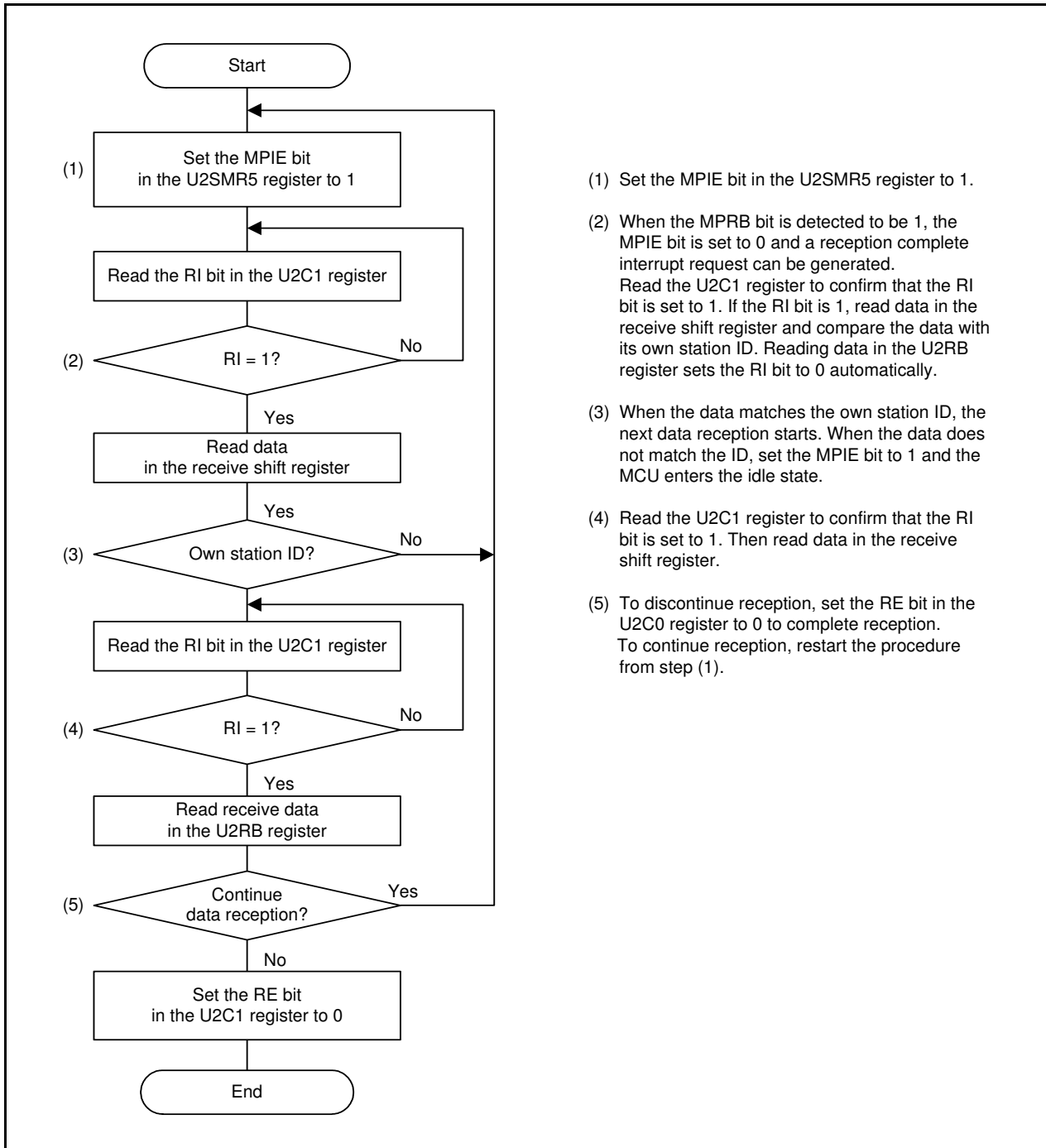


Figure 21.19 Sample Flowchart of Multiprocessor Data Transmission

## 21.6.2 Multiprocessor Reception

Figure 21.20 shows a Sample Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 21.21 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit).



- (1) Set the MPIE bit in the U2SMR5 register to 1.
- (2) When the MPRB bit is detected to be 1, the MPIE bit is set to 0 and a reception complete interrupt request can be generated. Read the U2C1 register to confirm that the RI bit is set to 1. If the RI bit is 1, read data in the receive shift register and compare the data with its own station ID. Reading data in the U2RB register sets the RI bit to 0 automatically.
- (3) When the data matches the own station ID, the next data reception starts. When the data does not match the ID, set the MPIE bit to 1 and the MCU enters the idle state.
- (4) Read the U2C1 register to confirm that the RI bit is set to 1. Then read data in the receive shift register.
- (5) To discontinue reception, set the RE bit in the U2C0 register to 0 to complete reception. To continue reception, restart the procedure from step (1).

Figure 21.20 Sample Flowchart of Multiprocessor Data Reception

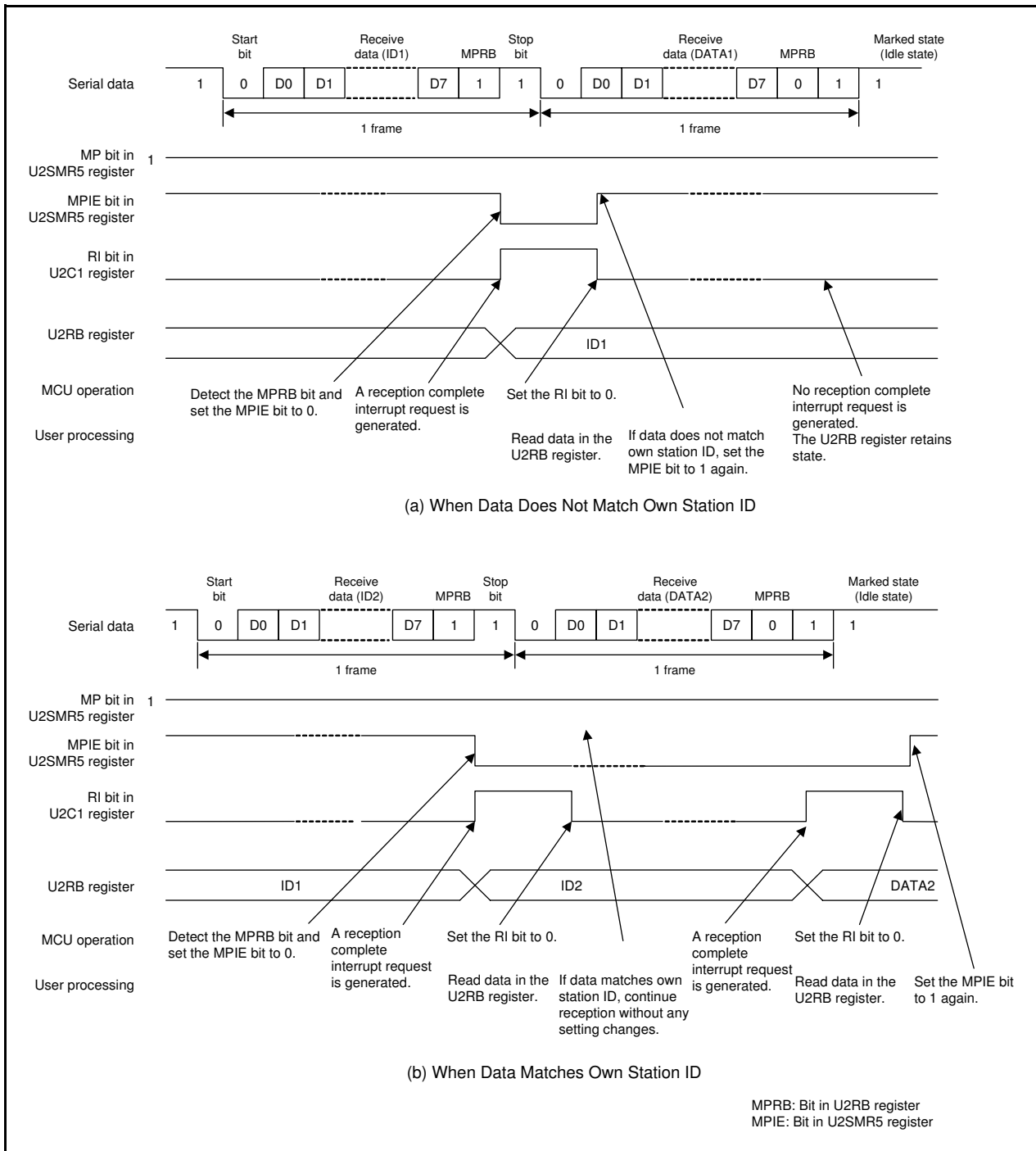


Figure 21.21 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit)

### 21.6.3 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filter enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.

In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise. Figure 21.22 shows a Block Diagram of RXD2 Digital Filter Circuit.

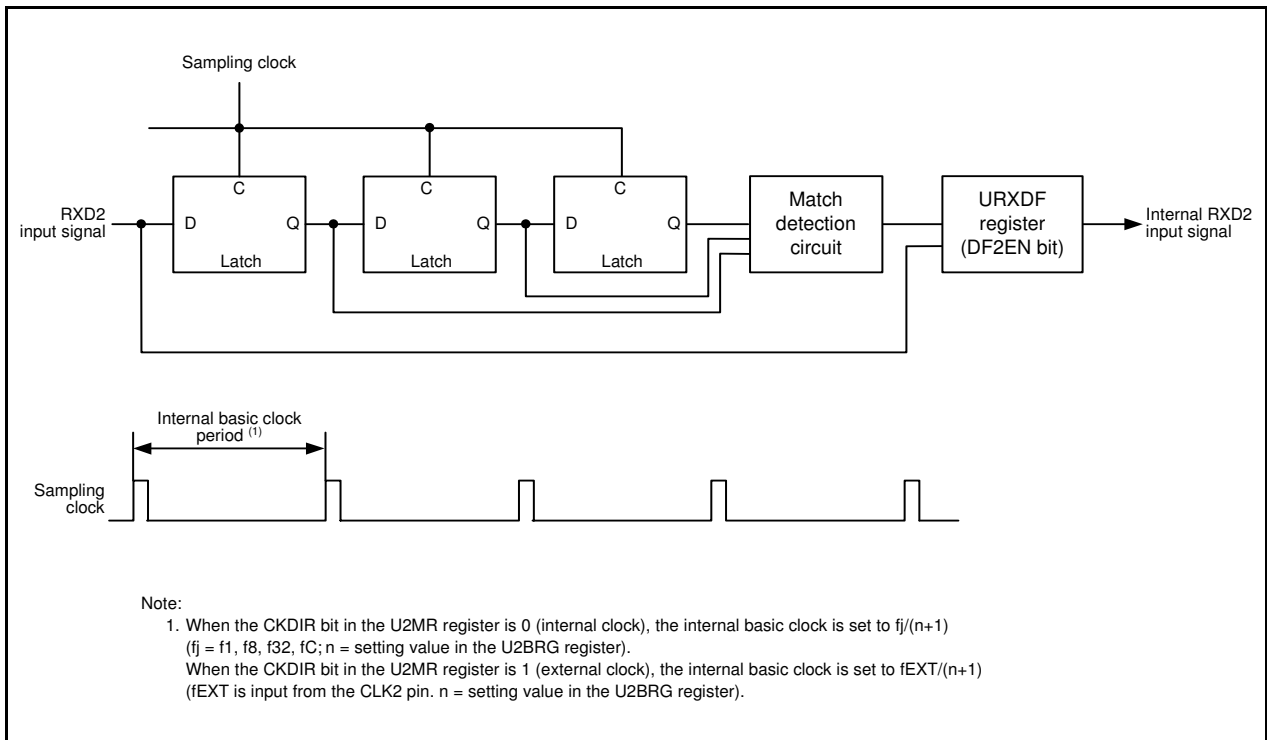


Figure 21.22 Block Diagram of RXD2 Digital Filter Circuit

## 21.7 Notes on Serial Interface (UART2)

### 21.7.1 Clock Synchronous Serial I/O Mode

#### 21.7.1.1 Transmission/Reception

When the  $\overline{\text{RTS}}$  function is used with an external clock, the  $\overline{\text{RTS2}}$  pin outputs “L,” which informs the transmitting side that the MCU is ready for a receive operation. The  $\overline{\text{RTS2}}$  pin outputs “H” when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the  $\overline{\text{RTS2}}$  pin to the  $\overline{\text{CTS2}}$  pin of the transmitting side. The  $\overline{\text{RTS}}$  function is disabled when an internal clock is selected.

#### 21.7.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the  $\overline{\text{CTS}}$  function is selected, input on the  $\overline{\text{CTS2}}$  pin = “L”

#### 21.7.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)



### 21.7.2 Special Mode 1 (I<sup>2</sup>C Mode)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

## 22. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0\_1, P0\_2, P0\_6, P0\_7, and P1\_0 to P1\_3.

### 22.1 Overview

Table 22.1 lists the A/D Converter Performance. Figure 22.1 shows a Block Diagram of A/D Converter.

**Table 22.1 A/D Converter Performance**

| Item  | Performance   |
|---|---|
| A/D conversion method   | Successive approximation (with capacitive coupling amplifier)   |
| Analog input voltage <sup>(1)</sup>                             | 0 V to AVCC   |
| Operating clock $\phi_{AD}$ <sup>(2)</sup>                      | fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8<br>(fAD=f1 or fOCO-F)   |
| Resolution  | 8 bits or 10 bits selectable  |
| Absolute accuracy   | AVCC = Vref = 5 V, $\phi_{AD}$ = 20 MHz<br>• 8-bit resolution $\pm 2$ LSB<br>• 10-bit resolution $\pm 3$ LSB<br>AVCC = Vref = 3.3 V, $\phi_{AD}$ = 16 MHz<br>• 8-bit resolution $\pm 2$ LSB<br>• 10-bit resolution $\pm 5$ LSB<br>AVCC = Vref = 3.0 V, $\phi_{AD}$ = 10 MHz<br>• 8-bit resolution $\pm 2$ LSB<br>• 10-bit resolution $\pm 5$ LSB<br>AVCC = Vref = 2.2 V, $\phi_{AD}$ = 5 MHz<br>• 8-bit resolution $\pm 2$ LSB<br>• 10-bit resolution $\pm 5$ LSB |
| Operating mode  | One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode   |
| Analog input pin  | 8 pins (AN0, AN1, AN5, AN6, AN8 to AN11)  |
| A/D conversion start condition                                  | • Software trigger<br>• Timer RC<br>• External trigger<br>(Refer to <b>22.3.3 A/D Conversion Start Condition.</b> )   |
| Conversion rate per pin<br>( $\phi_{AD} = fAD$ ) <sup>(3)</sup> | Minimum 43 $\phi_{AD}$ cycles   |

Notes:

1. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. Refer to **Table 26.3 A/D Converter Characteristics** for the operating clock  $\phi_{AD}$ .
3. The conversion rate per pin is minimum 43  $\phi_{AD}$  cycles for 8-bit and 10-bit resolution.

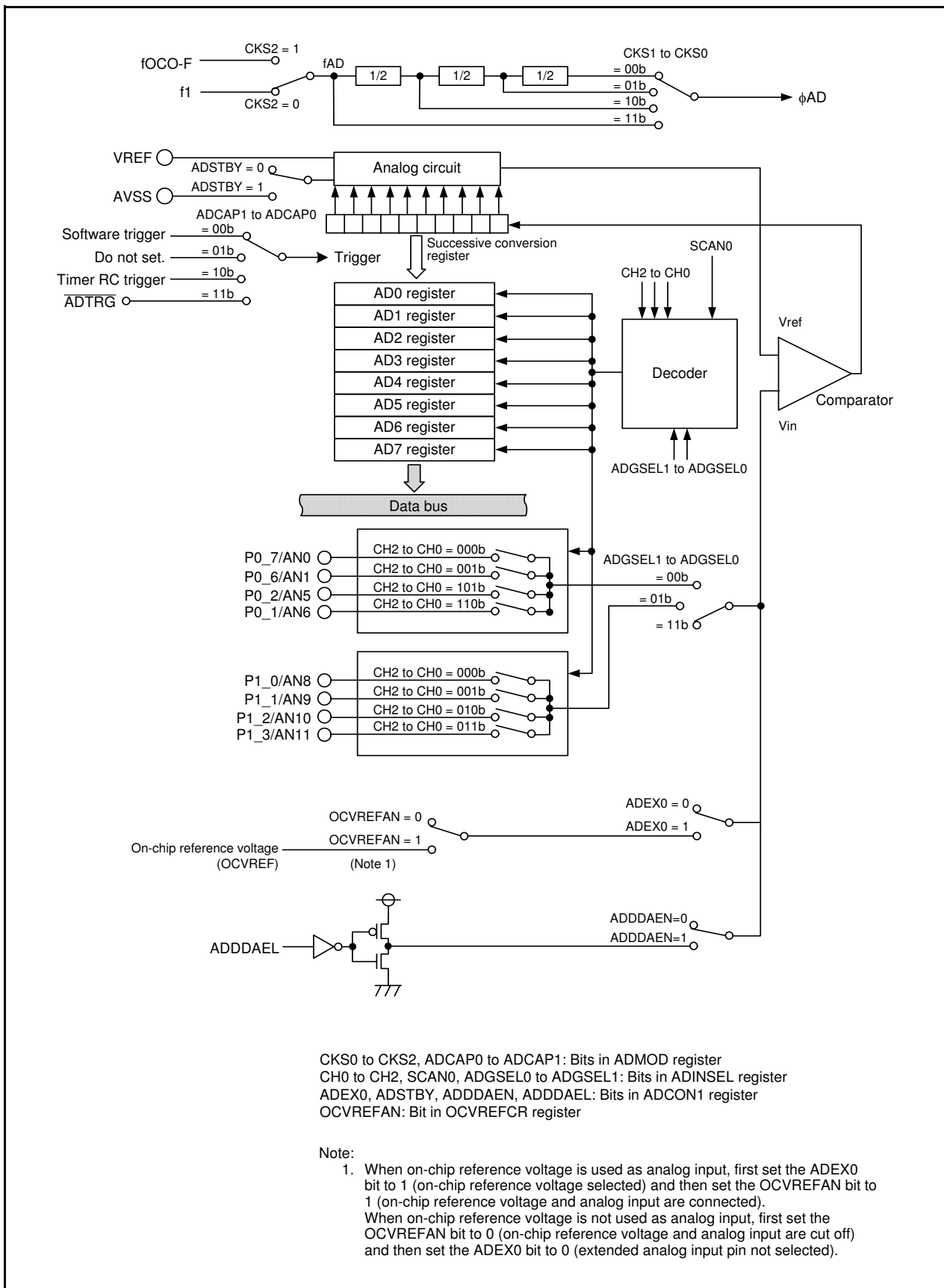


Figure 22.1 Block Diagram of A/D Converter

## 22.2 Registers

### 22.2.1 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

|             |    |    |    |    |    |    |    |          |
|-------------|----|----|----|----|----|----|----|----------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0       |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | OCVREFAN |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0        |

| Bit | Symbol   | Bit Name   | Function   | R/W |
|-----|----------|--|--|-----|
| b0  | OCVREFAN | On-chip reference voltage to analog input connect bit <sup>(1)</sup> | 0: On-chip reference voltage and analog input are cut off<br>1: On-chip reference voltage and analog input are connected | R/W |
| b1  | —        | Reserved bits  | Set to 0.  | R/W |
| b2  | —        |  |  |     |
| b3  | —        |  |  |     |
| b4  | —        |  |  |     |
| b5  | —        |  |  |     |
| b6  | —        |  |  |     |
| b7  | —        |  |  |     |

Note:

- When on-chip reference voltage is used as analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).  
When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.

If the contents of the OCVREFCR register are rewritten during A/D conversion, the conversion result is undefined.

### 22.2.2 A/D Register i (ADi) (i = 0 to 7)

Address 00C1h to 00C0h (AD0), 00C3h to 00C2h (AD1), 00C5h to 00C4h (AD2),  
00C7h to 00C6h (AD3), 00C9h to 00C8h (AD4), 00CBh to 00CAh (AD5),  
00CDh to 00CCh (AD6), 00CFh to 00CEh (AD7)

|             |    |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|----|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | —  |
| After Reset | X  | X  | X  | X  | X  | X  | X  | X  |

|             |     |     |     |     |     |     |    |    |
|-------------|-----|-----|-----|-----|-----|-----|----|----|
| Bit         | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
| Symbol      | —   | —   | —   | —   | —   | —   | —  | —  |
| After Reset | 0   | 0   | 0   | 0   | 0   | 0   | X  | X  |

| Bit | Function  |   | R/W |
|-----|---|---|-----|
|     | 10-Bit Mode<br>(BITS Bit in ADCON1 Register = 1)                          | 8-Bit Mode<br>(BITS Bit in ADCON1 Register = 0) |     |
| b0  | 8 low-order bits in A/D conversion result                                 | A/D conversion result                           | R   |
| b1  |   |   |     |
| b2  |   |   |     |
| b3  |   |   |     |
| b4  |   |   |     |
| b5  |   |   |     |
| b6  |   |   |     |
| b7  |   |   |     |
| b8  | 2 high-order bits in A/D conversion result                                | When read, the content is 0.                    | R   |
| b9  |   |   |     |
| b10 | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b11 |   |   |     |
| b12 |   |   |     |
| b13 |   |   |     |
| b14 |   |   |     |
| b15 | Reserved bit  | When read, the content is undefined.            | R   |

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.

When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

### 22.2.3 A/D Mode Register (ADMOD)

Address 00D4h

|             |        |        |     |     |     |      |      |      |
|-------------|--------|--------|-----|-----|-----|------|------|------|
| Bit         | b7     | b6     | b5  | b4  | b3  | b2   | b1   | b0   |
| Symbol      | ADCAP1 | ADCAP0 | MD2 | MD1 | MD0 | CKS2 | CKS1 | CKS0 |
| After Reset | 0      | 0      | 0   | 0   | 0   | 0    | 0    | 0    |

| Bit | Symbol | Bit Name                          | Function   | R/W |
|-----|--------|-----------------------------------|--|-----|
| b0  | CKS0   | Division select bit               | <sup>b1 b0</sup><br>0 0: fAD divided by 8<br>0 1: fAD divided by 4<br>1 0: fAD divided by 2<br>1 1: fAD divided by 1 (no division)   | R/W |
| b1  | CKS1   |                                   |  | R/W |
| b2  | CKS2   | Clock source select bit (1)       | 0: Selects f1<br>1: Selects fOCO-F   | R/W |
| b3  | MD0    | A/D operating mode select bit     | <sup>b5 b4 b3</sup><br>0 0 0: One-shot mode<br>0 0 1: Do not set.<br>0 1 0: Repeat mode 0<br>0 1 1: Repeat mode 1<br>1 0 0: Single sweep mode<br>1 0 1: Do not set.<br>1 1 0: Repeat sweep mode<br>1 1 1: Do not set.  | R/W |
| b4  | MD1    |                                   |  | R/W |
| b5  | MD2    |                                   |  | R/W |
| b6  | ADCAP0 | A/D conversion trigger select bit | <sup>b7 b6</sup><br>0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register)<br>0 1: Do not set.<br>1 0: A/D conversion starts by conversion trigger from timer RC<br>1 1: A/D conversion starts by external trigger ( $\overline{\text{ADTRG}}$ ) | R/W |
| b7  | ADCAP1 |                                   |  | R/W |

Note:

- When the CKS2 bit is changed, wait for 3  $\phi$ AD cycles or more before starting A/D conversion.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

### 22.2.4 A/D Input Select Register (ADINSEL)

Address 00D5h

|             |         |         |    |       |    |     |     |     |
|-------------|---------|---------|----|-------|----|-----|-----|-----|
| Bit         | b7      | b6      | b5 | b4    | b3 | b2  | b1  | b0  |
| Symbol      | ADGSEL1 | ADGSEL0 | —  | SCAN0 | —  | CH2 | CH1 | CH0 |
| After Reset | 1       | 1       | 0  | 0     | 0  | 0   | 0   | 0   |

| Bit | Symbol  | Bit Name                       | Function   | R/W |
|-----|---------|--------------------------------|--|-----|
| b0  | CH0     | Analog input pin select bit    | Refer to <b>Table 22.2 Analog Input Pin Selection</b>  | R/W |
| b1  | CH1     |                                |  | R/W |
| b2  | CH2     |                                |  | R/W |
| b3  | —       | Reserved bit                   | Set to 0.  | R/W |
| b4  | SCAN0   | A/D sweep pin count select bit | 0: 2 pins<br>1: 4 pins <sup>(1)</sup>  | R/W |
| b5  | —       | Reserved bit                   | Set to 0.  | R/W |
| b6  | ADGSEL0 | A/D input group select bit     | <sup>b7 b6</sup><br>0 0: Port P0 group selected<br>0 1: Port P1 group selected<br>1 0: Do not set.<br>1 1: Port group not selected | R/W |
| b7  | ADGSEL1 |                                |  | R/W |

Note:

- Set bits ADGSEL1 to ADGSEL0 to 01b (port P1 group selected) when the SCAN0 bit is set to 1 (4 pins).

If the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

**Table 22.2 Analog Input Pin Selection**

| Bits CH2 to CH0 | Bits ADGSEL1, ADGSEL0 = 00b | Bits ADGSEL1, ADGSEL0 = 01b |
|-----------------|-----------------------------|-----------------------------|
| 000b            | AN0                         | AN8                         |
| 001b            | AN1                         | AN9                         |
| 010b            | Do not set.                 | AN10                        |
| 011b            | Do not set.                 | AN11                        |
| 100b            | Do not set.                 | Do not set.                 |
| 101b            | AN5                         |                             |
| 110b            | AN6                         |                             |
| 111b            | Do not set.                 |                             |

### 22.2.5 A/D Control Register 0 (ADCON0)

Address 00D6h

|             |    |    |    |    |    |    |    |      |
|-------------|----|----|----|----|----|----|----|------|
| Bit         | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0   |
| Symbol      | —  | —  | —  | —  | —  | —  | —  | ADST |
| After Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0    |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | ADST   | A/D conversion start flag   | 0: Stop A/D conversion<br>1: Start A/D conversion | R/W |
| b1  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b2  | —      |   |   |     |
| b3  | —      |   |   |     |
| b4  | —      |   |   |     |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      |   |   |     |

#### ADST Bit (A/D conversion start flag)

[Conditions for setting to 1]

When A/D conversion starts and while A/D conversion is in progress.

[Condition for setting to 0]

When A/D conversion stops.



## 22.2.6 A/D Control Register 1 (ADCON1)

Address 00D7h

|             |         |         |        |      |    |    |    |       |
|-------------|---------|---------|--------|------|----|----|----|-------|
| Bit         | b7      | b6      | b5     | b4   | b3 | b2 | b1 | b0    |
| Symbol      | ADDDAEL | ADDDAEN | ADSTBY | BITS | —  | —  | —  | ADEX0 |
| After Reset | 0       | 0       | 0      | 0    | 0  | 0  | 0  | 0     |

| Bit | Symbol  | Bit Name  | Function  | R/W |
|-----|---------|---|---|-----|
| b0  | ADEX0   | Extended analog input pin select bit <sup>(1)</sup>                     | 0: Extended analog input pin not selected<br>1: On-chip reference voltage selected <sup>(2, 5, 6)</sup> | R/W |
| b1  | —       | Reserved bits   | Set to 0.   | R/W |
| b2  | —       |   |   |     |
| b3  | —       |   |   |     |
| b4  | BITS    |   |   |     |
| b5  | ADSTBY  | A/D standby bit <sup>(3)</sup>  | 0: A/D operation stops (standby)<br>1: A/D operation enabled  | R/W |
| b6  | ADDDAEN | A/D open-circuit detection assist function enable bit <sup>(4, 6)</sup> | 0: Disabled<br>1: Enabled   | R/W |
| b7  | ADDDAEL | A/D open-circuit detection assist method select bit <sup>(4)</sup>      | 0: Discharge before conversion<br>1: Precharge before conversion  | R/W |

## Notes:

- When on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).  
When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
- Do not set to 1 (A/D conversion using comparison reference voltage as input) in single sweep mode or repeat sweep mode.
- When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1  $\phi$ AD cycle or more before starting A/D conversion.
- To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).  
The conversion result with an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
- When on-chip reference voltage is used (ADEX0 = 1), set bits CH2 to CH0 in the ADINSEL register to 000b.
- When on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

## 22.3 Common Items for Multiple Modes

### 22.3.1 Input/Output Pins

The analog input shares pins P0\_1, P0\_2, P0\_6, P0\_7, and P1\_0 to P1\_3 in AN0, AN1, AN5, AN6, and AN8 to AN11.

When using the AN<sub>i</sub> (i = 0 to 1, 5 to 6, 8 to 11) pin as input, set the corresponding port direction bit to 0 (input mode).

After changing the A/D operating mode, select an analog input pin again.

### 22.3.2 A/D Conversion Cycles

Figure 22.2 shows a Timing Diagram of A/D Conversion. Figure 22.3 shows the A/D Conversion Cycles ( $\phi_{AD} = f_{AD}$ ).

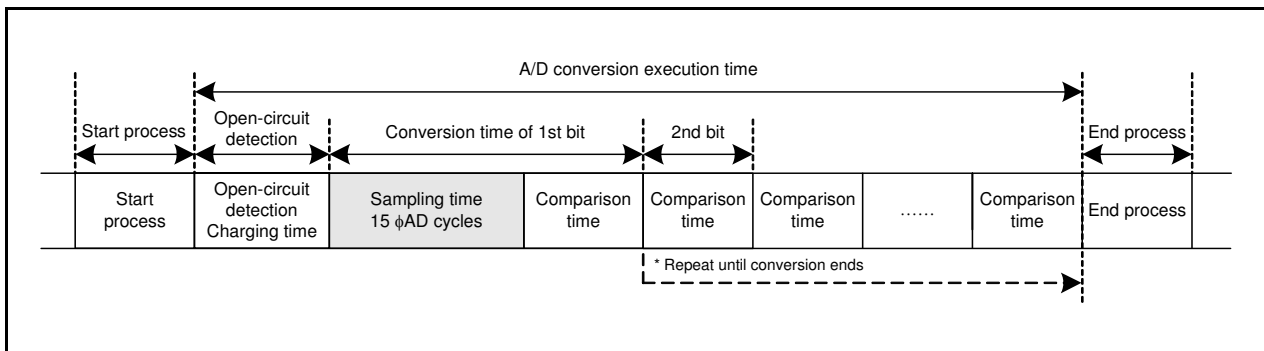


Figure 22.2 Timing Diagram of A/D Conversion

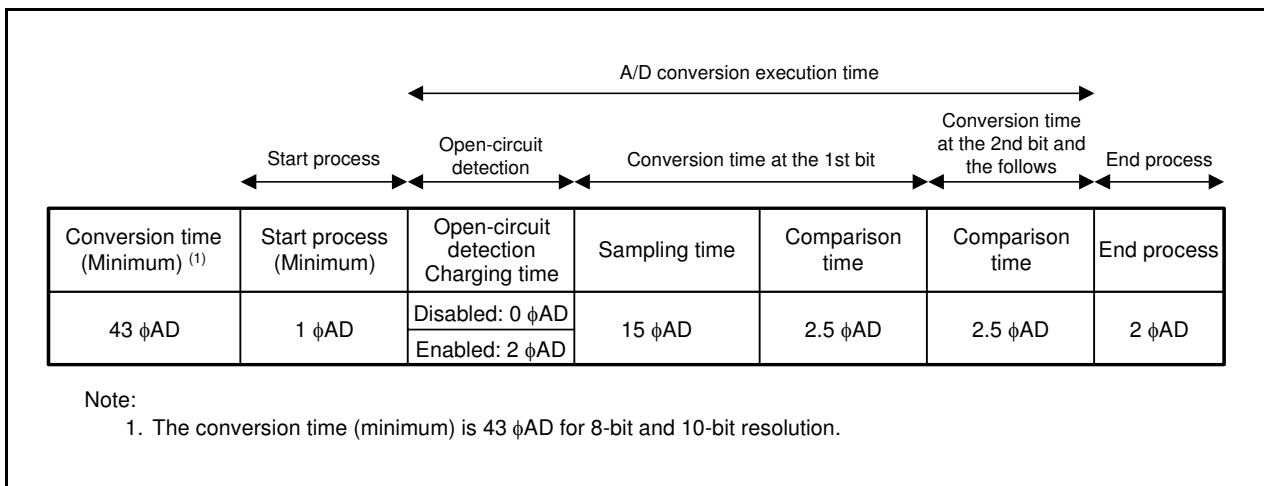


Figure 22.3 A/D Conversion Cycles ( $\phi_{AD} = f_{AD}$ )

Table 22.3 shows the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows.

The start process time varies depending on which  $\phi_{AD}$  is selected.

When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).

In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.

In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register.

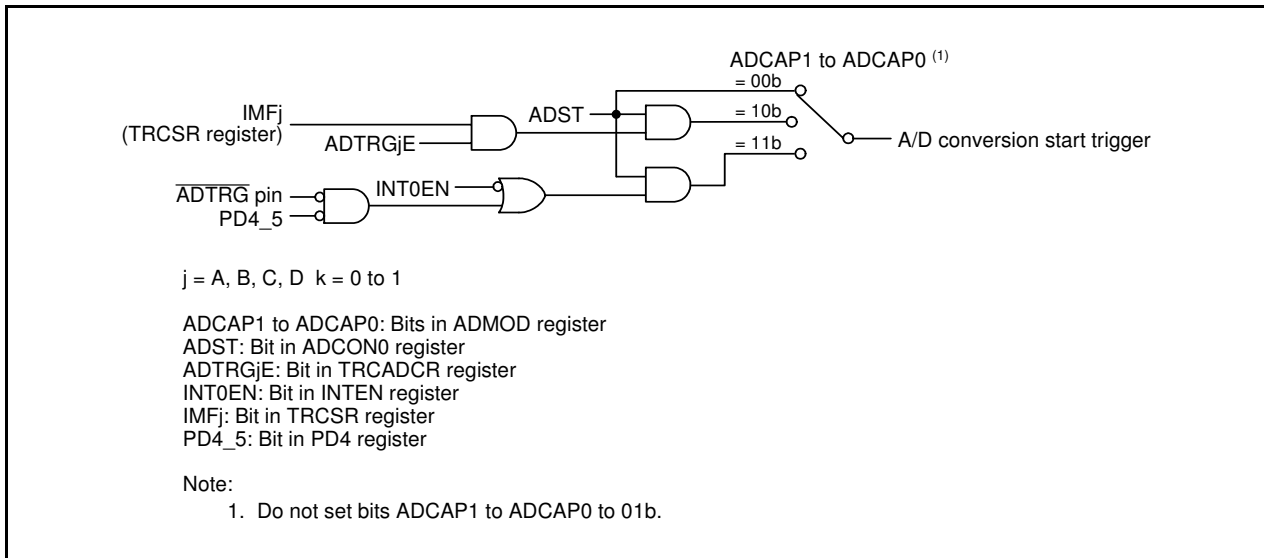
- In on-shot mode  
Start process time + A/D conversion execution time + end process time
- When two pins are selected in single sweep mode  
Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

**Table 22.3 Number of Cycles for A/D Conversion Items**

| A/D Conversion Item            |                                   | Number of Cycles       |
|--------------------------------|-----------------------------------|------------------------|
| Start process time             | $\phi_{AD} = f_{AD}$              | 1 or 2 $f_{AD}$ cycles |
|                                | $\phi_{AD} = f_{AD}$ divided by 2 | 2 or 3 $f_{AD}$ cycles |
|                                | $\phi_{AD} = f_{AD}$ divided by 4 | 3 or 4 $f_{AD}$ cycles |
|                                | $\phi_{AD} = f_{AD}$ divided by 8 | 5 or 6 $f_{AD}$ cycles |
| A/D conversion execution time  | Open-circuit detection disabled   | 40 $\phi_{AD}$ cycles  |
|                                | Open-circuit detection enabled    | 42 $\phi_{AD}$ cycles  |
| Between-execution process time |                                   | 1 $\phi_{AD}$ cycle    |
| End process time               |                                   | 2 or 3 $f_{AD}$ cycles |

### 22.3.3 A/D Conversion Start Condition

A software trigger, trigger from timer RC, and external trigger are used as A/D conversion start triggers. Figure 22.4 shows the Block Diagram of A/D Conversion Start Control Unit.



**Figure 22.4** Block Diagram of A/D Conversion Start Control Unit

#### 22.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger).

The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

#### 22.3.3.2 Trigger from Timer RC

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC). To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, PWM2 mode).
- The ADTRG<sub>jE</sub> bit ( $j = A, B, C, D$ ) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGR<sub>j</sub> register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMF<sub>j</sub> bit in the TRCSR register is changed from 0 to 1, A/D conversion starts.

Refer to **18. Timer RC**, **18.5 Timer Mode (Output Compare Function)**, **18.6 PWM Mode**, **18.7 PWM2 Mode** for the details of timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

### 22.3.3.3 External Trigger

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ( $\overline{\text{ADTRG}}$ )).

To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ( $\overline{\text{ADTRG}}$ )).
- Set the INT0EN bit in the INTEN register to 1 ( $\overline{\text{INT0}}$  input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- The PD4\_5 bit in the PD4 register is set to 0 (input mode).
- Select the  $\overline{\text{INT0}}$  digital filter by bits INT0F1 to INT0F0 in the INTF register.
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register and a change in the  $\overline{\text{ADTRG}}$  pin input (refer to **11.8 Notes on Interrupts**).

For details on interrupts, refer to **11. Interrupts**.

When the  $\overline{\text{ADTRG}}$  pin input is changed from “H” to “L” under the above conditions, A/D conversion starts.

### 22.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after a reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.

In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).

However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.

If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

### 22.3.5 Low Current Consumption Function

When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for 1  $\phi$ AD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.

Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during A/D conversion.

### 22.3.6 On-Chip Reference Voltage (OCVREF)

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.

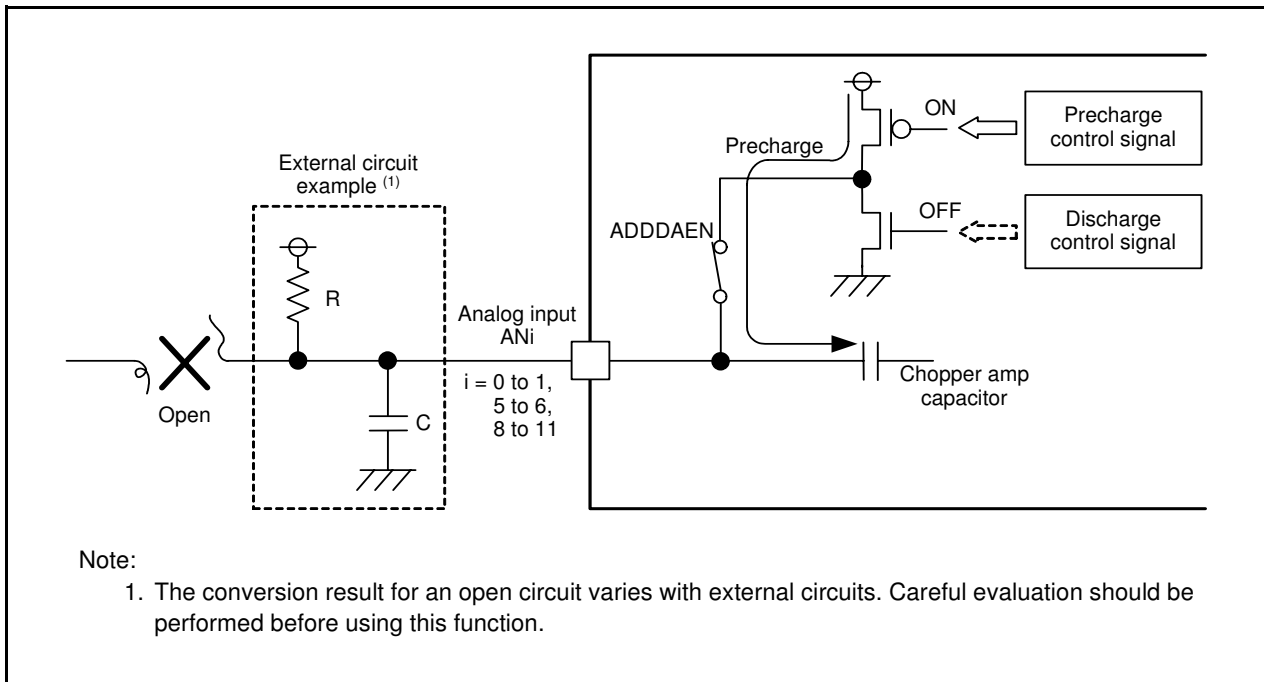
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.

The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

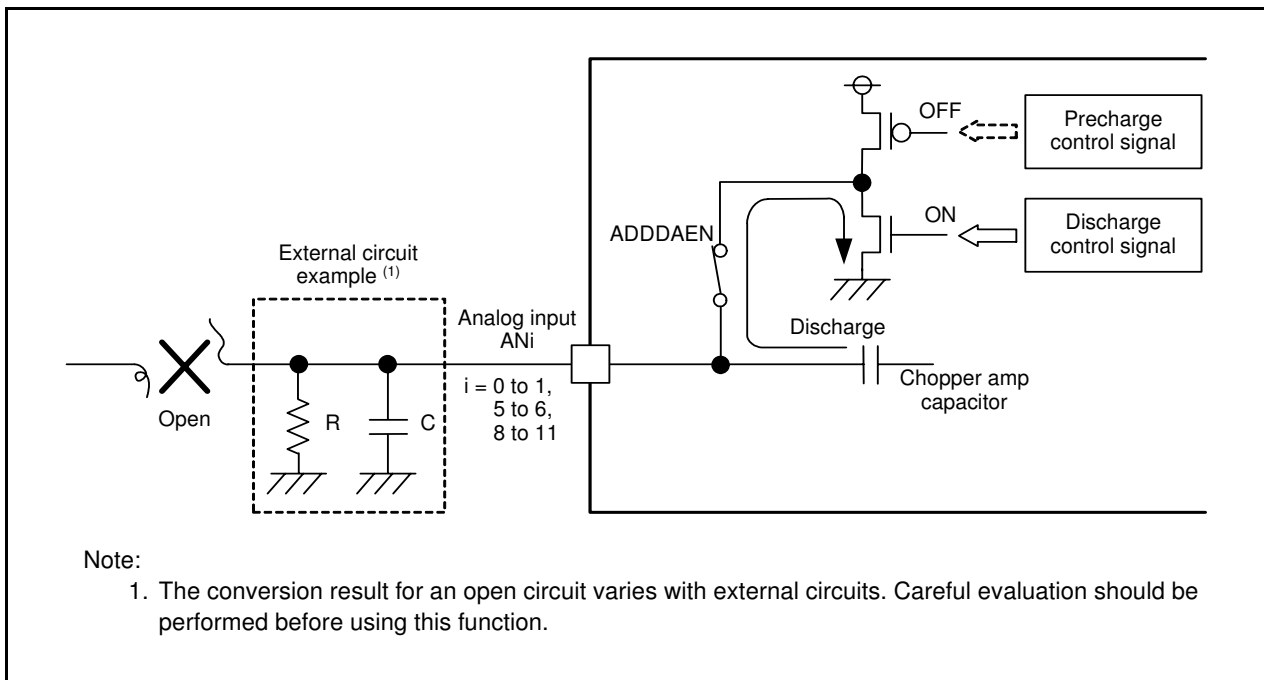
### 22.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.

This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins. Figure 22.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 22.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).



**Figure 22.5 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected)**



**Figure 22.6 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected)**

## 22.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0, AN1, AN5, AN6, AN8 to AN11 or OCVREF is A/D converted once.

Table 22.4 lists the One-Shot Mode Specifications.

**Table 22.4 One-Shot Mode Specifications**

| Item                                       | Specification  |
|--|--|
| Function                                   | The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted once.  |
| Resolution                                 | 8 bits or 10 bits  |
| A/D conversion start condition             | <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Timer RC</li> <li>• External trigger</li> </ul> (Refer to <b>22.3.3 A/D Conversion Start Condition</b> )  |
| A/D conversion stop condition              | <ul style="list-style-type: none"> <li>• A/D conversion completes (If bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.)</li> <li>• Set the ADST bit to 0</li> </ul> |
| Interrupt request generation timing        | When A/D conversion completes  |
| Analog input pin                           | One pin selectable from among AN0, AN1, AN5, AN6, AN8 to AN11, or OCVREF.  |
| Storage register for A/D conversion result | AD0 register: AN0, AN8, OCVREF<br>AD1 register: AN1, AN9<br>AD2 register: AN10<br>AD3 register: AN11<br>AD5 register: AN5<br>AD6 register: AN6   |
| Reading of result of A/D converter         | Read register AD0 to AD3, AD5, AD6 corresponding to the selected pin.  |



## 22.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0, AN1, AN5, AN6, AN8 to AN11 or OCVREF is A/D converted repeatedly.

Table 22.5 lists the Repeat Mode 0 Specifications.

**Table 22.5 Repeat Mode 0 Specifications**

| Item                                       | Specification   |
|--|---|
| Function                                   | The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly. |
| Resolution                                 | 8 bits or 10 bits   |
| A/D conversion start condition             | <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Timer RC</li> <li>• External trigger</li> </ul> (Refer to <b>22.3.3 A/D Conversion Start Condition</b> )     |
| A/D conversion stop condition              | Set the ADST bit in the ADCON0 register to 0  |
| Interrupt request generation timing        | Not generated   |
| Analog input pin                           | One pin selectable from among AN0, AN1, AN5, AN6, AN8 to AN11, or OCVREF.   |
| Storage register for A/D conversion result | AD0 register: AN0, AN8, OCVREF<br>AD1 register: AN1, AN9<br>AD2 register: AN10<br>AD3 register: AN11<br>AD5 register: AN5<br>AD6 register: AN6                                    |
| Reading of result of A/D converter         | Read register AD0 to AD3, AD5, AD6 corresponding to the selected pin.   |

## 22.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0, AN1, AN5, AN6, AN8 to AN11 or OCVREF is A/D converted repeatedly.

Table 22.6 lists the Repeat Mode 1 Specifications. Figure 22.7 shows the Operating Example of Repeat Mode 1.

**Table 22.6 Repeat Mode 1 Specifications**

| Item                                       | Specification   |
|--|---|
| Function                                   | The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.   |
| Resolution                                 | 8 bits or 10 bits   |
| A/D conversion start condition             | <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Timer RC</li> <li>• External trigger</li> </ul> (Refer to <b>22.3.3 A/D Conversion Start Condition</b> )   |
| A/D conversion stop condition              | Set the ADST bit in the ADCON0 register to 0  |
| Interrupt request generation timing        | When the A/D conversion result is stored in the AD7 register.   |
| Analog input pin                           | One pin selectable from among AN0, AN1, AN5, AN6, AN8 to AN11, or OCVREF.   |
| Storage register for A/D conversion result | AD0 register: 1st A/D conversion result, 9th A/D conversion result...<br>AD1 register: 2nd A/D conversion result, 10th A/D conversion result...<br>AD2 register: 3rd A/D conversion result, 11th A/D conversion result...<br>AD3 register: 4th A/D conversion result, 12th A/D conversion result...<br>AD4 register: 5th A/D conversion result, 13th A/D conversion result...<br>AD5 register: 6th A/D conversion result, 14th A/D conversion result...<br>AD6 register: 7th A/D conversion result, 15th A/D conversion result...<br>AD7 register: 8th A/D conversion result, 16th A/D conversion result... |
| Reading of result of A/D converter         | Read registers AD0 to AD7   |

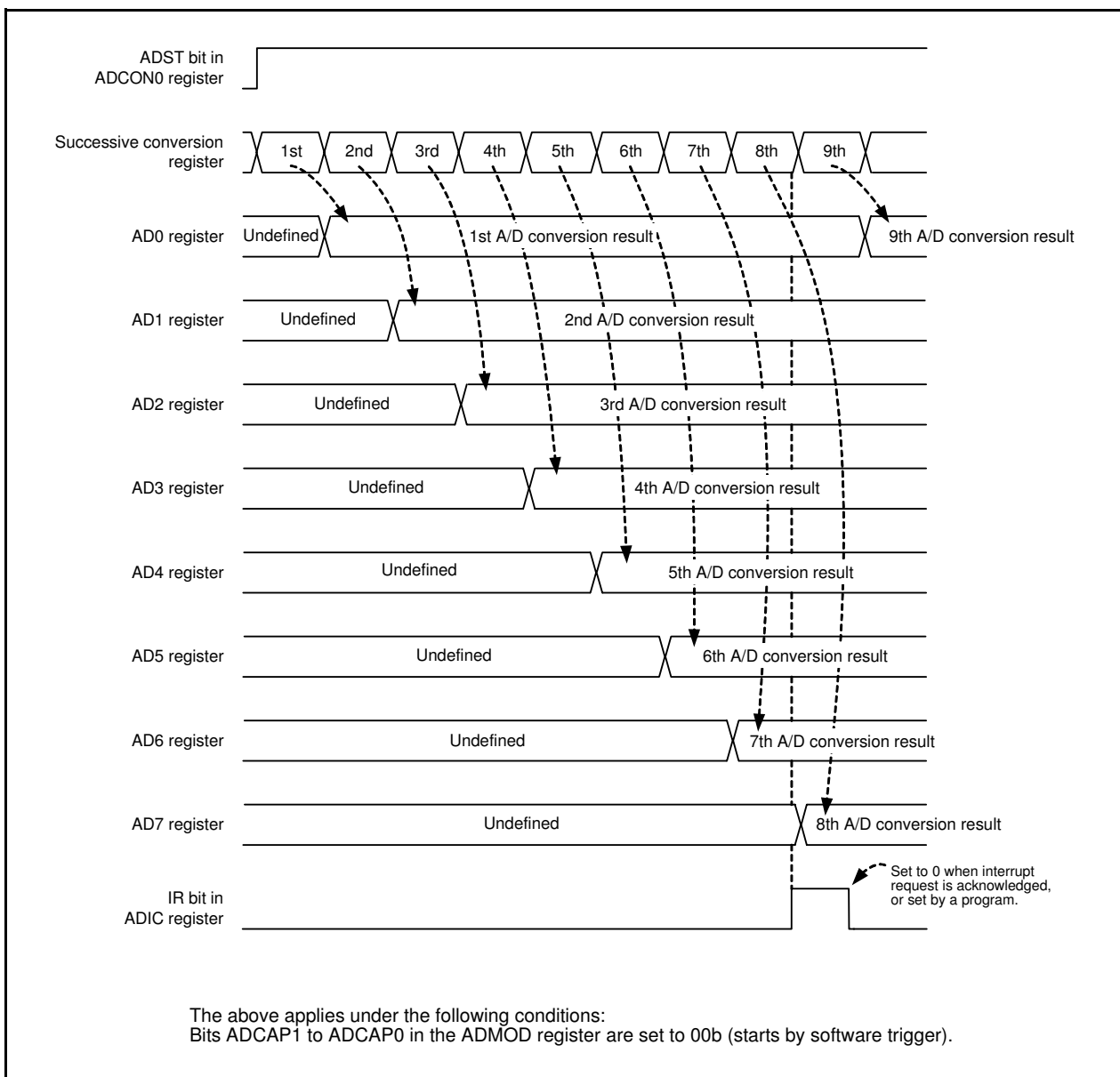


Figure 22.7 Operating Example of Repeat Mode 1

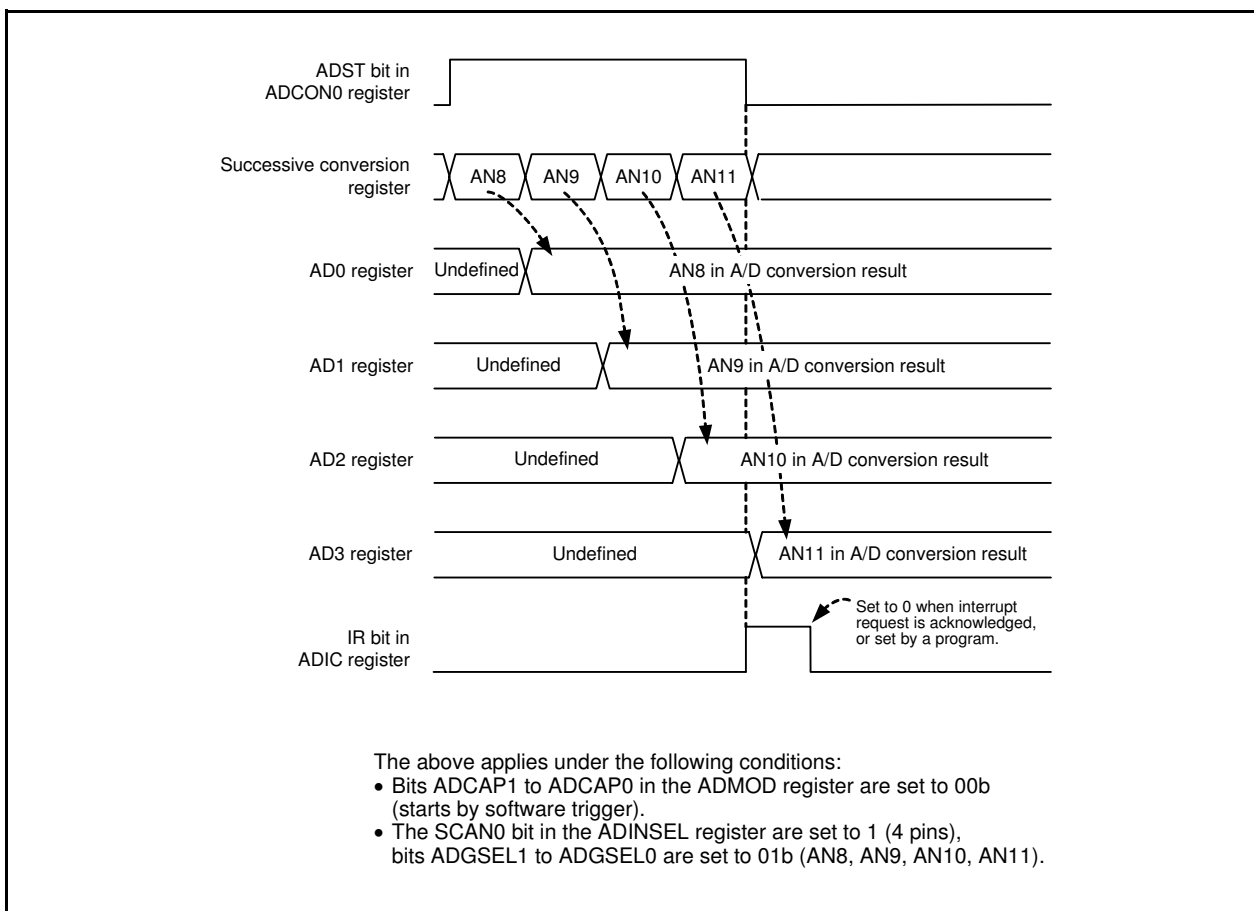
## 22.7 Single Sweep Mode

In single sweep mode, the input voltage to two or four pins selected from among AN0, AN1, AN8 to AN11 are A/D converted once.

Table 22.7 lists the Single Sweep Mode Specifications. Figure 22.8 shows the Operating Example of Single Sweep Mode.

**Table 22.7 Single Sweep Mode Specifications**

| Item                                       | Specification   |
|--|---|
| Function                                   | The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and the SCAN0 bit in the ADINSEL register is A/D converted once.  |
| Resolution                                 | 8 bits or 10 bits   |
| A/D conversion start condition             | <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Timer RC</li> <li>• External trigger</li> </ul> (Refer to <b>22.3.3 A/D Conversion Start Condition</b> )   |
| A/D conversion stop condition              | <ul style="list-style-type: none"> <li>• If two pins are selected, when A/D conversion of the two selected pins completes (the ADST bit in the ADCON0 register is set to 0).</li> <li>• If four pins are selected, when A/D conversion of the four selected pins completes (the ADST bit is set to 0).</li> <li>• Set the ADST bit to 0.</li> </ul> |
| Interrupt request generation timing        | <ul style="list-style-type: none"> <li>• If two pins are selected, when A/D conversion of the two selected pins completes.</li> <li>• If four pins are selected, when A/D conversion of the four selected pins completes.</li> </ul>  |
| Analog input pin                           | AN0 to AN1(2 pins), AN8 to AN9(2 pins), AN8 to AN11(4 pins),<br>(Selectable by the SCAN0 bit and bits ADGSEL1 to ADGSEL0.)  |
| Storage register for A/D conversion result | AD0 register: AN0, AN8<br>AD1 register: AN1, AN9<br>AD2 register: AN10<br>AD3 register: AN11  |
| Reading of result of A/D converter         | Read the registers from AD0 to AD3 corresponding to the selected pin.   |



**Figure 22.8** Operating Example of Single Sweep Mode

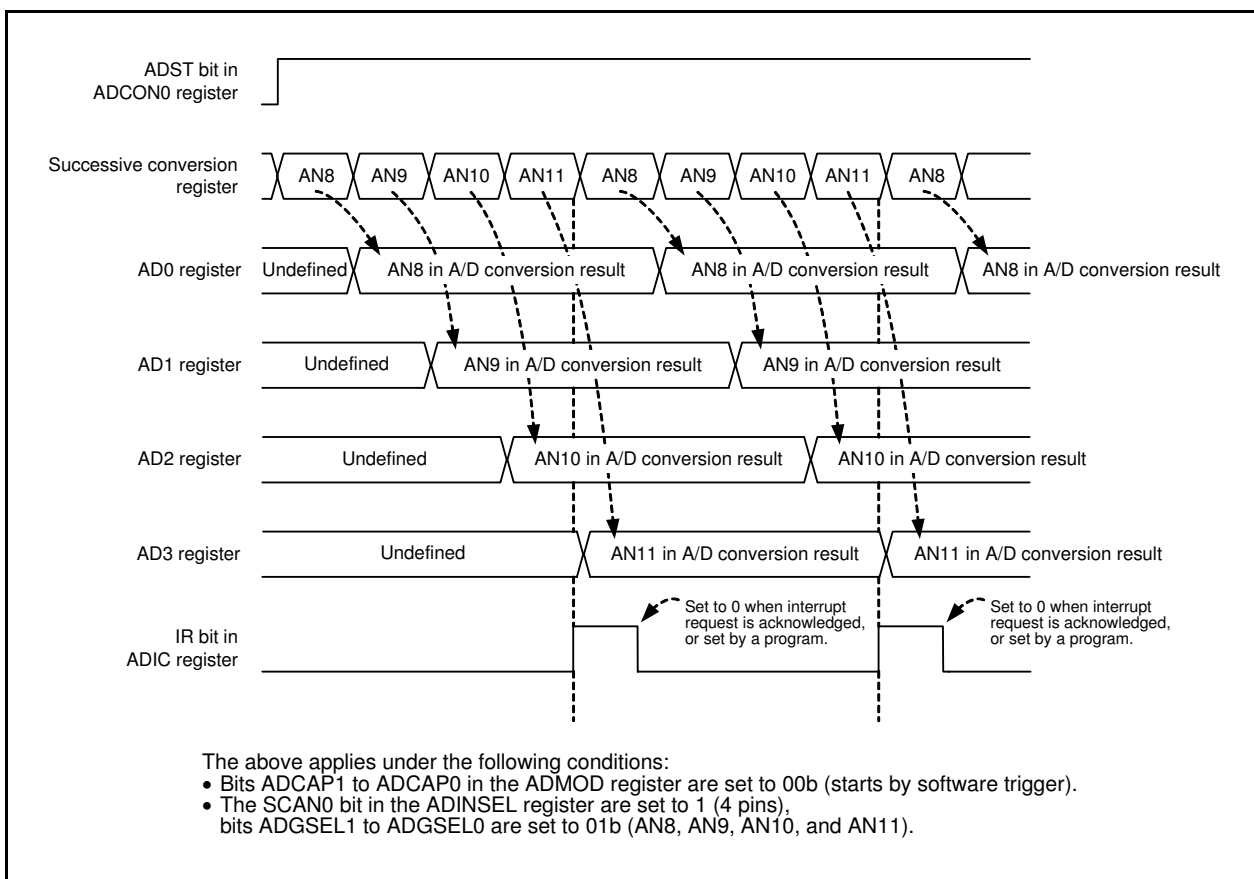
## 22.8 Repeat Sweep Mode

In repeat sweep mode, the input voltage to two or four pins selected from among AN0, AN1, AN8 to AN11 are A/D converted repeatedly.

Table 22.8 lists the Repeat Sweep Mode Specifications. Figure 22.9 shows the Operating Example of Repeat Sweep Mode.

**Table 22.8 Repeat Sweep Mode Specifications**

| Item                                       | Specification  |
|--|--|
| Function                                   | The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and the SCAN0 bit in the ADINSEL register are A/D converted repeatedly.  |
| Resolution                                 | 8 bits or 10 bits  |
| A/D conversion start condition             | <ul style="list-style-type: none"> <li>• Software trigger</li> <li>• Timer RC</li> <li>• External trigger</li> </ul> (Refer to <b>22.3.3 A/D Conversion Start Condition</b> )  |
| A/D conversion stop condition              | Set the ADST bit in the ADCON0 register to 0   |
| Interrupt request generation timing        | <ul style="list-style-type: none"> <li>• If two pins are selected, when A/D conversion of the two selected pins completes.</li> <li>• If four pins are selected, when A/D conversion of the four selected pins completes.</li> </ul> |
| Analog input pin                           | AN0 to AN1(2 pins), AN8 to AN9(2 pins), AN8 to AN11(4 pins),<br>(Selectable by the SCAN0 bit and bits ADGSEL1 to ADGSEL0.)   |
| Storage register for A/D conversion result | AD0 register: AN0, AN8<br>AD1 register: AN1, AN9<br>AD2 register: AN10<br>AD3 register: AN11   |
| Reading of result of A/D converter         | Read the registers from AD0 to AD3 corresponding to the selected pin.  |



**Figure 22.9** Operating Example of Repeat Sweep Mode

## 22.9 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 22.10 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

$$VC \text{ is generally } VC = VIN \left\{ 1 - e^{-\frac{1}{C(R0 + R)} t} \right\}$$

$$\text{And when } t = T, \quad VC = VIN - \frac{X}{Y} VIN = VIN \left( 1 - \frac{X}{Y} \right)$$

$$e^{-\frac{1}{C(R0 + R)} T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0 + R)} T = \ln \frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \cdot \ln \frac{X}{Y}} - R$$

Figure 22.10 shows Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN - (0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.

T = 0.75 μs when φAD = 20 MHz. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.75 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = \frac{0.75 \times 10^{-6}}{6.0 \times 10^{-12} \cdot \ln \frac{0.1}{1024}} - 10 \times 10^3 \approx 3.5 \times 10^3$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 3.5 kΩ maximum.

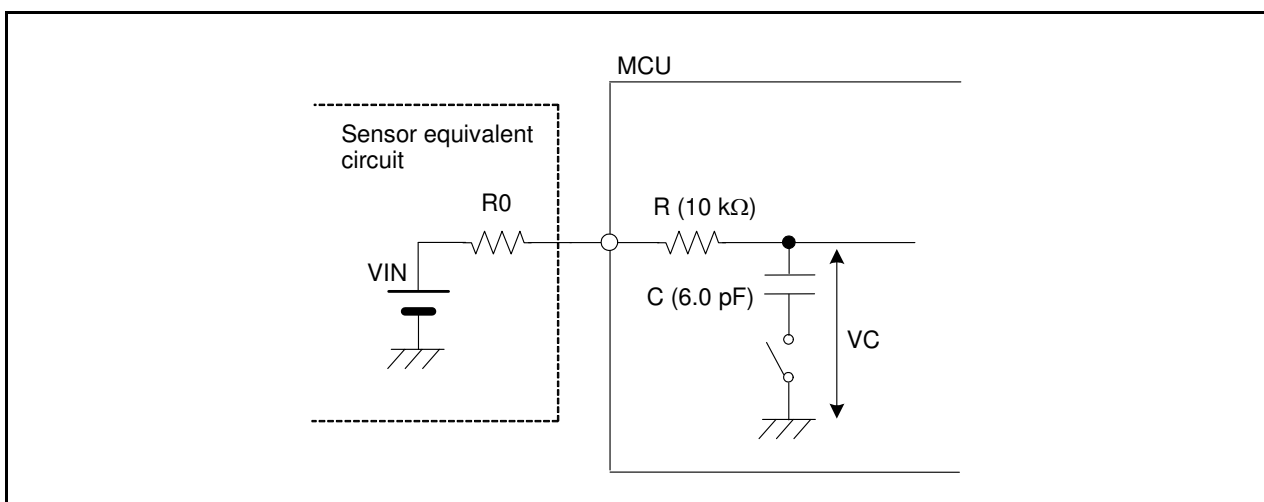


Figure 22.10 Analog Input Pin and External Sensor Equivalent Circuit



## 22.10 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock  $\phi_{AD}$  or more for the CPU clock during A/D conversion.  
Do not select fOCO-F as  $\phi_{AD}$ .
- Connect 0.1  $\mu$ F capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined. If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

## 23. Comparator B

Comparator B compares a reference input voltage and an analog input voltage. Comparator B1 and comparator B3 are independent of each other.

### 23.1 Overview

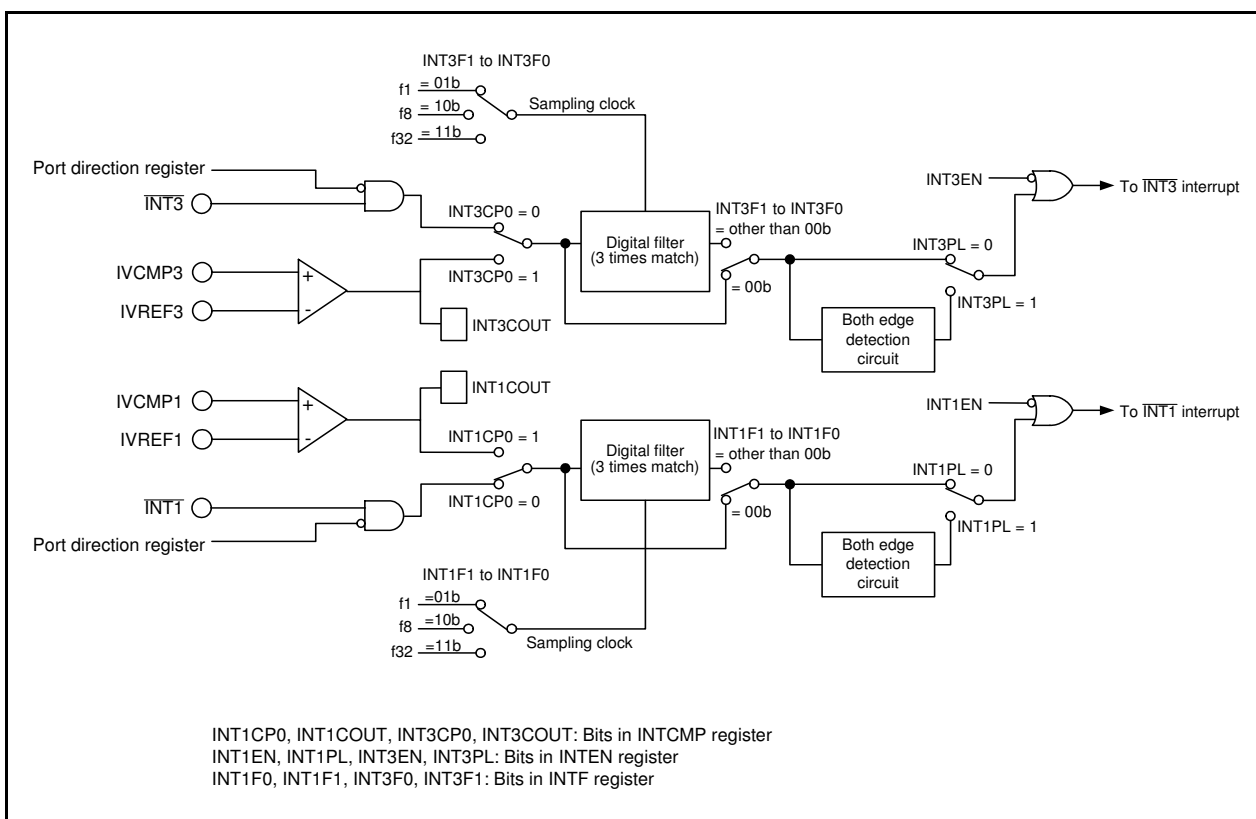
The comparison result of the reference input voltage and analog input voltage can be read by software. An input to the IVREFi (i = 1 or 3) pin can be used as the reference input voltage.

Table 23.1 lists the Comparator B Specifications, Figure 23.1 shows a Comparator B Block Diagram, and Table 23.2 lists the I/O Pins.

**Table 23.1 Comparator B Specifications**

| Item                                | Specification  |
|-------------------------------------|--|
| Analog input voltage                | Input voltage to the IVCMPi pin  |
| Reference input voltage             | Input voltage to the IVREFi pin  |
| Comparison result                   | Read from the INTiCOUT bit in the INTCMP register  |
| Interrupt request generation timing | When the comparison result changes.  |
| Selectable functions                | <ul style="list-style-type: none"> <li>Digital filter function</li> </ul> Whether the digital filter is applied or not and the sampling frequency can be selected. |

i = 1 or 3



**Figure 23.1 Comparator B Block Diagram**

**Table 23.2 I/O Pins**

| Pin Name | I/O   | Function                            |
|----------|-------|-------------------------------------|
| IVCMP1   | Input | Comparator B1 analog pin            |
| IVREF1   | Input | Comparator B1 reference voltage pin |
| IVCMP3   | Input | Comparator B3 analog pin            |
| IVREF3   | Input | Comparator B3 reference voltage pin |

## 23.2 Registers

### 23.2.1 Comparator B Control Register 0 (INTCMP)

Address 01F8h

| Bit         | b7       | b6 | b5 | b4      | b3       | b2 | b1 | b0      |
|-------------|----------|----|----|---------|----------|----|----|---------|
| Symbol      | INT3COUT | —  | —  | INT3CP0 | INT1COUT | —  | —  | INT1CP0 |
| After Reset | 0        | 0  | 0  | 0       | 0        | 0  | 0  | 0       |

| Bit | Symbol   | Bit Name                           | Function  | R/W |
|-----|----------|------------------------------------|---|-----|
| b0  | INT1CP0  | Comparator B1 operation enable bit | 0: Comparator B1 operation disabled<br>1: Comparator B1 operation enabled       | R/W |
| b1  | —        | Reserved bits                      | Set to 0.   | R/W |
| b2  | —        |                                    |   |     |
| b3  | INT1COUT | Comparator B1 monitor flag         | 0: IVCMP1 < IVREF1<br>or comparator B1 operation disabled<br>1: IVCMP1 > IVREF1 | R   |
| b4  | INT3CP0  | Comparator B3 operation enable bit | 0: Comparator B3 operation disabled<br>1: Comparator B3 operation enabled       | R/W |
| b5  | —        | Reserved bits                      | Set to 0.   | R/W |
| b6  | —        |                                    |   |     |
| b7  | INT3COUT | Comparator B3 monitor flag         | 0: IVCMP3 < IVREF3<br>or comparator B3 operation disabled<br>1: IVCMP3 > IVREF3 | R   |

### 23.2.2 External Input Enable Register 0 (INTEN)

Address 01FAh

| Bit         | b7     | b6     | b5 | b4 | b3     | b2     | b1     | b0     |
|-------------|--------|--------|----|----|--------|--------|--------|--------|
| Symbol      | INT3PL | INT3EN | —  | —  | INT1PL | INT1EN | INT0PL | INT0EN |
| After Reset | 0      | 0      | 0  | 0  | 0      | 0      | 0      | 0      |

| Bit | Symbol | Bit Name  | Function                     | R/W |
|-----|--------|---|------------------------------|-----|
| b0  | INT0EN | $\overline{\text{INT0}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b1  | INT0PL | $\overline{\text{INT0}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |
| b2  | INT1EN | $\overline{\text{INT1}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b3  | INT1PL | $\overline{\text{INT1}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |
| b4  | —      | Reserved bits   | Set to 0.                    | R/W |
| b5  | —      |   |                              |     |
| b6  | INT3EN | $\overline{\text{INT3}}$ input enable bit                 | 0: Disabled<br>1: Enabled    | R/W |
| b7  | INT3PL | $\overline{\text{INT3}}$ input polarity select bit (1, 2) | 0: One edge<br>1: Both edges | R/W |

Notes:

- To set the INTiPL bit (i = 0, 1, 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
- The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

### 23.2.3 INT Input Filter Select Register 0 (INTF)

Address 01FCh

|             |        |        |    |    |        |        |        |        |
|-------------|--------|--------|----|----|--------|--------|--------|--------|
| Bit         | b7     | b6     | b5 | b4 | b3     | b2     | b1     | b0     |
| Symbol      | INT3F1 | INT3F0 | —  | —  | INT1F1 | INT1F0 | INT0F1 | INT0F0 |
| After Reset | 0      | 0      | 0  | 0  | 0      | 0      | 0      | 0      |

| Bit | Symbol | Bit Name                     | Function  | R/W |
|-----|--------|------------------------------|---|-----|
| b0  | INT0F0 | INT0 input filter select bit | <sup>b1 b0</sup><br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b1  | INT0F1 |                              |   | R/W |
| b2  | INT1F0 | INT1 input filter select bit | <sup>b3 b2</sup><br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b3  | INT1F1 |                              |   | R/W |
| b4  | —      | Reserved bits                | Set to 0.   | R/W |
| b5  | —      |                              |   | R/W |
| b6  | INT3F0 | INT3 input filter select bit | <sup>b7 b6</sup><br>0 0: No filter<br>0 1: Filter with f1 sampling<br>1 0: Filter with f8 sampling<br>1 1: Filter with f32 sampling | R/W |
| b7  | INT3F1 |                              |   | R/W |

### 23.3 Functional Description

Comparator B1 and comparator B3 operate independently. Their operations are the same. Table 23.3 lists the Procedure for Setting Registers Associated with Comparator B.

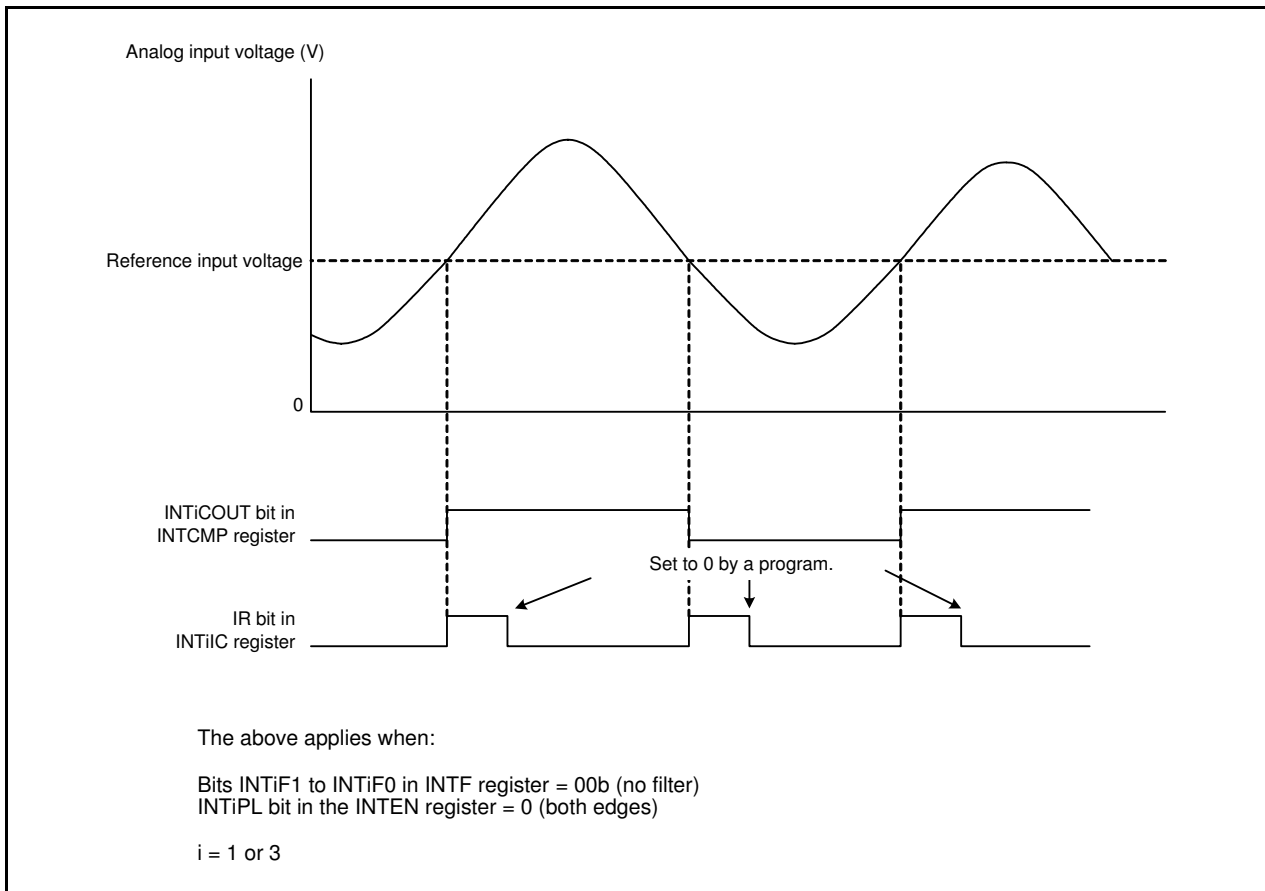
**Table 23.3 Procedure for Setting Registers Associated with Comparator B**

| Step | Register  | Bit   | Setting Value   |
|------|---|---|---|
| 1    | Select the function of pins IVCMP <sub>i</sub> and IVREF <sub>i</sub> . Refer to <b>7.5 Port Settings</b> .<br>However, set registers and bits other than listed in step 2 and the following steps. |   |   |
| 2    | INTF  | Select whether to enable or disable the filter.<br>Select the sampling clock. |   |
| 3    | INTCMP  | INTiCP0   | 1 (operation enabled)   |
| 4    | Wait for comparator stability time (100 μs max.)  |   |   |
| 5    | INTEN   | INTiEN  | When using an interrupt: 1 (interrupt enabled)                      |
|      |   | INTiPL  | When using an interrupt: Select the input polarity.                 |
| 6    | INTiIC  | ILVL2 to ILVL0  | When using an interrupt: Select the interrupt priority level.       |
|      |   | IR  | When using an interrupt: 0 (no interrupt requested: initialization) |

$i = 1 \text{ or } 3$

Figure 23.2 shows an Operating Example of Comparator Bi ( $i = 1 \text{ or } 3$ ).

If the analog input voltage is higher than the reference input voltage, the INTiCOUT bit in the INTCMP register is set to 1. If the analog input voltage is lower than the reference input voltage, the INTiCOUT bit is set to 0. To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. Refer to **23.4 Comparator B1 and Comparator B3 Interrupts** for details of interrupts.



**Figure 23.2 Operating Example of Comparator Bi ( $i = 1 \text{ or } 3$ )**

### 23.3.1 Comparator Bi Digital Filter (i = 1 or 3)

Comparator Bi can use the same digital filter as the  $\overline{\text{INTi}}$  input. The sampling clock can be selected by bits INTiF1 and INTiF0 in the INTF register. The INTiCOUT signal output from comparator Bi is sampled every sampling clock. When the level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 23.3 shows a Configuration of Comparator Bi Digital Filter, and Figure 23.4 shows an Operating Example of Comparator Bi Digital Filter.

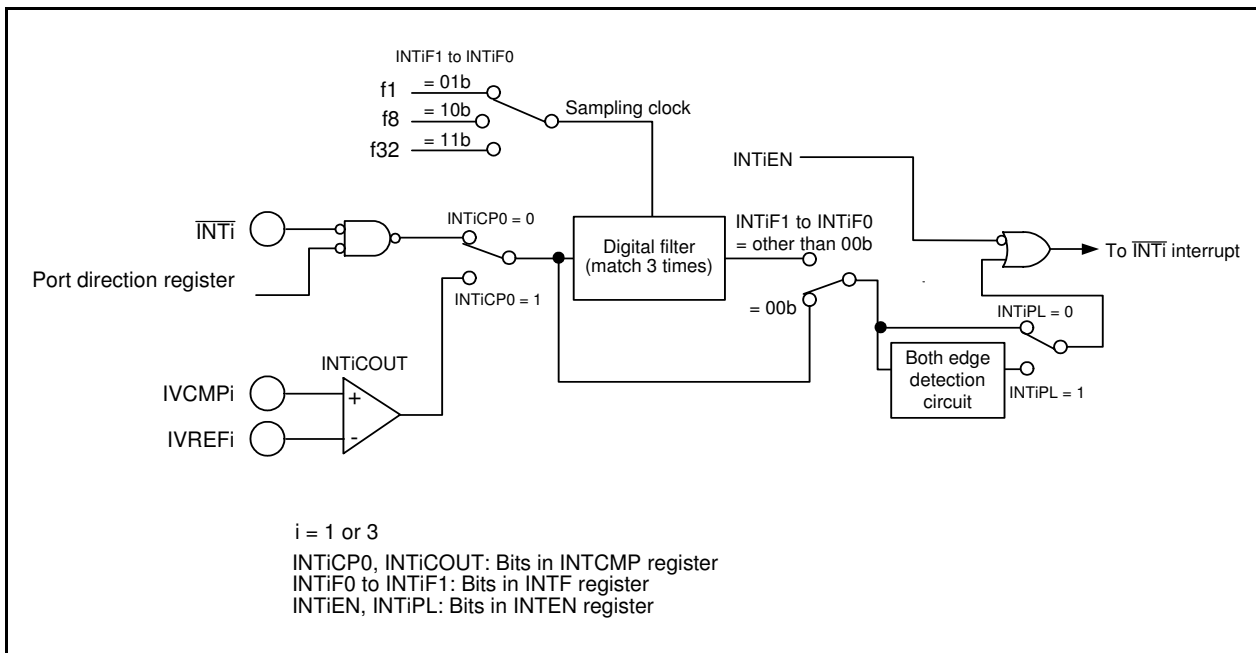


Figure 23.3 Configuration of Comparator Bi Digital Filter

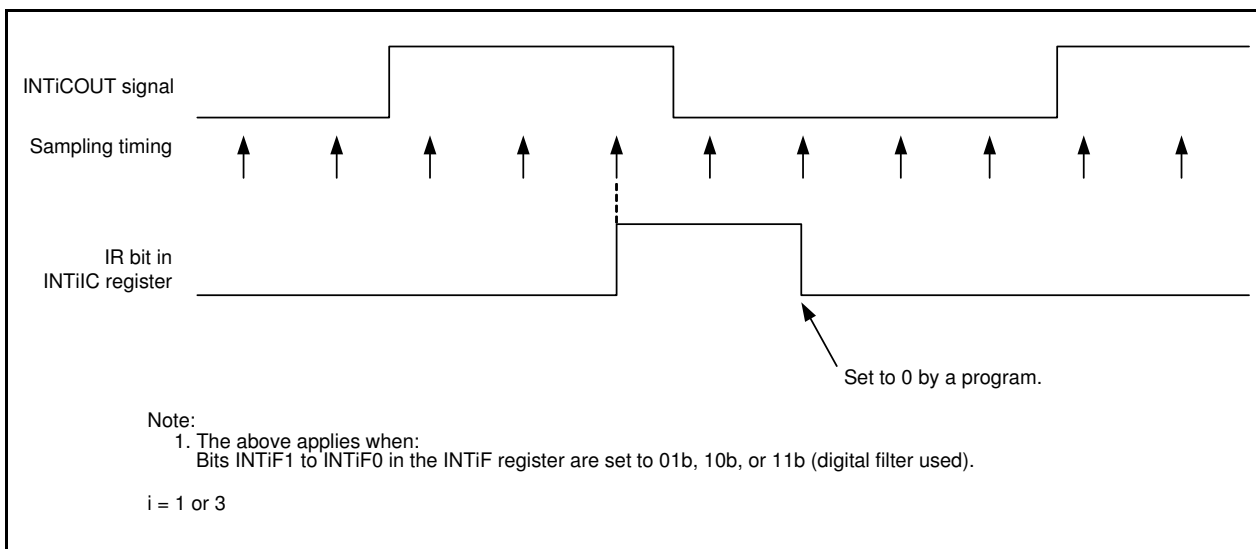


Figure 23.4 Operating Example of Comparator Bi Digital Filter

### 23.4 Comparator B1 and Comparator B3 Interrupts

Comparator B generates an interrupt request from two sources, comparator B1 and comparator B3. The comparator Bi (i = 1 or 3) interrupt uses the same INTiIC register (bits IR and ILVL0 to ILVL2) as the  $\overline{\text{INTi}}$  (i = 1 or 3) and a single vector.

To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). In addition, the polarity can be selected by the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.

Inputs can also be passed through the digital filter with three different sampling clocks.



## 24. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

### 24.1 Overview

Table 24.1 lists the Flash Memory Version Performance. (Refer to **Table 1.1** and **Table 1.2 R8C/3GD Group Specifications** for items not listed in Table 24.1.)

**Table 24.1 Flash Memory Version Performance**

| Item  |  | Specification  |
|---|--|--|
| Flash memory operating mode                           |  | 3 modes (CPU rewrite, standard serial I/O, and parallel I/O) |
| Division of erase blocks                              |  | Refer to <b>Figure 24.1</b> .                                |
| Programming method                                    |  | Byte units   |
| Erasure method  |  | Block erase  |
| Programming and erasure control method <sup>(1)</sup> |  | Program and erase control by software commands               |
| Rewrite control method                                | Blocks 0 to 3 (Program ROM) <sup>(3)</sup> | Rewrite protect control in block units by the lock bit       |
| Number of commands                                    |  | 7 commands   |
| Programming and erasure endurance <sup>(2)</sup>      | Blocks 0 to 3 (Program ROM) <sup>(3)</sup> | 1,000 times  |
| ID code check function                                |  | Standard serial I/O mode supported                           |
| ROM code protection                                   |  | Parallel I/O mode supported                                  |

Notes:

- To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
- Definition of programming and erasure endurance  
The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- The number of blocks and block division vary with the MCU. Refer to **Figure 24.1 R8C/3GD Group Flash Memory Block Diagram** for details.

**Table 24.2 Flash Memory Rewrite Mode**

| Flash Memory Rewrite Mode | CPU Rewrite Mode  | Standard Serial I/O Mode  | Parallel I/O Mode   |
|---------------------------|---|---|---|
| Function                  | User ROM area is rewritten by executing software commands from the CPU. | User ROM area is rewritten using a dedicated serial programmer. | User ROM area is rewritten using a dedicated parallel programmer. |
| Rewritable area           | User ROM  | User ROM  | User ROM  |
| Rewrite programs          | User program  | Standard boot program   | –   |

## 24.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).

Figure 24.1 shows the R8C/3GD Group Flash Memory Block Diagram.

The user ROM area contains program ROM.

Program ROM: Flash memory mainly used for storing programs

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.

The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

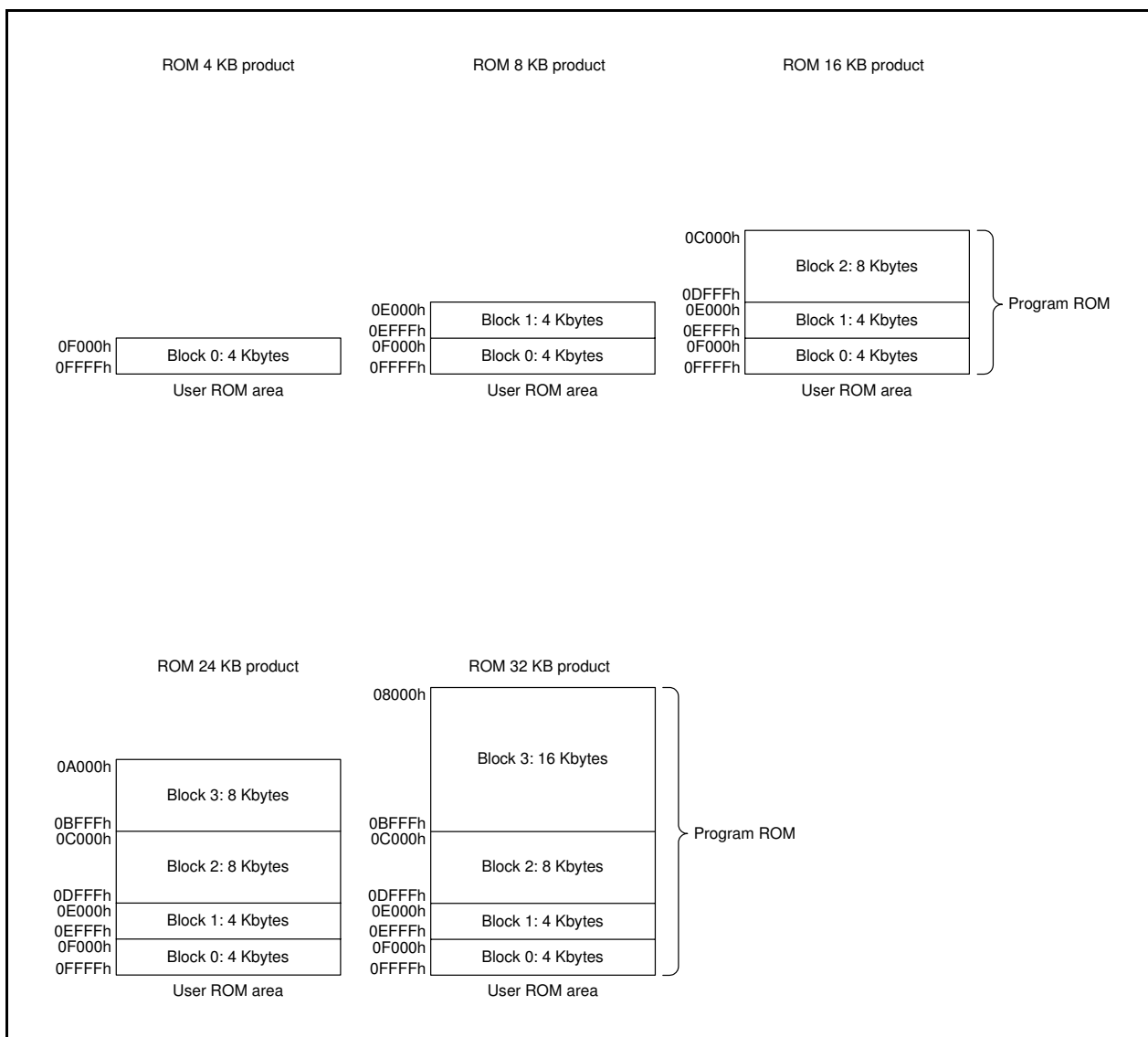


Figure 24.1 R8C/3GD Group Flash Memory Block Diagram

## 24.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

### 24.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **12. ID Code Areas**.

### 24.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.

Refer to **13. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.

Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

### 24.3.3 Option Function Select Register (OFS)

Address 0FFFFh

| Bit         | b7                                | b6    | b5     | b4     | b3     | b2    | b1 | b0    |
|-------------|-----------------------------------|-------|--------|--------|--------|-------|----|-------|
| Symbol      | CSPROINI                          | LVDAS | VDSEL1 | VDSEL0 | ROMCP1 | ROMCR | —  | WDTON |
| After Reset | User Setting Value <sup>(1)</sup> |       |        |        |        |       |    |       |

| Bit | Symbol   | Bit Name   | Function  | R/W |
|-----|----------|--|---|-----|
| b0  | WDTON    | Watchdog timer start select bit                      | 0: Watchdog timer automatically starts after reset.<br>1: Watchdog timer is stopped after reset.  | R/W |
| b1  | —        | Reserved bit   | Set to 1.   | R/W |
| b2  | ROMCR    | ROM code protect disable bit                         | 0: ROM code protect disabled<br>1: ROMCP1 bit enabled   | R/W |
| b3  | ROMCP1   | ROM code protect bit                                 | 0: ROM code protect enabled<br>1: ROM code protect disabled   | R/W |
| b4  | VDSEL0   | Voltage detection 0 level select bit <sup>(2)</sup>  | b5 b4<br>0 0: 3.80 V selected (Vdet0_3)<br>0 1: 2.85 V selected (Vdet0_2)<br>1 0: 2.35 V selected (Vdet0_1)<br>1 1: 1.90 V selected (Vdet0_0) | R/W |
| b5  | VDSEL1   |  |   | R/W |
| b6  | LVDAS    | Voltage detection 0 circuit start bit <sup>(3)</sup> | 0: Voltage monitor 0 reset enabled after reset<br>1: Voltage monitor 0 reset disabled after reset   | R/W |
| b7  | CSPROINI | Count source protection mode after reset select bit  | 0: Count source protect mode enabled after reset<br>1: Count source protect mode disabled after reset   | R/W |

Notes:

- The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.  
Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.  
When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.  
When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
- The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
- To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

#### LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

## 24.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.

The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.

Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.

Table 24.3 lists the Differences between EW0 Mode and EW1 Mode.

**Table 24.3 Differences between EW0 Mode and EW1 Mode**

| Item  | EW0 Mode  | EW1 Mode  |
|---|---|---|
| Operating mode  | Single-chip mode  | Single-chip mode  |
| Rewrite control program allocatable area                                | User ROM  | User ROM  |
| Rewrite control program executable areas                                | RAM (The rewrite control program must be transferred before being executed.)  | User ROM or RAM   |
| Rewritable area   | User ROM  | User ROM<br>However, blocks which contain the rewrite control program are excluded.   |
| Software command restrictions   | —   | Program and block erase commands<br>Cannot be executed to any block which contains the rewrite control program.   |
| Mode after programming or block erasure or after entering erase-suspend | Read array mode   | Read array mode   |
| CPU state during programming and block erasure                          | The CPU operates.   | The CPU is put in a hold state while the program ROM area is being programmed or block erased. (I/O ports retain the state before the command execution). |
| Flash memory status detection   | Read bits FST7, FMT5, and FMT4 in the FST register by a program.  | Read bits FST7, FMT5, and FMT4 in the FST register by a program.  |
| Conditions for entering erase-suspend                                   | <ul style="list-style-type: none"> <li>• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program.</li> <li>• Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.</li> </ul> | Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.   |
| CPU clock   | Max. 20 MHz   | Max. 20 MHz   |

### 24.4.1 Flash Memory Status Register (FST)

Address 01B2h

| Bit         | b7   | b6   | b5   | b4   | b3 | b2     | b1     | b0     |
|-------------|------|------|------|------|----|--------|--------|--------|
| Symbol      | FST7 | FST6 | FST5 | FST4 | —  | LBDATA | BSYAEI | RDYSTI |
| After Reset | 1    | 0    | 0    | 0    | 0  | X      | 0      | 0      |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | RDYSTI | Flash ready status interrupt request flag (1, 4)                          | 0: No flash ready status interrupt request<br>1: Flash ready status interrupt request | R/W |
| b1  | BSYAEI | Flash access error interrupt request flag (2, 4)                          | 0: No flash access error interrupt request<br>1: Flash access error interrupt request | R/W |
| b2  | LBDATA | LBDATA monitor flag   | 0: Locked<br>1: Not locked  | R   |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | FST4   | Program error flag (3)  | 0: No program error<br>1: Program error   | R   |
| b5  | FST5   | Erase error/blank check error flag (3)                                    | 0: No erase error/blank check error<br>1: Erase error/blank check error               | R   |
| b6  | FST6   | Erase-suspend status flag   | 0: Other than erase-suspend<br>1: During erase-suspend                                | R   |
| b7  | FST7   | Ready/busy status flag  | 0: Busy<br>1: Ready   | R   |

Notes:

1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

#### RDYSTI Bit (Flash Ready Status Flag Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).

During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]

Set to 0 by an interrupt handling program.

[Condition for setting to 1]

When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.

The status is changed from busy to ready in the following states:

- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it has been stopped.

### BSYAEI Bit (Flash Access Error Interrupt Request Flag)

The BSYAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]

- (1) Set to 0 by an interrupt handling program.
- (2) Execute the clear status register command.

[Conditions for setting to 1]

- (1) Read or write the area that is being erased/written when the BSYAEIE bit in the FMR0 register is set to 1 and while the flash memory is busy.  
(Note that the read value is undefined. Writing has no effect.)
- (2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

### LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).

The condition for updating this bit is when the program, erase, read lock bit status commands are generated.

When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

### FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **24.4.11 Full Status Check**.

### FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-programming or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **24.4.11 Full Status Check** for details.

### FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

### FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:

- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

### 24.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

|             |         |         |         |        |       |       |       |    |
|-------------|---------|---------|---------|--------|-------|-------|-------|----|
| Bit         | b7      | b6      | b5      | b4     | b3    | b2    | b1    | b0 |
| Symbol      | RDYSTIE | BSYAEIE | CMDERIE | CMDRST | FMSTP | FMR02 | FMR01 | —  |
| After Reset | 0       | 0       | 0       | 0      | 0     | 0     | 0     | 0  |

| Bit | Symbol  | Bit Name                                | Function  | R/W |
|-----|---------|---|---|-----|
| b0  | —       | Reserved bit                            | Set to 0.   | R/W |
| b1  | FMR01   | CPU rewrite mode select bit (1, 4)      | 0: CPU rewrite mode disabled<br>1: CPU rewrite mode enabled   | R/W |
| b2  | FMR02   | EW1 mode select bit (1)                 | 0: EW0 mode<br>1: EW1 mode  | R/W |
| b3  | FMSTP   | Flash memory stop bit (2)               | 0: Flash memory operates<br>1: Flash memory stops<br>(Low-power consumption state, flash memory initialization)                                 | R/W |
| b4  | CMDRST  | Erase/write sequence reset bit (3)      | When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped.<br>When read, the content is 0. | R/W |
| b5  | CMDERIE | Erase/write error interrupt enable bit  | 0: Erase/write error interrupt disabled<br>1: Erase/write error interrupt enabled   | R/W |
| b6  | BSYAEIE | Flash access error interrupt enable bit | 0: Flash access error interrupt disabled<br>1: Flash access error interrupt enabled   | R/W |
| b7  | RDYSTIE | Flash ready status interrupt enable bit | 0: Flash ready status interrupt disabled<br>1: Flash ready status interrupt enabled   | R/W |

Notes:

- To set this bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.
- Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
- The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
- To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

#### FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

#### FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.



### FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.

Write to the FMSTP bit by a program transferred to the RAM.

To reduce the power consumption further in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stopped), and low-speed clock mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **25.2.9 Stopping Flash Memory** for details.

When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.

When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

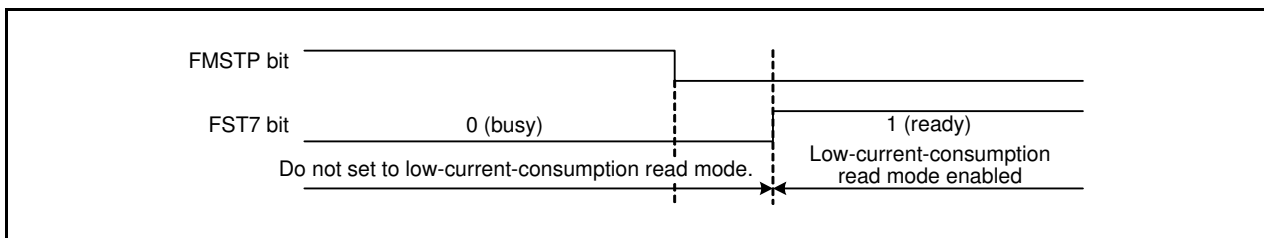


Figure 24.2 Transition to Low-Current-Consumption Read Mode

### CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command. The user ROM area can be read while the flash memory sequence is being initialized.

If the program or erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erasure command again.

When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.

When  $t_d(\text{CMDRST-READY})$  has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly stopped and reading from the flash memory is enabled.

### CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables an flash command error interrupt to be generated if the following errors occur:

- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.

If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

### BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

### RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

### 24.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

| Bit         | b7 | b6 | b5 | b4 | b3    | b2    | b1    | b0    |
|-------------|----|----|----|----|-------|-------|-------|-------|
| Symbol      | —  | —  | —  | —  | FMR13 | FMR12 | FMR11 | FMR10 |
| After Reset | 0  | 0  | 0  | 0  | 0     | 0     | 0     | 0     |

| Bit | Symbol | Bit Name  | Function                                    | R/W |
|-----|--------|---|---|-----|
| b0  | FMR10  | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b1  | FMR11  |   |   |     |
| b2  | FMR12  |   |   |     |
| b3  | FMR13  | Lock bit disable select bit <sup>(1)</sup>                                | 0: Lock bit enabled<br>1: Lock bit disabled | R/W |
| b4  | —      | Reserved bits   | Set to 0.                                   | R/W |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | —      |   |   |     |

Note:

- To set the FMR13 bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

#### FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **24.4.9 Data Protect Function** for the details of the lock bit.

The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]

The FMR13 bit is set to 0 when one of the following conditions is met.

- Completion of the program command
- Completion of the erase command
- Transition to erase-suspend
- Generation of a command sequence error
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]

Set to 1 by a program.

### 24.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

| Bit         | b7    | b6 | b5 | b4 | b3 | b2    | b1    | b0    |
|-------------|-------|----|----|----|----|-------|-------|-------|
| Symbol      | FMR27 | —  | —  | —  | —  | FMR22 | FMR21 | FMR20 |
| After Reset | 0     | 0  | 0  | 0  | 0  | 0     | 0     | 0     |

| Bit | Symbol | Bit Name  | Function  | R/W |
|-----|--------|---|---|-----|
| b0  | FMR20  | Erase-suspend enable bit <sup>(1)</sup>                                   | 0: Erase-suspend disabled<br>1: Erase-suspend enabled   | R/W |
| b1  | FMR21  | Erase-suspend request bit <sup>(2)</sup>                                  | 0: Erase restart<br>1: Erase-suspend request  | R/W |
| b2  | FMR22  | Interrupt request suspend request enable bit <sup>(1)</sup>               | 0: Erase-suspend request disabled by interrupt request<br>1: Erase-suspend request enabled by interrupt request | R/W |
| b3  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |   | —   |
| b4  | —      | Reserved bits   | Set to 0.   | R/W |
| b5  | —      |   |   |     |
| b6  | —      |   |   |     |
| b7  | FMR27  | Low-current-consumption read mode enable bit <sup>(1, 3)</sup>            | 0: Low-current-consumption read mode disabled<br>1: Low-current-consumption read mode enabled                   | R/W |

Notes:

- To set this bit to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.
- To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
- Set the FMR27 bit to 1 after setting either of the following:
  - Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
  - Set the CPU clock to the XCIN clock divided by 1 (no division), 2, 4, or 8.
 Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

#### FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

#### FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]

Set to 0 by a program.

[Conditions for setting to 1]

- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

### **FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)**

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

### **FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)**

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **25.2.10 Low-Current-Consumption Read Mode** for details.

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

### 24.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST6 bit is set to 0 (other than erase-suspend).

### 24.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after  $t_d(SR-SUS)$ . After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

### 24.4.7 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erase.

When auto-erase is suspended, the next operation can be executed. (Refer to **Table 24.4 Executable Operation during Suspend.**)

- When suspending the auto-erase of any block in program ROM, auto-programming and reading another block can be executed.
- To check the suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase-suspend), erasure completes.

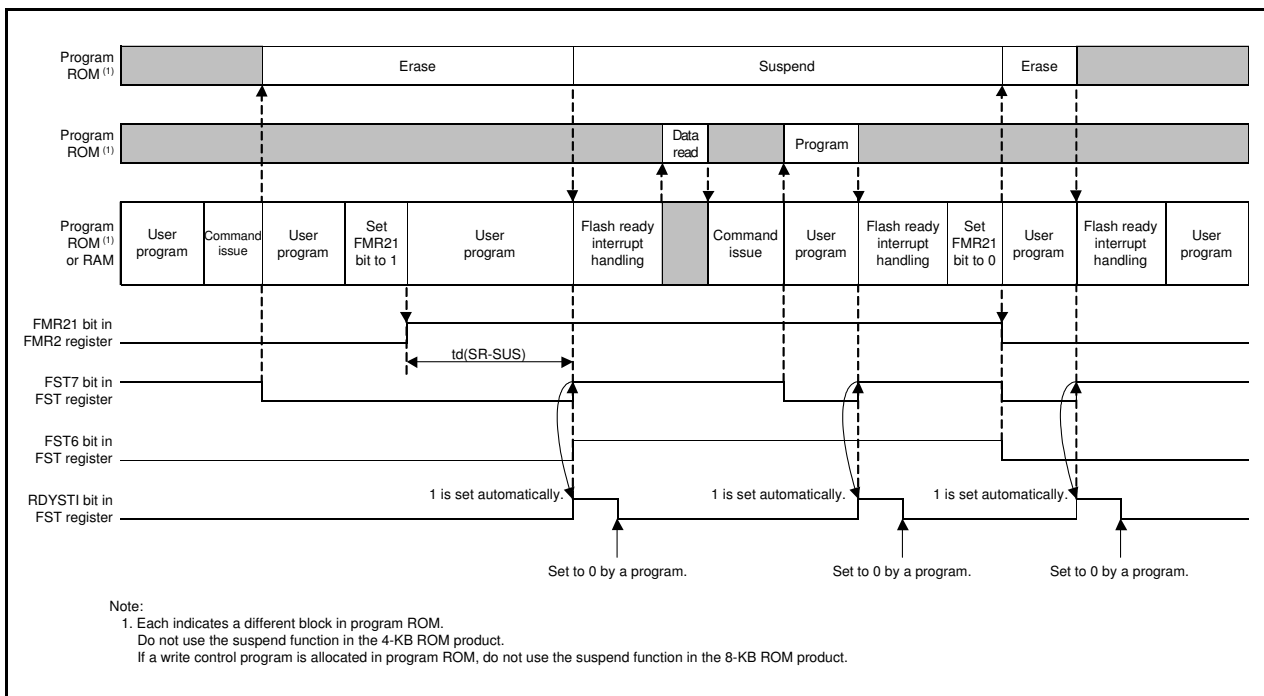
Figure 24.3 shows the Suspend Operation Timing.

**Table 24.4 Executable Operation during Suspend**

|  |             | Operation during Suspend   |         |      |   |         |      |
|--|-------------|--|---------|------|---|---------|------|
|  |             | Program ROM (Block during erasure execution before entering suspend) |         |      | Program ROM (Block during no erasure execution before entering suspend) |         |      |
|  |             | Erase  | Program | Read | Erase   | Program | Read |
| Areas during erasure execution before entering suspend | Program ROM | D  | D       | D    | D   | E       | E    |

Notes:

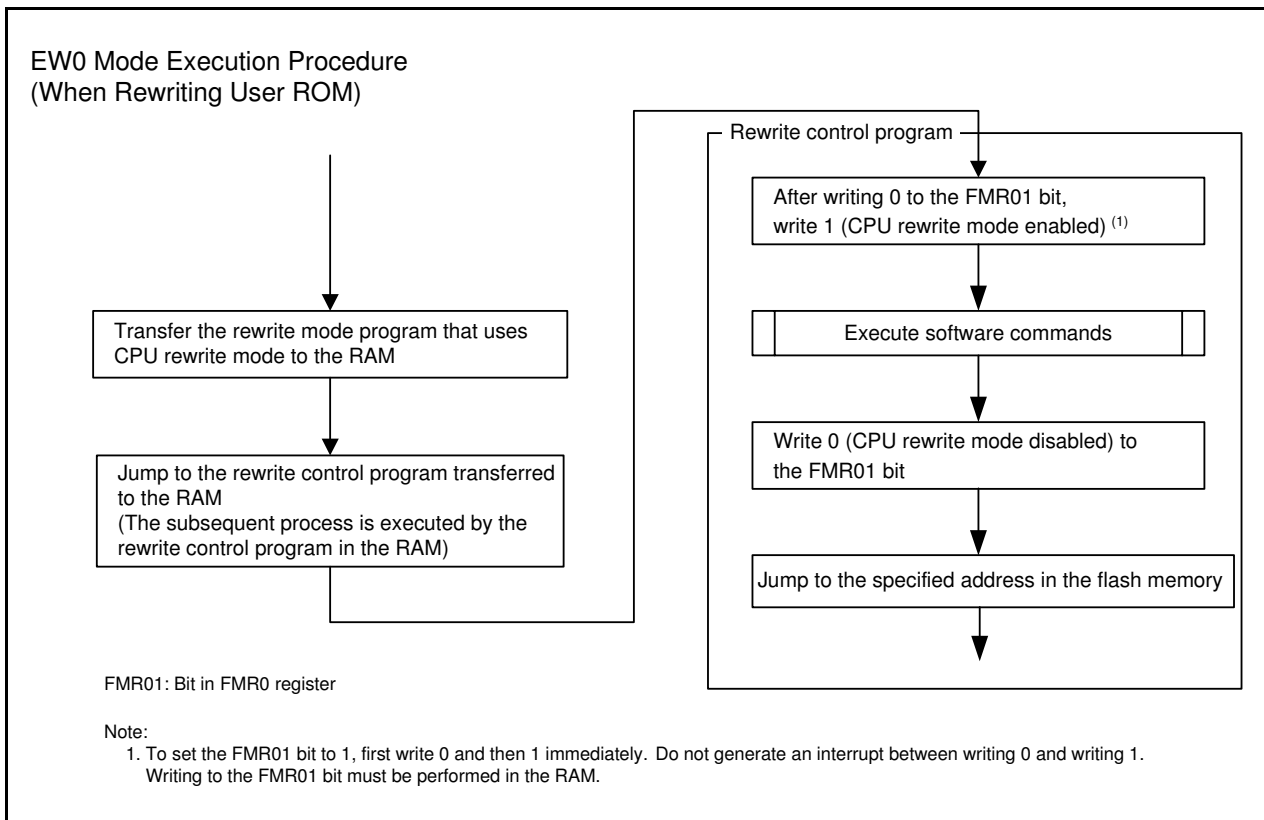
1. E indicates operation is enabled by using the suspend function and D indicates operation is disabled.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.  
The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).  
The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.



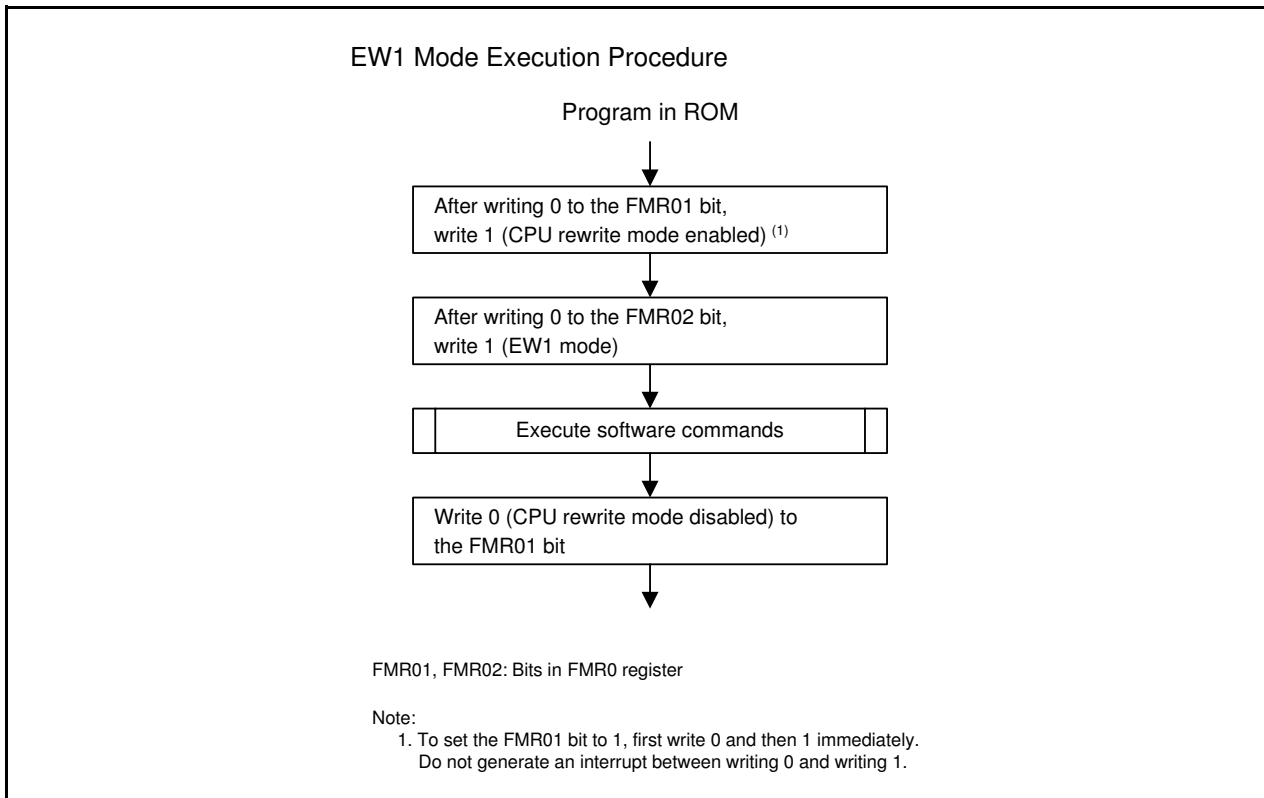
**Figure 24.3 Suspend Operation Timing**

### 24.4.8 How to Set and Exit Each Mode

Figure 24.4 shows How to Set and Exit EW0 Mode and Figure 24.5 shows How to Set and Exit EW1 Mode.



**Figure 24.4 How to Set and Exit EW0 Mode**



**Figure 24.5 How to Set and Exit EW1 Mode**

### 24.4.9 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.

The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).

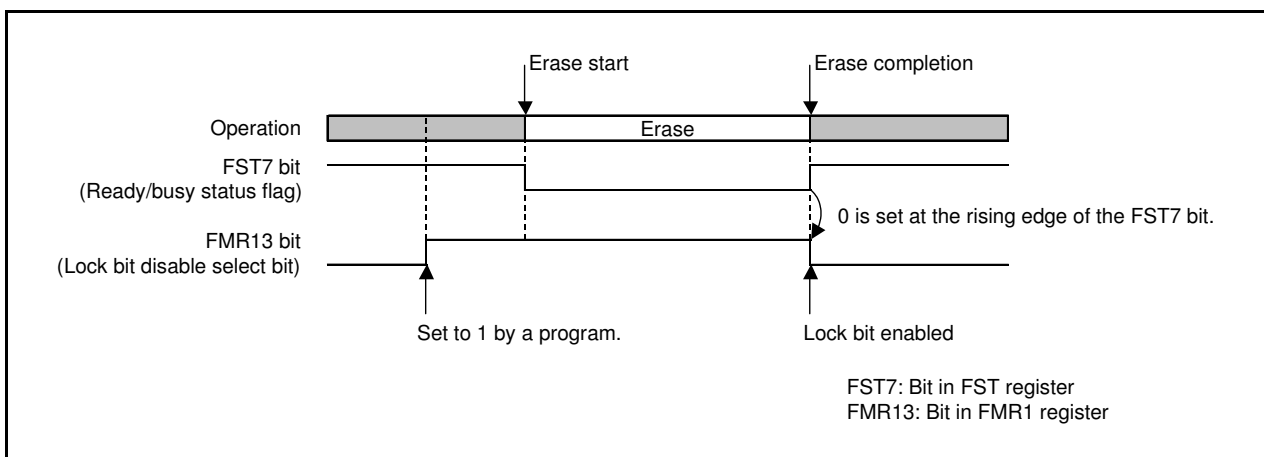
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.

Refer to **24.4.10 Software Commands** for the details of individual commands.

The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FM0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 24.6 shows the FMR13 Bit Operation Timing.



**Figure 24.6 FMR13 Bit Operation Timing**



### 24.4.10 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.  
Do not input any command other than those listed in the table below.

**Table 24.5 Software Commands**

| Command               | First Bus Cycle |         |      | Second Bus Cycle |         |      |
|-----------------------|-----------------|---------|------|------------------|---------|------|
|                       | Mode            | Address | Data | Mode             | Address | Data |
| Read array            | Write           | x       | FFh  |                  |         |      |
| Clear status register | Write           | x       | 50h  |                  |         |      |
| Program               | Write           | WA      | 40h  | Write            | WA      | WD   |
| Block erase           | Write           | x       | 20h  | Write            | BA      | D0h  |
| Lock bit program      | Write           | BT      | 77h  | Write            | BT      | D0h  |
| Read lock bit status  | Write           | x       | 71h  | Write            | BT      | D0h  |
| Block blank check     | Write           | x       | 25h  | Write            | BA      | D0h  |

WA: Write address

WD: Write data

BA: Any block address

BT: Starting block address

x: Any address in the user ROM area

#### 24.4.10.1 Read Array Command

The read array command is used to read the flash memory.

When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.

Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.

In addition, after a reset, the MCU enters read array mode after programming or block erasure or after entering erase-suspend.

#### 24.4.10.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.

When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

### 24.4.10.3 Program Command

The program command is used to write data to the flash memory in 1-byte units.

When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.

The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.

After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **24.4.11 Full Status Check**).

Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.

Figure 24.7 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 24.8 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

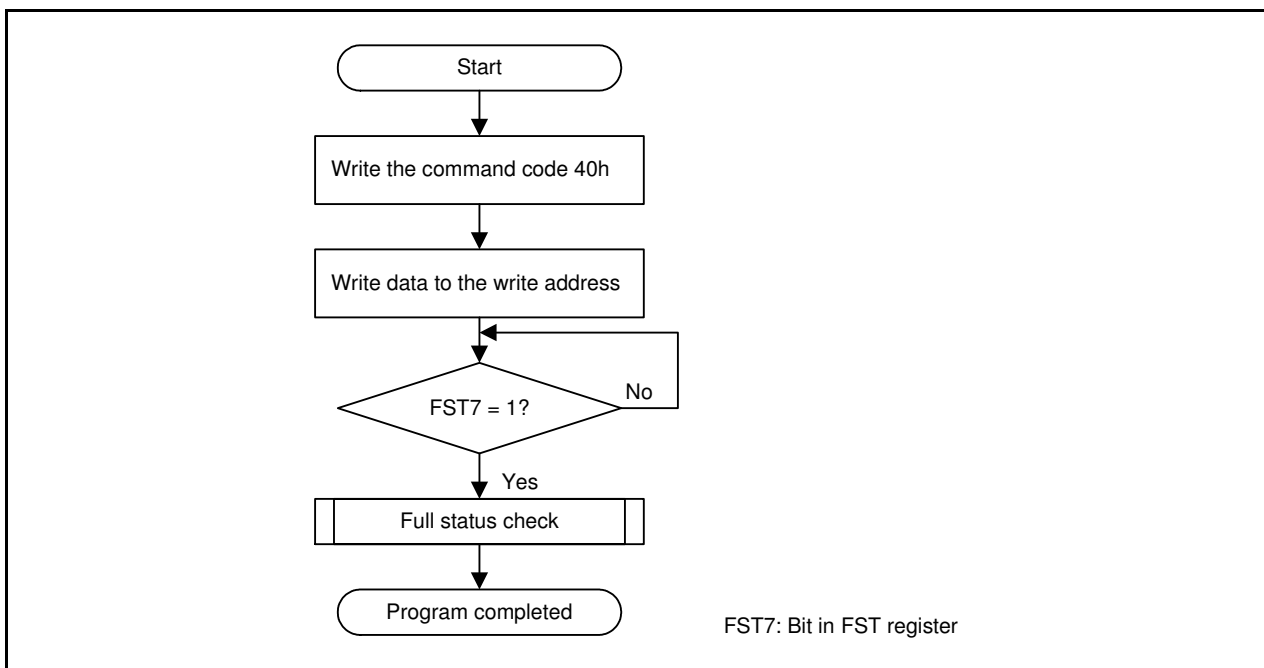


Figure 24.7 Program Flowchart (Flash Ready Status Interrupt Disabled)

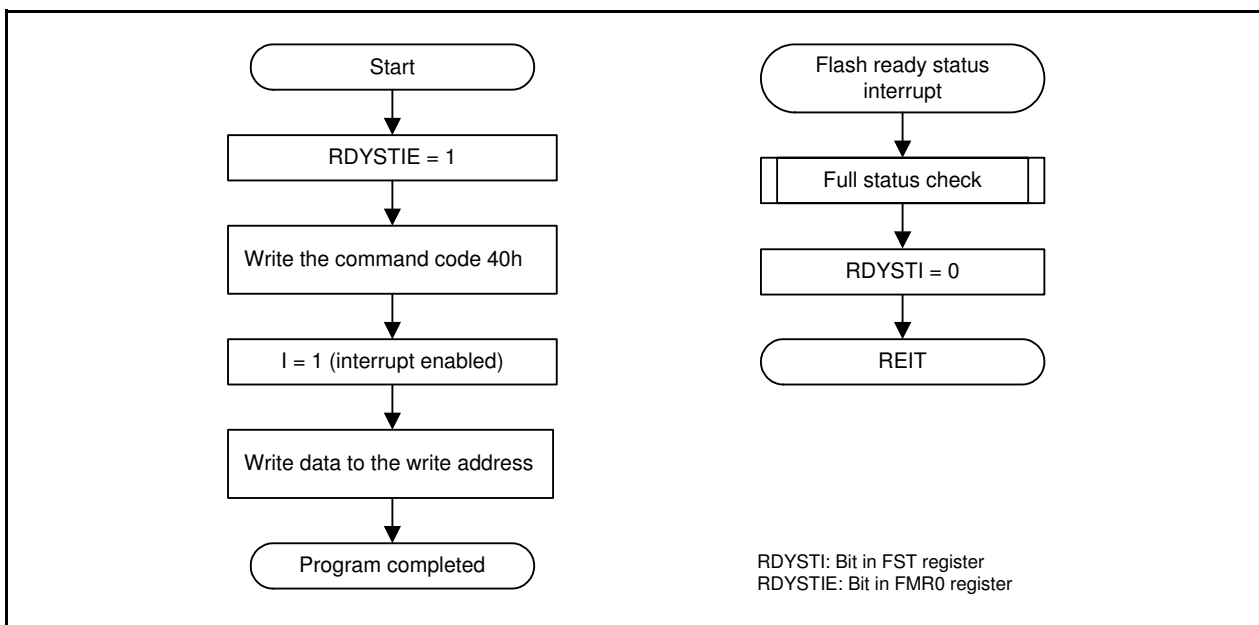


Figure 24.8 Program Flowchart (Flash Ready Status Interrupt Enabled)

#### 24.4.10.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.

The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.

After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **24.4.11 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.

Figure 24.9 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 24.10 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 24.11 shows a Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

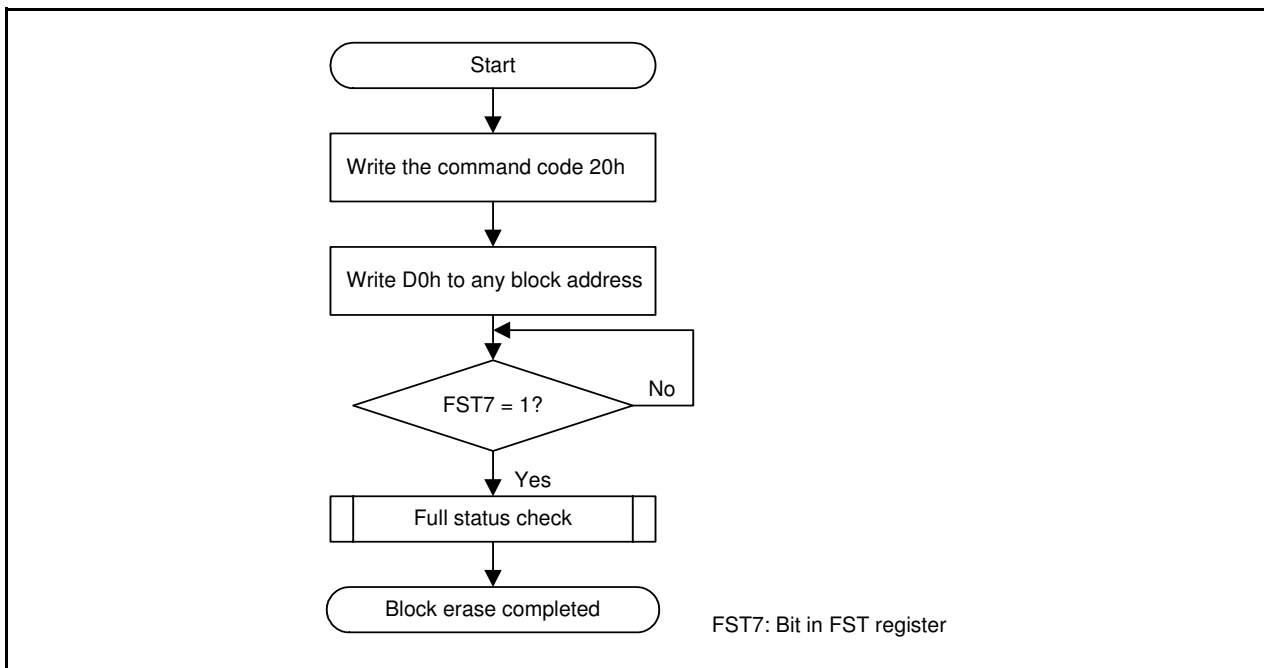
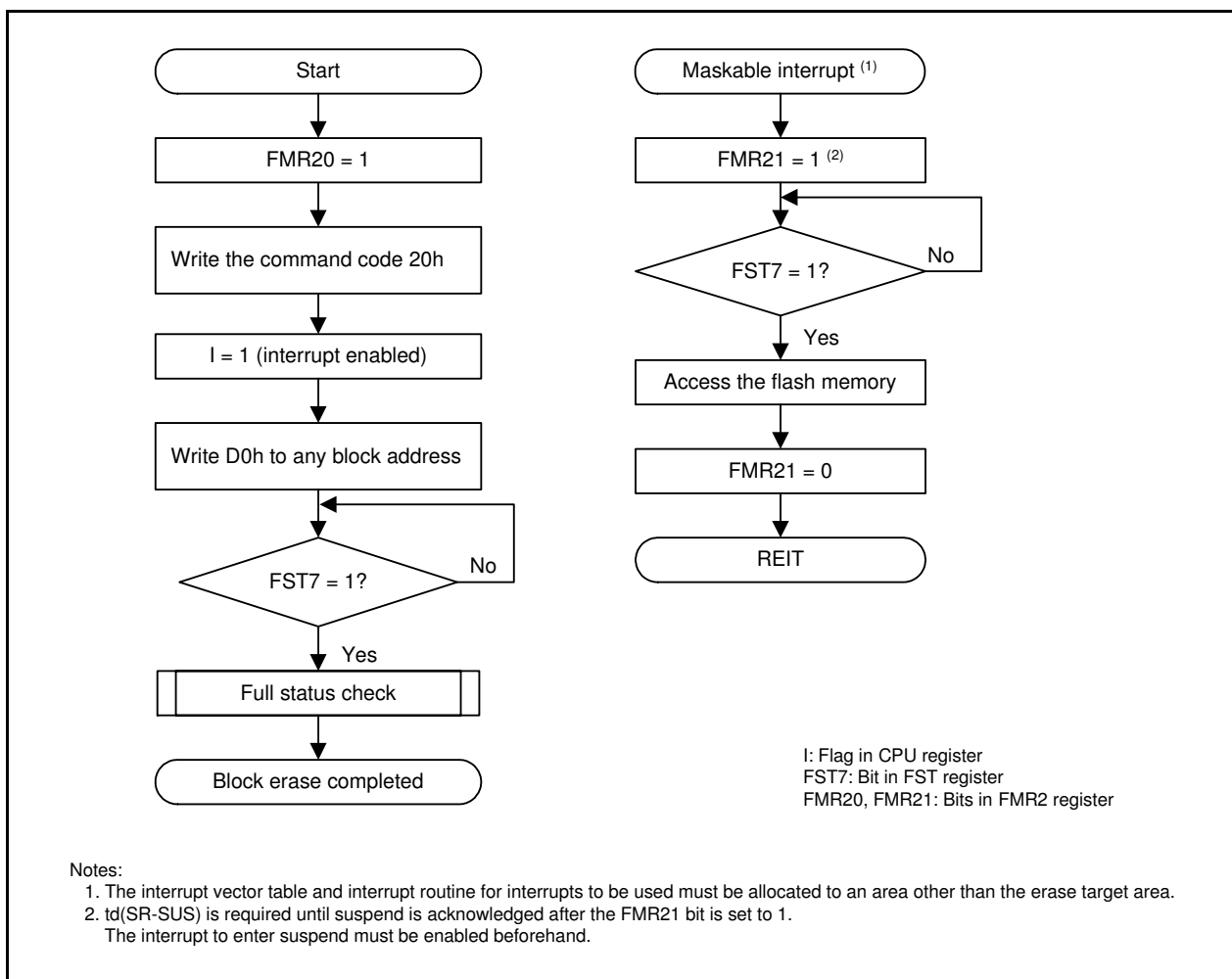


Figure 24.9 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



**Figure 24.10 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled)**

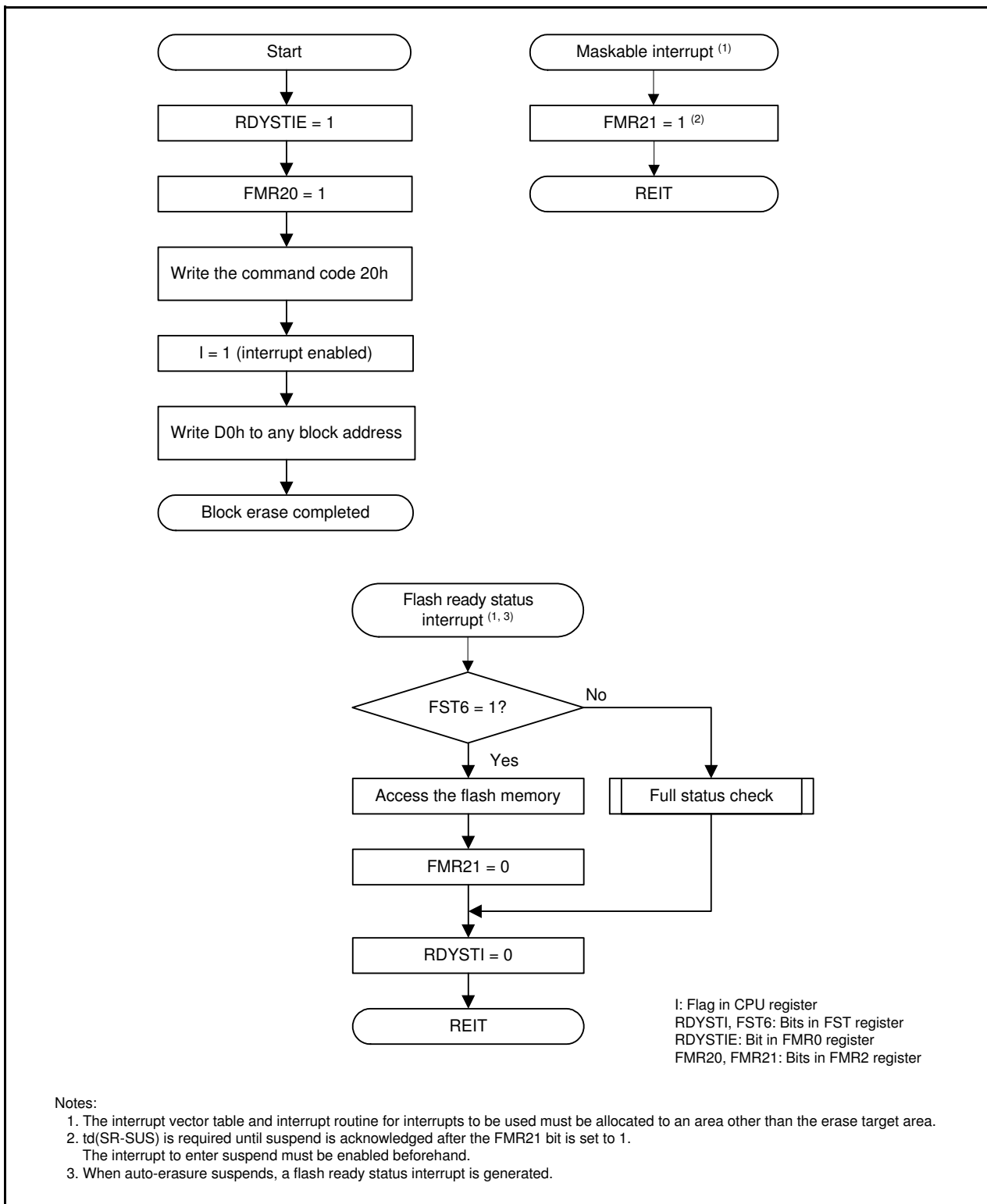


Figure 24.11 Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled)

### 24.4.10.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).

When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.

Figure 24.12 shows a Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.

The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.

Refer to **24.4.9 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

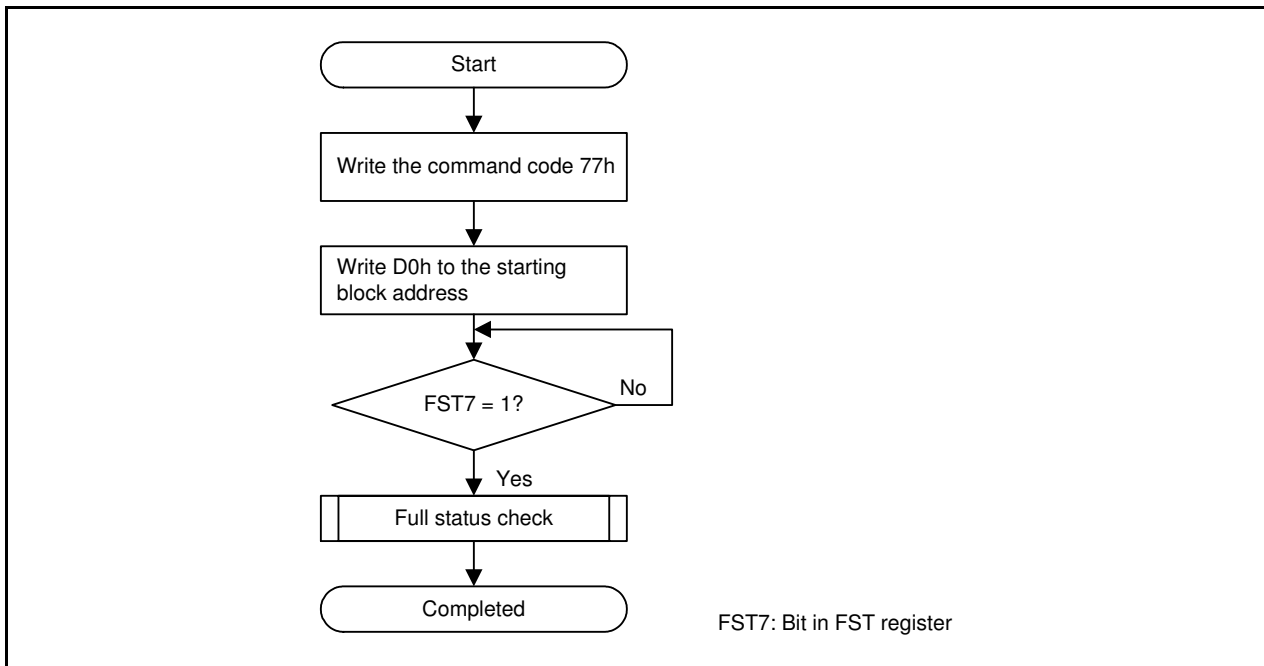


Figure 24.12 Lock Bit Program Flowchart



### 24.4.10.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any address in the program ROM area.

When 71h written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.

Figure 24.13 shows a Read Lock Bit Status Flowchart.

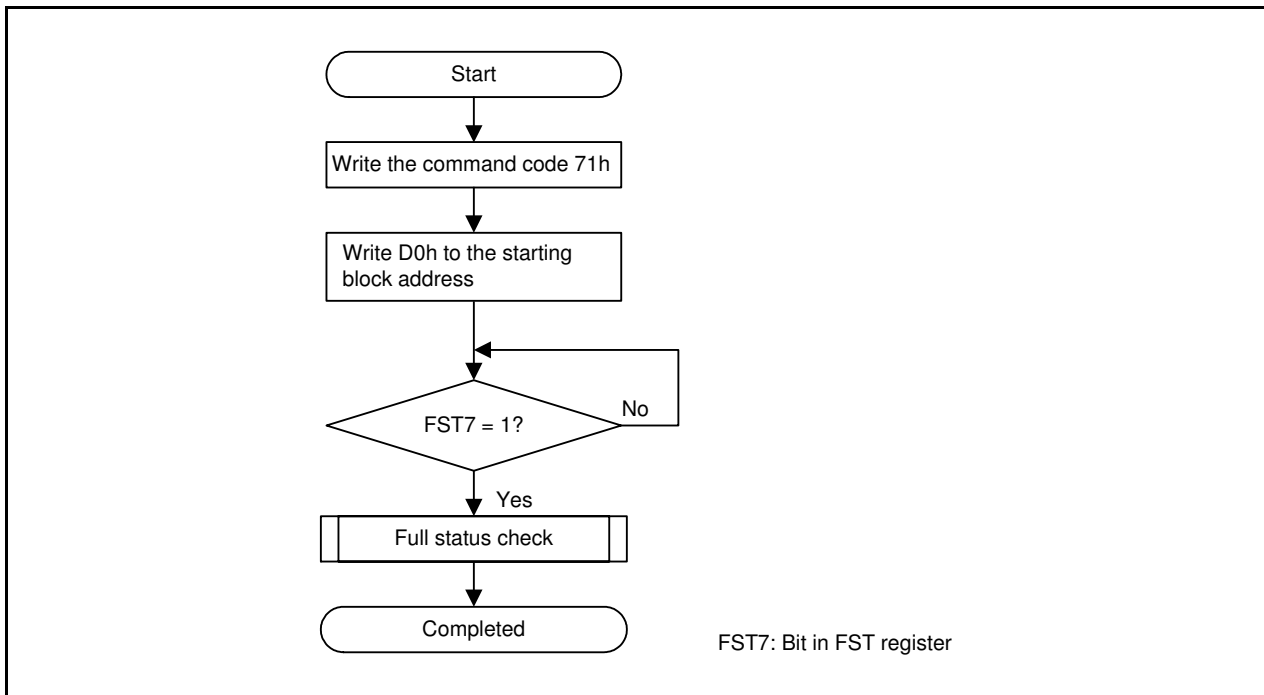


Figure 24.13 Read Lock Bit Status Flowchart

### 24.4.10.7 Block Blank Check Command

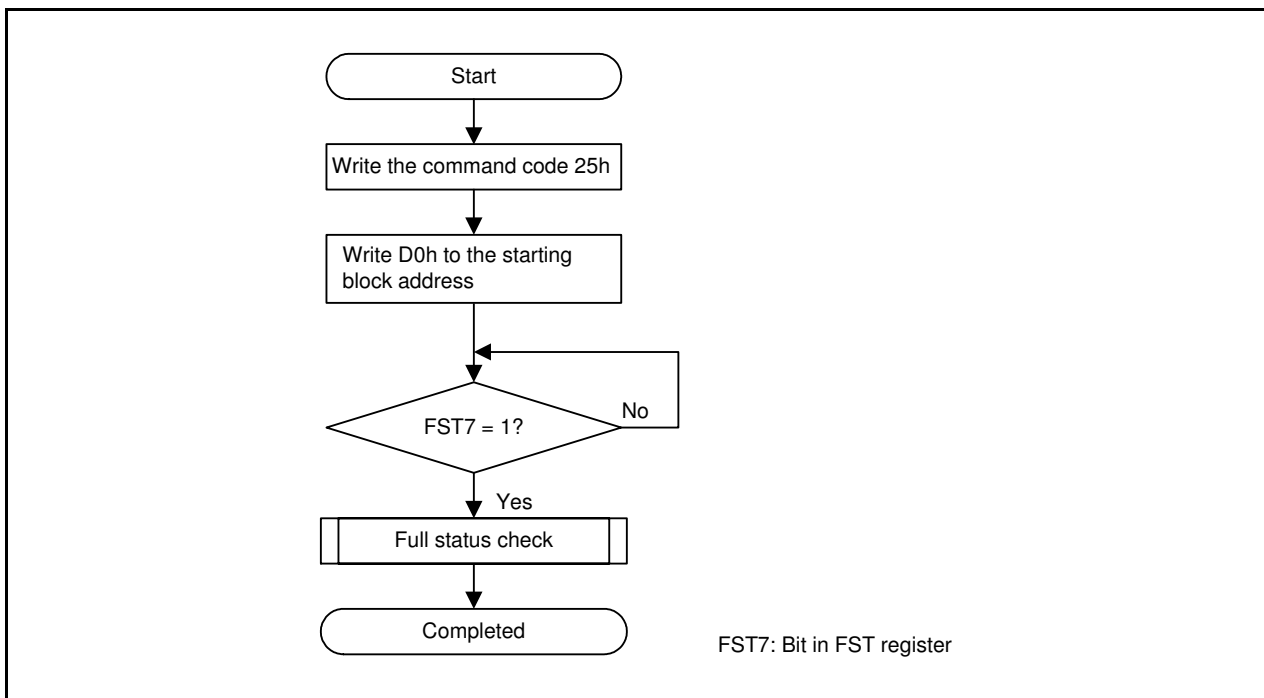
This command is used to confirm that all addresses in any block are blank data FFh.

When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.

After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **24.4.11 Full Status Check**.) This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).

Figure 24.14 shows a Block Blank Check Flowchart.



**Figure 24.14 Block Blank Check Flowchart**

This command is intended for programmer manufactures, not for general users.

### 24.4.11 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).

Table 24.6 lists the Errors and FST Register Status. Figure 24.15 shows the Full Status Check and Handling Procedure for Individual Errors.

**Table 24.6 Errors and FST Register Status**

| FST Register Status |      | Error                                    | Error Occurrence Condition  |
|---------------------|------|--|---|
| FST5                | FST4 |  |   |
| 1                   | 1    | Command sequence error                   | <ul style="list-style-type: none"> <li>• When a command is not written correctly.</li> <li>• When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command <sup>(1)</sup>.</li> <li>• The erase command is executed during suspend</li> <li>• The command is executed to the block during suspend</li> </ul> |
| 1                   | 0    | Erase error                              | When the block erase command is executed, but auto-erasure does not complete correctly.   |
|                     |      | Blank check error                        | When the block blank check command is executed and data other than blank data FFh is read.  |
| 0                   | 1    | Program error/<br>lock bit program error | When the program command is executed, but auto-programming does not complete correctly.   |

Note:

1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

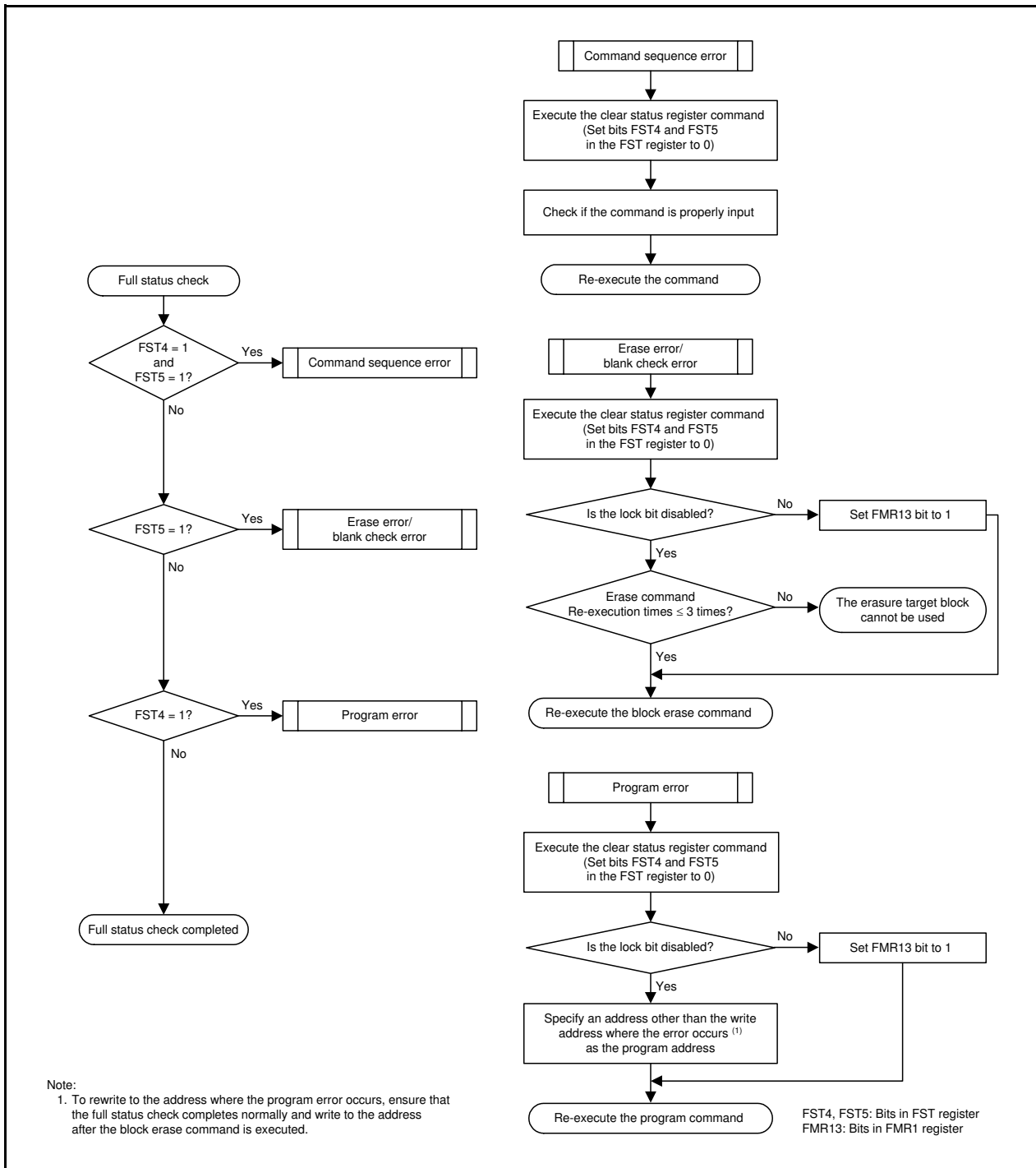


Figure 24.15 Full Status Check and Handling Procedure for Individual Errors

## 24.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.

There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

Table 24.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 24.16 shows Pin Handling in Standard Serial I/O Mode 2. Table 24.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 24.17 shows Pin Handling in Standard Serial I/O Mode 3.

After handling the pins shown in Table 24.8 and rewriting the flash memory using the programmer, apply a "H" level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

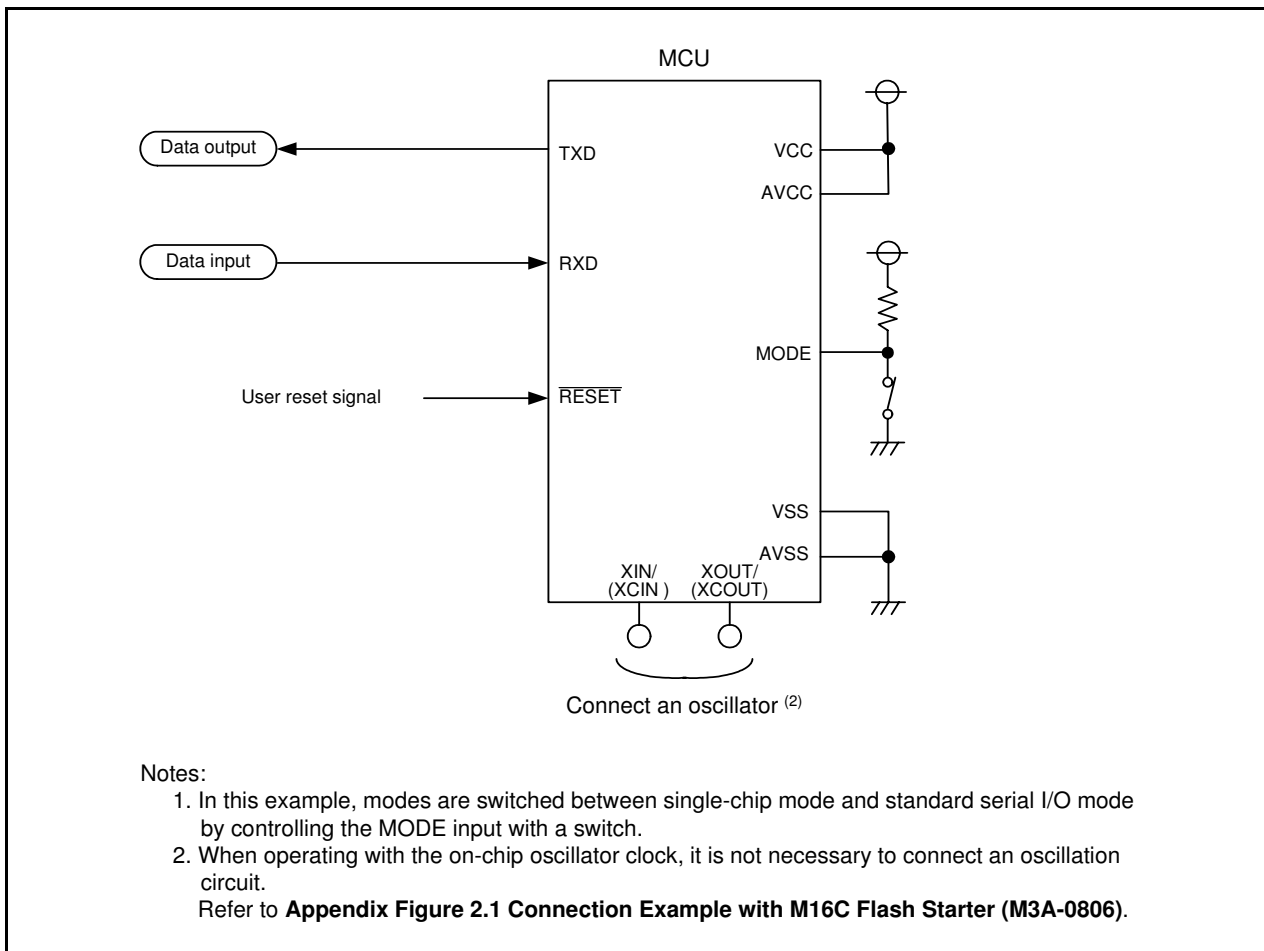
### 24.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.

Refer to **12. ID Code Areas** for details of the ID code check.

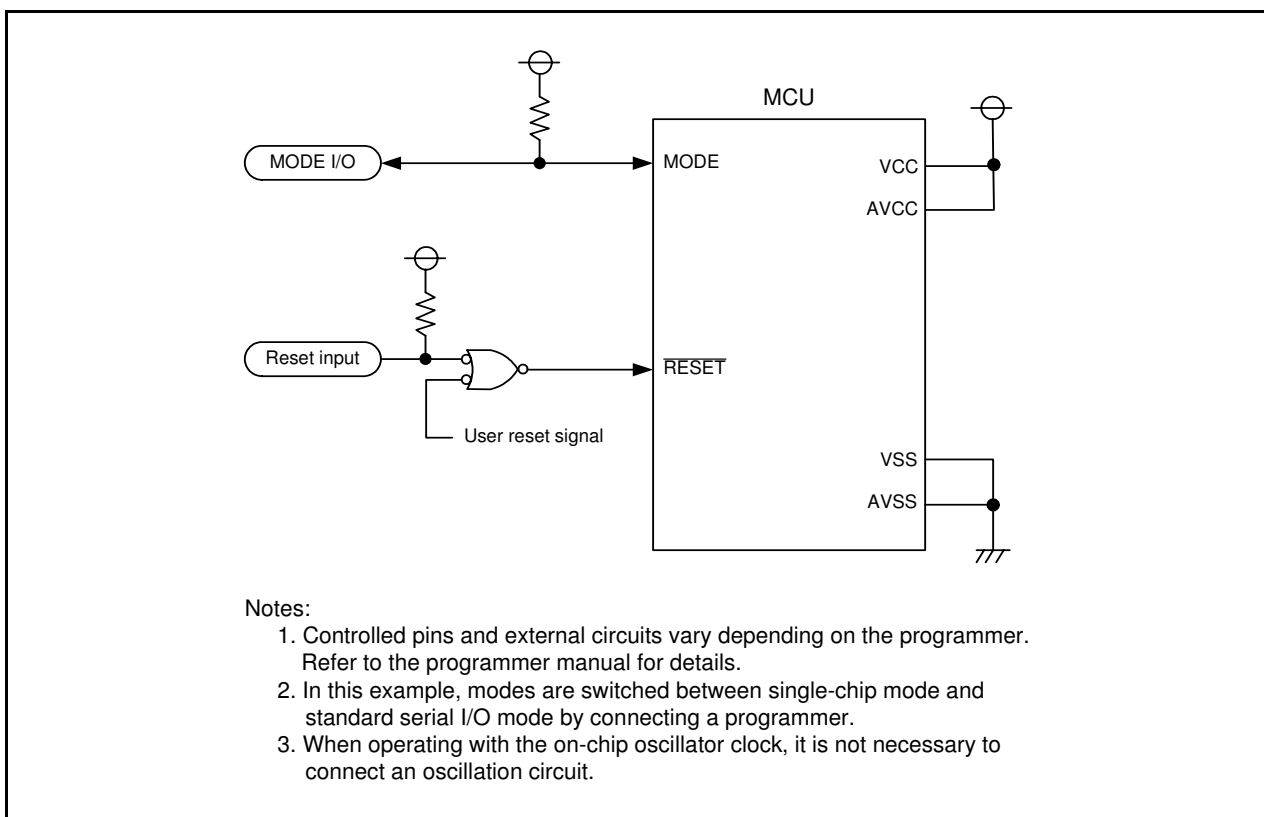
**Table 24.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)**

| Pin                         | Name                    | I/O | Description   |
|-----------------------------|-------------------------|-----|---|
| VCC, VSS                    | Power supply input      |     | Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin. |
| RESET                       | Reset input             | I   | Reset input pin   |
| P4_6/XIN/(XCIN)             | P4_6 input/clock input  | I   | Connect a ceramic resonator or crystal oscillator between pins XIN(XCIN) and XOUT(XCOUT).   |
| P4_7/XOUT/(XCOUT)           | P4_7 input/clock output | I/O |   |
| P0_1, P0_2,<br>P0_6, P0_7   | Input port P0           | I   | Input a "H" or "L" level signal or leave open.  |
| P1_0 to P1_3,<br>P1_6, P1_7 | Input port P1           | I   | Input a "H" or "L" level signal or leave open.  |
| P3_3 to P3_5, P3_7          | Input port P3           | I   | Input a "H" or "L" level signal or leave open.  |
| P4_2/VREF, P4_5             | Input port P4           | I   | Input a "H" or "L" level signal or leave open.  |
| MODE                        | MODE                    | I/O | Input a "L" level signal.   |
| P1_4                        | TXD output              | O   | Serial data output pin  |
| P1_5                        | RXD input               | I   | Serial data input pin   |

**Figure 24.16 Pin Handling in Standard Serial I/O Mode 2**

**Table 24.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)**

| Pin                       | Name                    | I/O | Description   |
|---------------------------|-------------------------|-----|---|
| VCC, VSS                  | Power supply input      |     | Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.                                       |
| RESET                     | Reset input             | I   | Reset input pin   |
| P4_6/XIN/(XCIN)           | P4_6 input/clock input  | I   | If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN(XCIN) and XOUT(XCOUT). |
| P4_7/XOUT/(XCOUT)         | P4_7 input/clock output | I/O | To use as an input port, input a "H" or "L" level signal or leave the pin open.   |
| P0_1, P0_2,<br>P0_6, P0_7 | Input port P0           | I   | Input a "H" or "L" level signal or leave open.  |
| P1_0 to P1_7              | Input port P1           | I   | Input a "H" or "L" level signal or leave open.  |
| P3_3 to P3_5, P3_7        | Input port P3           | I   | Input a "H" or "L" level signal or leave open.  |
| P4_2/VREF, P4_5           | Input port P4           | I   | Input a "H" or "L" level signal or leave open.  |
| MODE                      | MODE                    | I/O | Serial data I/O pin. Connect the pin to a programmer.   |

**Figure 24.17 Pin Handling in Standard Serial I/O Mode 3**

## 24.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.

Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.

In parallel I/O mode, the user ROM areas shown in Figure 24.1 can be rewritten.

### 24.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to the **24.3.2 ROM Code Protect Function**.)



## 24.7 Notes on Flash Memory

### 24.7.1 CPU Rewrite Mode

#### 24.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

#### 24.7.1.2 Interrupts

Tables 24.9 and 24.10 show CPU Rewrite Mode Interrupts, respectively.

**Table 24.9 CPU Rewrite Mode Interrupts (1)**

| Mode | Erase/<br>Write<br>Target | Status  | Maskable Interrupt   |
|------|---------------------------|---|--|
| EW0  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | Usable by allocating a vector in RAM.  |
|      |                           | During auto-erasure<br>(suspend disabled)                 |  |
|      |                           | During<br>auto-programming                                |  |
| EW1  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. |
|      |                           | During auto-erasure<br>(suspend disabled<br>or FMR22 = 0) | Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.  |
|      |                           | During<br>auto-programming                                |  |

FMR21, FMR22: Bits in FMR2 register

**Table 24.10 CPU Rewrite Mode Interrupts (2)**

| Mode | Erase/<br>Write<br>Target | Status  | <ul style="list-style-type: none"> <li>• Watchdog Timer</li> <li>• Oscillation Stop Detection</li> <li>• Voltage Monitor 2</li> <li>• Voltage Monitor 1</li> <li>• NMI</li> </ul> <p style="text-align: right;">(Note 1)</p>  | <ul style="list-style-type: none"> <li>• Undefined Instruction</li> <li>• INTO Instruction</li> <li>• BRK Instruction</li> <li>• Single Step</li> <li>• Address Match</li> <li>• Address Break</li> </ul> <p style="text-align: right;">(Note 1)</p> |
|------|---------------------------|---|---|--|
| EW0  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | <p>When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period.</p> <p>Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally.</p> <p>The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.</p> | Not usable during auto-erasure or auto-programming.  |
|      |                           | During auto-erasure<br>(suspend disabled)                 |   |  |
|      |                           | During<br>auto-programming                                |   |  |
| EW1  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | <p>When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period.</p> <p>Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally.</p> <p>The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.</p> | Not usable during auto-erasure or auto-programming.  |
|      |                           | During auto-erasure<br>(suspend disabled<br>or FMR22 = 0) |   |  |
|      |                           | During<br>auto-programming                                |   |  |

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

### 24.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Do not generate an interrupt between writing 1 and writing 0.

- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

### 24.7.1.4 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

### 24.7.1.5 Programming

Do not write additions to the already programmed address.

### 24.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

If the FST7 in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.

Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

### 24.7.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  as the supply voltage. Do not perform programming and erasure at less than  $2.7\text{ V}$ .

### 24.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

### 24.7.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

To reduce the power consumption, refer to **25. Reducing Power Consumption**.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

## 25. Reducing Power Consumption

### 25.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

### 25.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

#### 25.2.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). If voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).

If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

#### 25.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

#### 25.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation: CM14 bit in CM1 register

Stopping high-speed on-chip oscillator oscillation: FRA00 bit in FRA0 register

#### 25.2.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **9.7 Power Control** for details.

#### 25.2.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

#### 25.2.6 Timers

If timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).

If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).

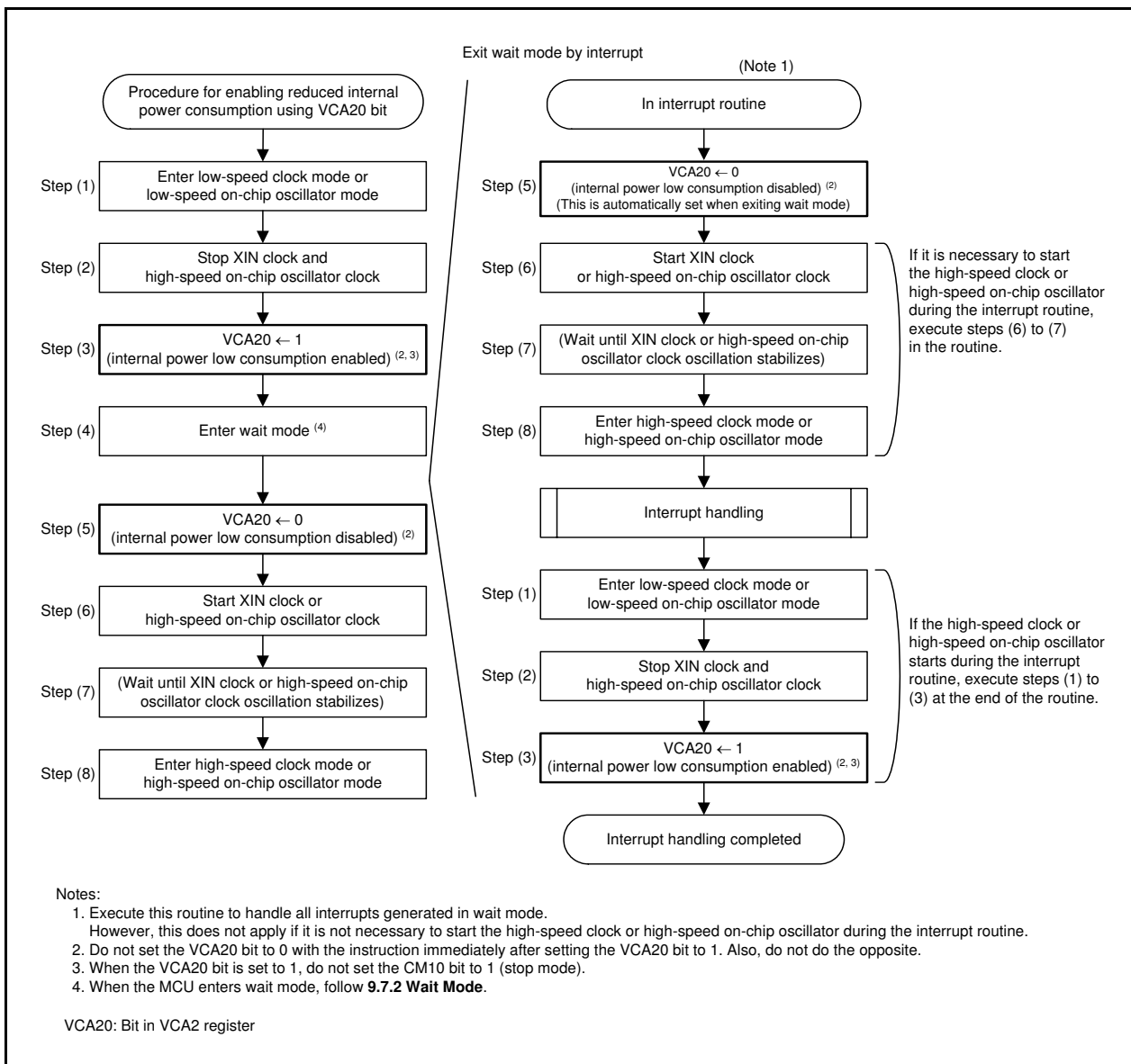
If timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).

#### 25.2.7 A/D Converter

When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

### 25.2.8 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 25.1 shows the Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit. To enable reduced internal power consumption by the VCA20 bit, follow Figure 25.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit.



**Figure 25.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit**

### 25.2.9 Stopping Flash Memory

In low-speed on-chip oscillator mode and low-speed clock mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exit stop mode or wait mode. This eliminates the need to set the FMR0 register.

Figure 25.2 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

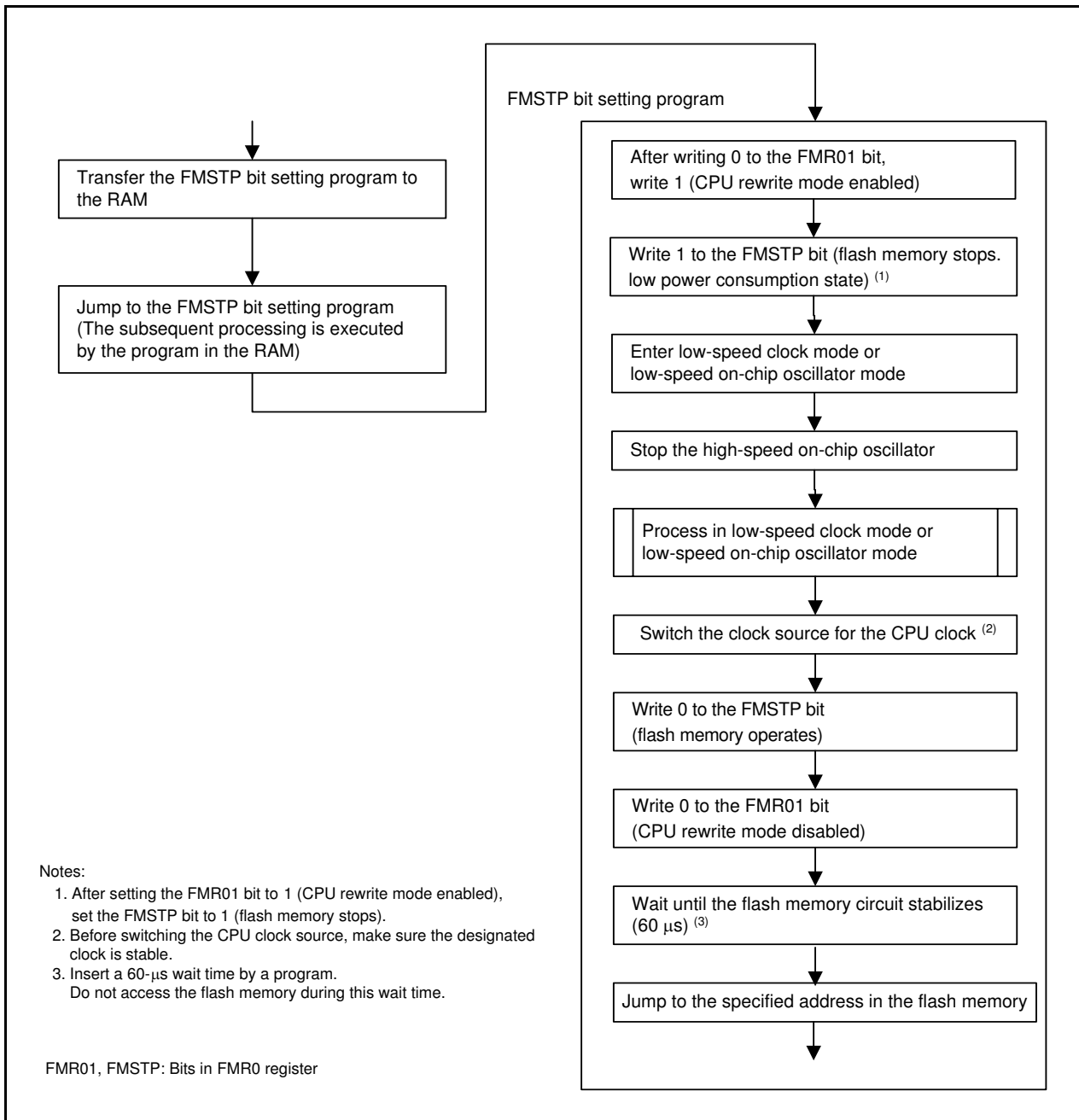


Figure 25.2 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

### 25.2.10 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

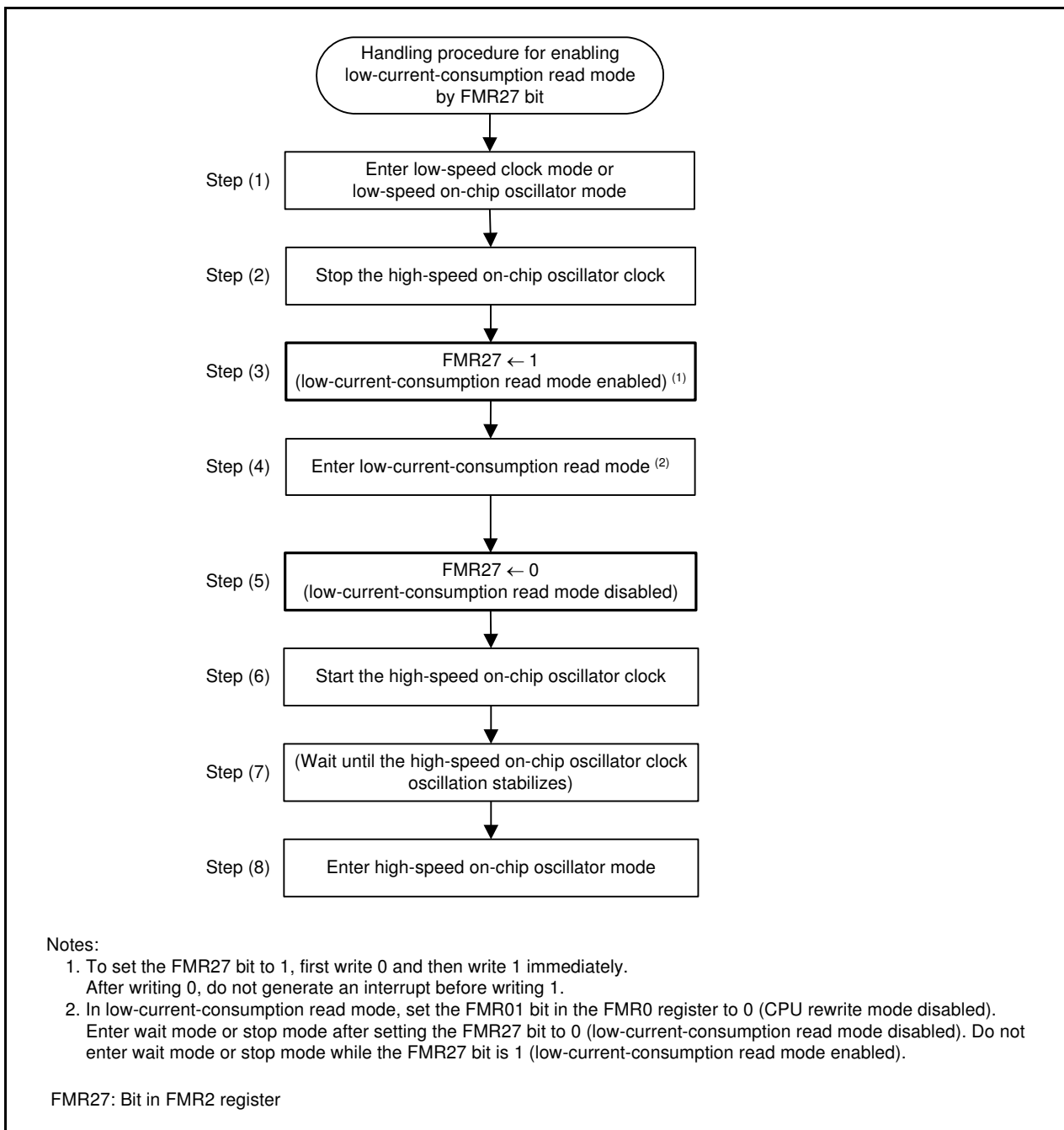
- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

Figure 25.3 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



**Figure 25.3 Handling Procedure Example of Low-Current-Consumption Read Mode**

## 26. Electrical Characteristics

**Table 26.1 Absolute Maximum Ratings**

| Symbol                            | Parameter                     | Condition                       | Rated Value                                      | Unit |
|-----------------------------------|-------------------------------|---------------------------------|--|------|
| V <sub>CC</sub> /AV <sub>CC</sub> | Supply voltage                |                                 | -0.3 to 6.5                                      | V    |
| V <sub>I</sub>                    | Input voltage                 |                                 | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
| V <sub>O</sub>                    | Output voltage                |                                 | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
| P <sub>d</sub>                    | Power dissipation             | -40°C ≤ T <sub>opr</sub> ≤ 85°C | 500  | mW   |
| T <sub>opr</sub>                  | Operating ambient temperature |                                 | -20 to 85 (N version) /<br>-40 to 85 (D version) | °C   |
| T <sub>stg</sub>                  | Storage temperature           |                                 | -65 to 150                                       | °C   |



Table 26.2 Recommended Operating Conditions

| Symbol                            | Parameter   |                                       | Conditions                                | Standard                                     |                                 |                      | Unit                |                      |   |
|-----------------------------------|---|---------------------------------------|---|--|---------------------------------|----------------------|---------------------|----------------------|---|
|                                   |   |                                       |   | Min.   | Typ.                            | Max.                 |                     |                      |   |
| V <sub>CC</sub> /AV <sub>CC</sub> | Supply voltage  |                                       |   | 1.8  | –                               | 5.5                  | V                   |                      |   |
| V <sub>SS</sub> /AV <sub>SS</sub> | Supply voltage  |                                       |   | –  | 0                               | –                    | V                   |                      |   |
| V <sub>IH</sub>                   | Input “H” voltage   | Other than CMOS input                 |   |  | 0.8 V <sub>CC</sub>             | –                    | V <sub>CC</sub>     | V                    |   |
|                                   |   | CMOS input                            | Input level switching function (I/O port) | Input level selection : 0.35 V <sub>CC</sub> | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.5 V <sub>CC</sub>  | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.55 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.65 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   | Input level selection : 0.5 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.65 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.7 V <sub>CC</sub>  | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.8 V <sub>CC</sub>  | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   | Input level selection : 0.7 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0.85 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0.85 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0.85 V <sub>CC</sub> | –                   | V <sub>CC</sub>      | V |
|                                   | External clock input (XOUT)                               |                                       |   | 1.2  | –                               | V <sub>CC</sub>      | V                   |                      |   |
| V <sub>IL</sub>                   | Input “L” voltage   | Other than CMOS input                 |   |  | 0                               | –                    | 0.2 V <sub>CC</sub> | V                    |   |
|                                   |   | CMOS input                            | Input level switching function (I/O port) | Input level selection : 0.35 V <sub>CC</sub> | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | –                   | 0.2 V <sub>CC</sub>  | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | –                   | 0.2 V <sub>CC</sub>  | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | –                   | 0.2 V <sub>CC</sub>  | V |
|                                   |   |                                       |   | Input level selection : 0.5 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | –                   | 0.4 V <sub>CC</sub>  | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | –                   | 0.3 V <sub>CC</sub>  | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | –                   | 0.2 V <sub>CC</sub>  | V |
|                                   |   |                                       |   | Input level selection : 0.7 V <sub>CC</sub>  | 4.0 V ≤ V <sub>CC</sub> ≤ 5.5 V | 0                    | –                   | 0.55 V <sub>CC</sub> | V |
|                                   |   |                                       |   |  | 2.7 V ≤ V <sub>CC</sub> < 4.0 V | 0                    | –                   | 0.45 V <sub>CC</sub> | V |
|                                   |   |                                       |   |  | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | 0                    | –                   | 0.35 V <sub>CC</sub> | V |
|                                   | External clock input (XOUT)                               |                                       |   | 0  | –                               | 0.4                  | V                   |                      |   |
| I <sub>OH(sum)</sub>              | Peak sum output “H” current                               | Sum of all pins I <sub>OH(peak)</sub> |   | –  | –                               | –160                 | mA                  |                      |   |
| I <sub>OH(sum)</sub>              | Average sum output “H” current                            | Sum of all pins I <sub>OH(avg)</sub>  |   | –  | –                               | –80                  | mA                  |                      |   |
| I <sub>OH(peak)</sub>             | Peak output “H” current                                   | Drive capacity Low                    |   | –  | –                               | –10                  | mA                  |                      |   |
|                                   |   | Drive capacity High                   |   | –  | –                               | –40                  | mA                  |                      |   |
| I <sub>OH(avg)</sub>              | Average output “H” current                                | Drive capacity Low                    |   | –  | –                               | –5                   | mA                  |                      |   |
|                                   |   | Drive capacity High                   |   | –  | –                               | –20                  | mA                  |                      |   |
| I <sub>OL(sum)</sub>              | Peak sum output “L” current                               | Sum of all pins I <sub>OL(peak)</sub> |   | –  | –                               | 160                  | mA                  |                      |   |
| I <sub>OL(sum)</sub>              | Average sum output “L” current                            | Sum of all pins I <sub>OL(avg)</sub>  |   | –  | –                               | 80                   | mA                  |                      |   |
| I <sub>OL(peak)</sub>             | Peak output “L” current                                   | Drive capacity Low                    |   | –  | –                               | 10                   | mA                  |                      |   |
|                                   |   | Drive capacity High                   |   | –  | –                               | 40                   | mA                  |                      |   |
| I <sub>OL(avg)</sub>              | Average output “L” current                                | Drive capacity Low                    |   | –  | –                               | 5                    | mA                  |                      |   |
|                                   |   | Drive capacity High                   |   | –  | –                               | 20                   | mA                  |                      |   |
| f <sub>(XIN)</sub>                | XIN clock input oscillation frequency                     | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | –  | –                               | 20                   | MHz                 |                      |   |
|                                   |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   | –  | –                               | 5                    | MHz                 |                      |   |
| f <sub>(XCIN)</sub>               | XCIN clock input oscillation frequency                    | 1.8 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | –  | 32.768                          | 50                   | kHz                 |                      |   |
| f <sub>(OCO40M)</sub>             | When used as the count source for timer RC <sup>(3)</sup> | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | 32   | –                               | 40                   | MHz                 |                      |   |
| f <sub>(OCO-F)</sub>              | f <sub>(OCO-F)</sub> frequency                            | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | –  | –                               | 20                   | MHz                 |                      |   |
|                                   |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   | –  | –                               | 5                    | MHz                 |                      |   |
| –                                 | System clock frequency                                    | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | –  | –                               | 20                   | MHz                 |                      |   |
|                                   |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   | –  | –                               | 5                    | MHz                 |                      |   |
| f <sub>(BCLK)</sub>               | CPU clock frequency                                       | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V       |   | –  | –                               | 20                   | MHz                 |                      |   |
|                                   |   | 1.8 V ≤ V <sub>CC</sub> < 2.7 V       |   | –  | –                               | 5                    | MHz                 |                      |   |

## Notes:

1. V<sub>CC</sub> = 1.8 to 5.5 V at T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. f<sub>(OCO40M)</sub> can be used as the count source for timer RC in the range of V<sub>CC</sub> = 2.7 V to 5.5 V.

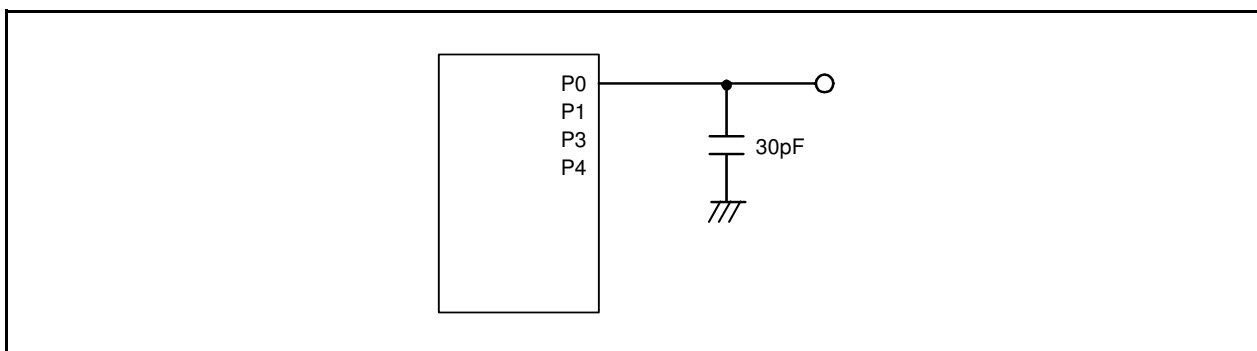


Figure 26.1 Ports P0, P1, P3, P4 Timing Measurement Circuit

**Table 26.3 A/D Converter Characteristics**

| Symbol     | Parameter                 |             | Conditions   | Standard |      |           | Unit          |
|------------|---------------------------|-------------|--|----------|------|-----------|---------------|
|            |                           |             |  | Min.     | Typ. | Max.      |               |
| –          | Resolution                |             | $V_{ref} = AV_{CC}$  | –        | –    | 10        | Bit           |
| –          | Absolute accuracy         | 10-bit mode | $V_{ref} = AV_{CC} = 5.0\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 3$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 3.3\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 5$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 3.0\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 5$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 2.2\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 5$   | LSB           |
|            |                           | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 2$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 3.3\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 2$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 3.0\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 2$   | LSB           |
|            |                           |             | $V_{ref} = AV_{CC} = 2.2\text{ V}$<br>AN0, AN1, AN5, AN6,<br>AN8 to AN11 input | –        | –    | $\pm 2$   | LSB           |
| $\phi AD$  | A/D conversion clock      |             | $4.0 \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (2)                             | 2        | –    | 20        | MHz           |
|            |                           |             | $3.2 \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (2)                             | 2        | –    | 16        | MHz           |
|            |                           |             | $2.7 \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (2)                             | 2        | –    | 10        | MHz           |
|            |                           |             | $2.2 \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}$ (2)                             | 2        | –    | 5         | MHz           |
| –          | Tolerance level impedance |             |  | –        | 3    | –         | $k\Omega$     |
| $t_{CONV}$ | Conversion time           | 10-bit mode | $V_{ref} = AV_{CC} = 5.0\text{ V}$ , $\phi AD = 20\text{ MHz}$                 | 2.15     | –    | –         | $\mu\text{s}$ |
|            |                           | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0\text{ V}$ , $\phi AD = 20\text{ MHz}$                 | 2.15     | –    | –         | $\mu\text{s}$ |
| $t_{SAMP}$ | Sampling time             |             | $\phi AD = 20\text{ MHz}$  | 0.75     | –    | –         | $\mu\text{s}$ |
| $I_{Vref}$ | $V_{ref}$ current         |             | $V_{CC} = 5\text{ V}$ , $XIN = f1 = \phi AD = 20\text{ MHz}$                   | –        | 45   | –         | $\mu\text{A}$ |
| $V_{ref}$  | Reference voltage         |             |  | 2.2      | –    | $AV_{CC}$ | V             |
| $V_{IA}$   | Analog input voltage (3)  |             |  | 0        | –    | $V_{ref}$ | V             |
| $OCVREF$   | On-chip reference voltage |             | $2\text{ MHz} \leq \phi AD \leq 4\text{ MHz}$                                  | 1.19     | 1.34 | 1.49      | V             |

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = -20$  to  $85^\circ\text{C}$  (N version) /  $-40$  to  $85^\circ\text{C}$  (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 26.4 Comparator B Electrical Characteristics**

| Symbol    | Parameter                              |  | Condition                         | Standard |      |                | Unit          |
|-----------|--|--|-----------------------------------|----------|------|----------------|---------------|
|           |  |  |                                   | Min.     | Typ. | Max.           |               |
| $V_{ref}$ | IVREF1, IVREF3 input reference voltage |  |                                   | 0        | –    | $V_{CC} - 1.4$ | V             |
| $V_i$     | IVCMP1, IVCMP3 input voltage           |  |                                   | $-0.3$   | –    | $V_{CC} + 0.3$ | V             |
| –         | Offset                                 |  |                                   | –        | 5    | 100            | mV            |
| $t_d$     | Comparator output delay time (2)       |  | $V_i = V_{ref} \pm 100\text{ mV}$ | –        | 0.1  | –              | $\mu\text{s}$ |
| $I_{CMP}$ | Comparator operating current           |  | $V_{CC} = 5.0\text{ V}$           | –        | 17.5 | –              | $\mu\text{A}$ |

Notes:

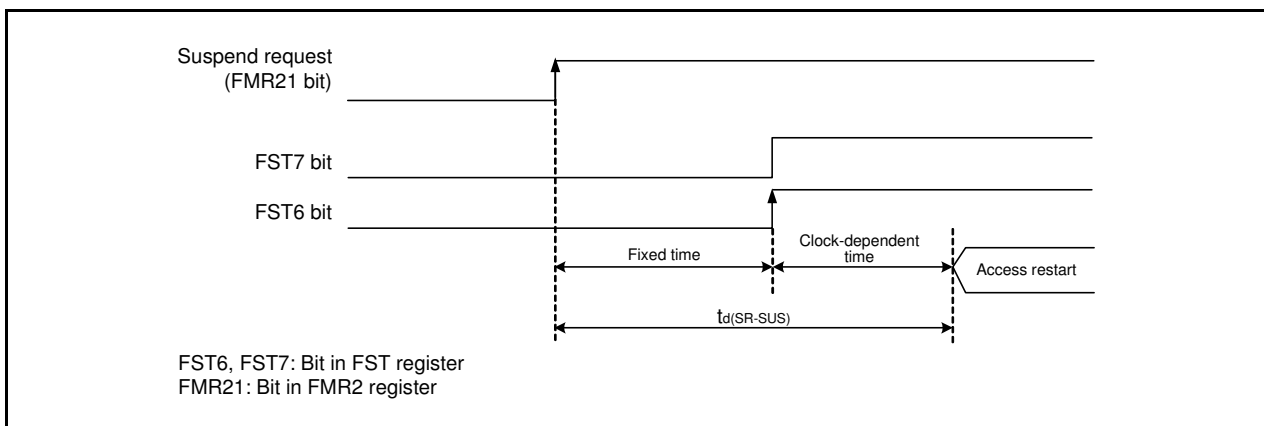
- $V_{CC} = 2.7$  to  $5.5\text{ V}$ ,  $T_{opr} = -20$  to  $85^\circ\text{C}$  (N version) /  $-40$  to  $85^\circ\text{C}$  (D version), unless otherwise specified.
- When the digital filter is disabled.

**Table 26.5 Flash Memory (Program ROM) Electrical Characteristics**

| Symbol                        | Parameter   | Conditions                 | Standard             |      |                           | Unit  |
|-------------------------------|---|----------------------------|----------------------|------|---------------------------|-------|
|                               |   |                            | Min.                 | Typ. | Max.                      |       |
| –                             | Program/erase endurance <sup>(2)</sup>                              |                            | 1,000 <sup>(3)</sup> | –    | –                         | times |
| –                             | Byte program time   |                            | –                    | 80   | 500                       | μs    |
| –                             | Block erase time  |                            | –                    | 0.3  | –                         | s     |
| t <sub>d</sub> (SR-SUS)       | Time delay from suspend request until suspend                       |                            | –                    | –    | 5+CPU clock<br>× 3 cycles | ms    |
| –                             | Interval from erase start/restart until following suspend request   |                            | 0                    | –    | –                         | μs    |
| –                             | Time from suspend until erase restart                               |                            | –                    | –    | 30+CPU clock<br>× 1 cycle | μs    |
| t <sub>d</sub> (CMDRST-READY) | Time from when command is forcibly stopped until reading is enabled |                            | –                    | –    | 30+CPU clock<br>× 1 cycle | μs    |
| –                             | Program, erase voltage  |                            | 2.7                  | –    | 5.5                       | V     |
| –                             | Read voltage  |                            | 1.8                  | –    | 5.5                       | V     |
| –                             | Program, erase temperature  |                            | 0                    | –    | 60                        | °C    |
| –                             | Data hold time <sup>(7)</sup>                                       | Ambient temperature = 55°C | 20                   | –    | –                         | year  |

**Notes:**

- V<sub>CC</sub> = 2.7 to 5.5 V at T<sub>opr</sub> = 0 to 60°C, unless otherwise specified.
- Definition of programming/erasure endurance  
The programming and erasure endurance is defined on a per-block basis.  
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

**Figure 26.2 Time delay until Suspend**

**Table 26.6 Voltage Detection 0 Circuit Electrical Characteristics**

| Symbol  | Parameter   | Condition   | Standard |      |      | Unit |
|---------|---|---|----------|------|------|------|
|         |   |   | Min.     | Typ. | Max. |      |
| Vdet0   | Voltage detection level Vdet0_0 (2)                               |   | 1.80     | 1.90 | 2.05 | V    |
|         | Voltage detection level Vdet0_1 (2)                               |   | 2.15     | 2.35 | 2.50 | V    |
|         | Voltage detection level Vdet0_2 (2)                               |   | 2.70     | 2.85 | 3.05 | V    |
|         | Voltage detection level Vdet0_3 (2)                               |   | 3.55     | 3.80 | 4.05 | V    |
| –       | Voltage detection 0 circuit response time (4)                     | At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V | –        | 6    | 150  | μs   |
| –       | Voltage detection circuit self power consumption                  | VCA25 = 1, Vcc = 5.0 V                              | –        | 1.5  | –    | μA   |
| td(E-A) | Waiting time until voltage detection circuit operation starts (3) |   | –        | –    | 100  | μs   |

## Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

**Table 26.7 Voltage Detection 1 Circuit Electrical Characteristics**

| Symbol  | Parameter  | Condition   | Standard |      |      | Unit |
|---------|--|---|----------|------|------|------|
|         |  |   | Min.     | Typ. | Max. |      |
| Vdet1   | Voltage detection level Vdet1_0 (2)                                  | At the falling of Vcc                               | 2.00     | 2.20 | 2.40 | V    |
|         | Voltage detection level Vdet1_1 (2)                                  | At the falling of Vcc                               | 2.15     | 2.35 | 2.55 | V    |
|         | Voltage detection level Vdet1_2 (2)                                  | At the falling of Vcc                               | 2.30     | 2.50 | 2.70 | V    |
|         | Voltage detection level Vdet1_3 (2)                                  | At the falling of Vcc                               | 2.45     | 2.65 | 2.85 | V    |
|         | Voltage detection level Vdet1_4 (2)                                  | At the falling of Vcc                               | 2.60     | 2.80 | 3.00 | V    |
|         | Voltage detection level Vdet1_5 (2)                                  | At the falling of Vcc                               | 2.75     | 2.95 | 3.15 | V    |
|         | Voltage detection level Vdet1_6 (2)                                  | At the falling of Vcc                               | 2.85     | 3.10 | 3.40 | V    |
|         | Voltage detection level Vdet1_7 (2)                                  | At the falling of Vcc                               | 3.00     | 3.25 | 3.55 | V    |
|         | Voltage detection level Vdet1_8 (2)                                  | At the falling of Vcc                               | 3.15     | 3.40 | 3.70 | V    |
|         | Voltage detection level Vdet1_9 (2)                                  | At the falling of Vcc                               | 3.30     | 3.55 | 3.85 | V    |
|         | Voltage detection level Vdet1_A (2)                                  | At the falling of Vcc                               | 3.45     | 3.70 | 4.00 | V    |
|         | Voltage detection level Vdet1_B (2)                                  | At the falling of Vcc                               | 3.60     | 3.85 | 4.15 | V    |
|         | Voltage detection level Vdet1_C (2)                                  | At the falling of Vcc                               | 3.75     | 4.00 | 4.30 | V    |
|         | Voltage detection level Vdet1_D (2)                                  | At the falling of Vcc                               | 3.90     | 4.15 | 4.45 | V    |
|         | Voltage detection level Vdet1_E (2)                                  | At the falling of Vcc                               | 4.05     | 4.30 | 4.60 | V    |
|         | Voltage detection level Vdet1_F (2)                                  | At the falling of Vcc                               | 4.20     | 4.45 | 4.75 | V    |
| –       | Hysteresis width at the rising of Vcc in voltage detection 1 circuit | Vdet1_0 to Vdet1_5 selected                         | –        | 0.07 | –    | V    |
|         |  | Vdet1_6 to Vdet1_F selected                         | –        | 0.10 | –    | V    |
| –       | Voltage detection 1 circuit response time (3)                        | At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V | –        | 60   | 150  | μs   |
| –       | Voltage detection circuit self power consumption                     | VCA26 = 1, Vcc = 5.0 V                              | –        | 1.7  | –    | μA   |
| td(E-A) | Waiting time until voltage detection circuit operation starts (4)    |   | –        | –    | 100  | μs   |

## Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 26.8 Voltage Detection 2 Circuit Electrical Characteristics**

| Symbol              | Parameter  | Condition   | Standard |      |      | Unit |
|---------------------|--|---|----------|------|------|------|
|                     |  |   | Min.     | Typ. | Max. |      |
| Vdet2               | Voltage detection level Vdet2_0  | At the falling of Vcc                               | 3.70     | 4.00 | 4.30 | V    |
| –                   | Hysteresis width at the rising of Vcc in voltage detection 2 circuit         |   | –        | 0.10 | –    | V    |
| –                   | Voltage detection 2 circuit response time <sup>(2)</sup>                     | At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V | –        | 20   | 150  | μs   |
| –                   | Voltage detection circuit self power consumption                             | VCA27 = 1, Vcc = 5.0 V                              | –        | 1.7  | –    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts <sup>(3)</sup> |   | –        | –    | 100  | μs   |

Notes:

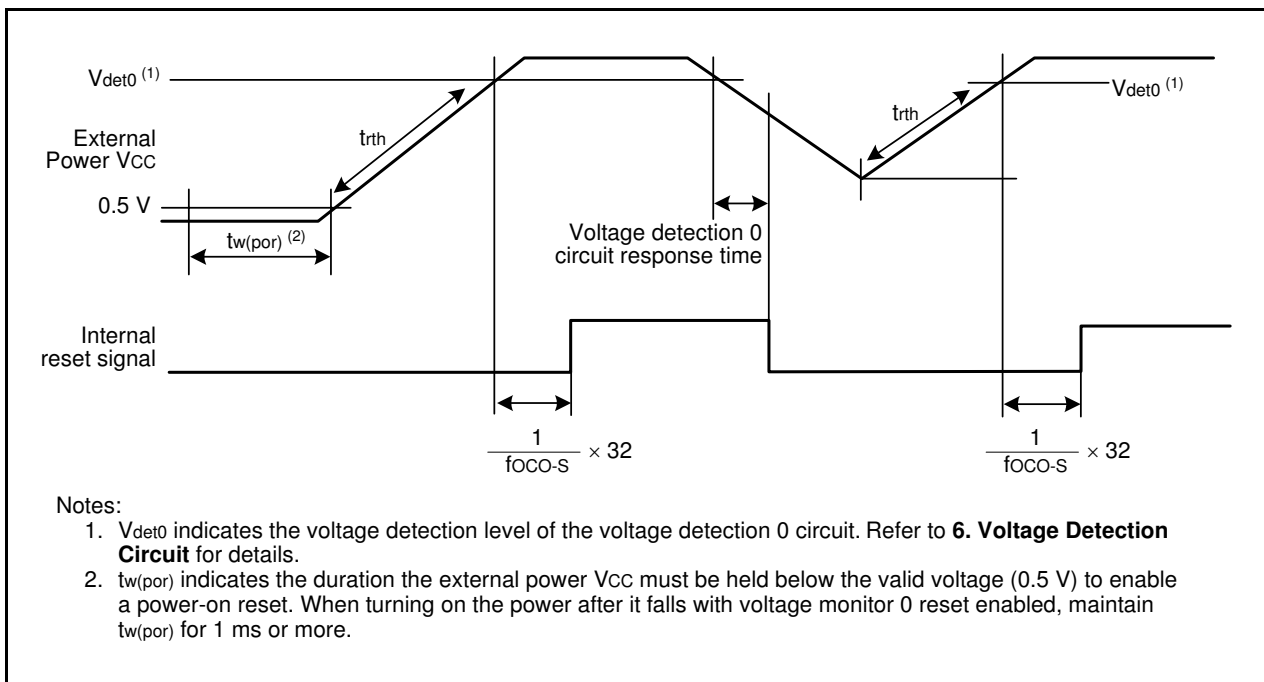
1. The measurement condition is V<sub>CC</sub> = 1.8 V to 5.5 V and T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 26.9 Power-on Reset Circuit (2)**

| Symbol           | Parameter                        | Condition      | Standard |      |       | Unit    |
|------------------|----------------------------------|----------------|----------|------|-------|---------|
|                  |                                  |                | Min.     | Typ. | Max.  |         |
| t <sub>rth</sub> | External power Vcc rise gradient | <sup>(1)</sup> | 0        | –    | 50000 | mV/msec |

Notes:

1. The measurement condition is T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

**Figure 26.3 Power-on Reset Circuit Electrical Characteristics**

**Table 26.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter  | Condition  | Standard |        |        | Unit          |
|--------|--|--|----------|--------|--------|---------------|
|        |  |  | Min.     | Typ.   | Max.   |               |
| –      | High-speed on-chip oscillator frequency after reset  | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 38.4     | 40     | 41.6   | MHz           |
|        |  | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 38.0     | 40     | 42.0   | MHz           |
|        | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register <sup>(2)</sup> | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 35.389   | 36.864 | 38.338 | MHz           |
|        |  | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 35.020   | 36.864 | 38.707 | MHz           |
|        | High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register                | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 30.72    | 32     | 33.28  | MHz           |
|        |  | $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$<br>$-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$ | 30.40    | 32     | 33.60  | MHz           |
| –      | Oscillation stability time   | $V_{CC} = 5.0 \text{ V}, T_{opr} = 25^{\circ}\text{C}$   | –        | 0.5    | 3      | ms            |
| –      | Self power consumption at oscillation  | $V_{CC} = 5.0 \text{ V}, T_{opr} = 25^{\circ}\text{C}$   | –        | 400    | –      | $\mu\text{A}$ |

Notes:

- $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}, T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$  (N version) /  $-40 \text{ to } 85^{\circ}\text{C}$  (D version), unless otherwise specified.
- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 26.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics**

| Symbol | Parameter                              | Condition  | Standard |      |      | Unit          |
|--------|--|--|----------|------|------|---------------|
|        |  |  | Min.     | Typ. | Max. |               |
| fOCO-S | Low-speed on-chip oscillator frequency |  | 60       | 125  | 250  | kHz           |
| –      | Oscillation stability time             | $V_{CC} = 5.0 \text{ V}, T_{opr} = 25^{\circ}\text{C}$ | –        | 30   | 100  | $\mu\text{s}$ |
| –      | Self power consumption at oscillation  | $V_{CC} = 5.0 \text{ V}, T_{opr} = 25^{\circ}\text{C}$ | –        | 2    | –    | $\mu\text{A}$ |

Note:

- $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}, T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$  (N version) /  $-40 \text{ to } 85^{\circ}\text{C}$  (D version), unless otherwise specified.

**Table 26.12 Power Supply Circuit Timing Characteristics**

| Symbol               | Parameter   | Condition | Standard |      |      | Unit          |
|----------------------|---|-----------|----------|------|------|---------------|
|                      |   |           | Min.     | Typ. | Max. |               |
| t <sub>d</sub> (P-R) | Time for internal power supply stabilization during power-on <sup>(2)</sup> |           | –        | –    | 2000 | $\mu\text{s}$ |

Notes:

- The measurement condition is  $V_{CC} = 1.8 \text{ to } 5.5 \text{ V}$  and  $T_{opr} = 25^{\circ}\text{C}$ .
- Waiting time until the internal power supply generation circuit stabilizes during power-on.

**Table 26.13 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]**

| Symbol           | Parameter           |  | Condition                    |               | Standard  |      |      | Unit |
|------------------|---------------------|--|------------------------------|---------------|-----------|------|------|------|
|                  |                     |  |                              |               | Min.      | Typ. | Max. |      |
| VOH              | Output "H" voltage  | Other than XOUT  | Drive capacity High Vcc = 5V | IOH = -20 mA  | Vcc - 2.0 | -    | Vcc  | V    |
|                  |                     |  | Drive capacity Low Vcc = 5V  | IOH = -5 mA   | Vcc - 2.0 | -    | Vcc  | V    |
|                  |                     | XOUT   | Vcc = 5V                     | IOH = -200 μA | 1.0       | -    | Vcc  | V    |
| VOL              | Output "L" voltage  | Other than XOUT  | Drive capacity High Vcc = 5V | IOL = 20 mA   | -         | -    | 2.0  | V    |
|                  |                     |  | Drive capacity Low Vcc = 5V  | IOL = 5 mA    | -         | -    | 2.0  | V    |
|                  |                     | XOUT   | Vcc = 5V                     | IOL = 200 μA  | -         | -    | 0.5  | V    |
| VT+-VT-          | Hysteresis          | INT0, INT1, INT3,<br>KI0, KI1, KI2, KI3,<br>TRAIO, TRBO,<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, RXD2,<br>CLK0, CLK2 |                              |               | 0.1       | 1.2  | -    | V    |
|                  |                     | RESET  |                              |               | 0.1       | 1.2  | -    | V    |
| IiH              | Input "H" current   |  | VI = 5 V, Vcc = 5.0V         |               | -         | -    | 5.0  | μA   |
| IiL              | Input "L" current   |  | VI = 0 V, Vcc = 5.0V         |               | -         | -    | -5.0 | μA   |
| RPULLUP          | Pull-up resistance  |  | VI = 0 V, Vcc = 5.0V         |               | 25        | 50   | 100  | kΩ   |
| RfXIN            | Feedback resistance | XIN  |                              |               | -         | 0.3  | -    | MΩ   |
| RfXCIN           | Feedback resistance | XCIN   |                              |               | -         | 8    | -    | MΩ   |
| V <sub>RAM</sub> | RAM hold voltage    |  | During stop mode             |               | 1.8       | -    | -    | V    |

Note:

1. 4.2 V ≤ Vcc ≤ 5.5 V at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

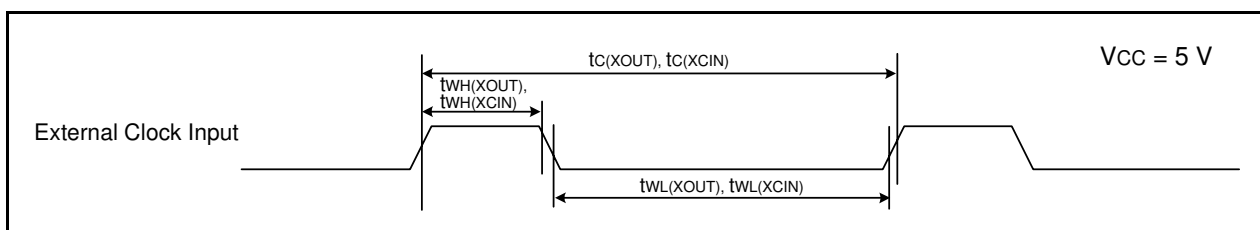


**Table 26.14 Electrical Characteristics (2) [3.3 V ≤ V<sub>CC</sub> ≤ 5.5 V]**  
**(T<sub>opr</sub> = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

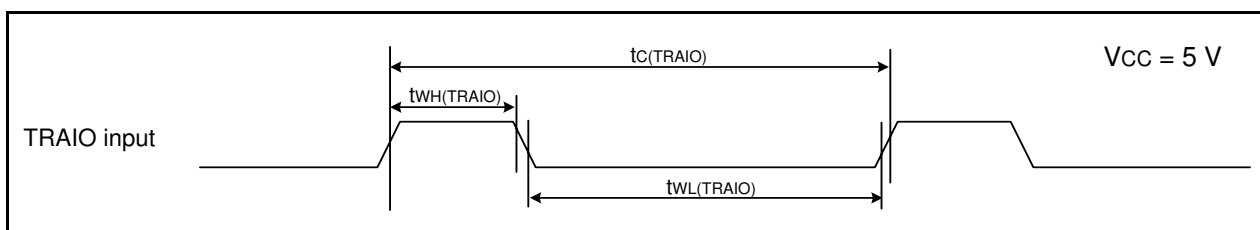
| Symbol          | Parameter   | Condition                          | Standard   |      |      | Unit |    |
|-----------------|---|------------------------------------|--|------|------|------|----|
|                 |   |                                    | Min.   | Typ. | Max. |      |    |
| I <sub>CC</sub> | Power supply current (V <sub>CC</sub> = 3.3 to 5.5 V)<br>Single-chip mode, output pins are open, other pins are V <sub>SS</sub> | High-speed clock mode              | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –    | 6.5  | 15   | mA |
|                 |   |                                    | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –    | 5.3  | 12.5 | mA |
|                 |   |                                    | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –    | 3.6  | –    | mA |
|                 |   |                                    | XIN = 20 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –    | 3.0  | –    | mA |
|                 |   |                                    | XIN = 16 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –    | 2.2  | –    | mA |
|                 |   |                                    | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –    | 1.5  | –    | mA |
|                 |   | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –    | 7.0  | 15   | mA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –    | 3.0  | –    | mA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTTRC = 1  | –    | 1    | –    | mA |
|                 |   | Low-speed on-chip oscillator mode  | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0   | –    | 90   | 400  | μA |
|                 |   | Low-speed clock mode               | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0   | –    | 85   | 400  | μA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0                   | –    | 47   | –    | μA |
|                 |   | Wait mode                          | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1                      | –    | 15   | 100  | μA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1                            | –    | 4    | 90   | μA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | –    | 3.5  | –    | μA |
|                 |   | Stop mode                          | XIN clock off, T <sub>opr</sub> = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0   | –    | 2.0  | 5.0  | μA |
|                 |   |                                    | XIN clock off, T <sub>opr</sub> = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0   | –    | 5.0  | –    | μA |

**Timing Requirements (Unless Otherwise Specified:  $V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = 25^\circ\text{C}$ )****Table 26.15 External clock input (XOUT, XCIN)**

| Symbol         | Parameter             | Standard |      | Unit          |
|----------------|-----------------------|----------|------|---------------|
|                |                       | Min.     | Max. |               |
| $t_{c(XOUT)}$  | XOUT input cycle time | 50       | –    | ns            |
| $t_{WH(XOUT)}$ | XOUT input “H” width  | 24       | –    | ns            |
| $t_{WL(XOUT)}$ | XOUT input “L” width  | 24       | –    | ns            |
| $t_{c(XCIN)}$  | XCIN input cycle time | 14       | –    | $\mu\text{s}$ |
| $t_{WH(XCIN)}$ | XCIN input “H” width  | 7        | –    | $\mu\text{s}$ |
| $t_{WL(XCIN)}$ | XCIN input “L” width  | 7        | –    | $\mu\text{s}$ |

**Figure 26.4 External Clock Input Timing Diagram when  $V_{CC} = 5\text{ V}$** **Table 26.16 TRAI0 Input**

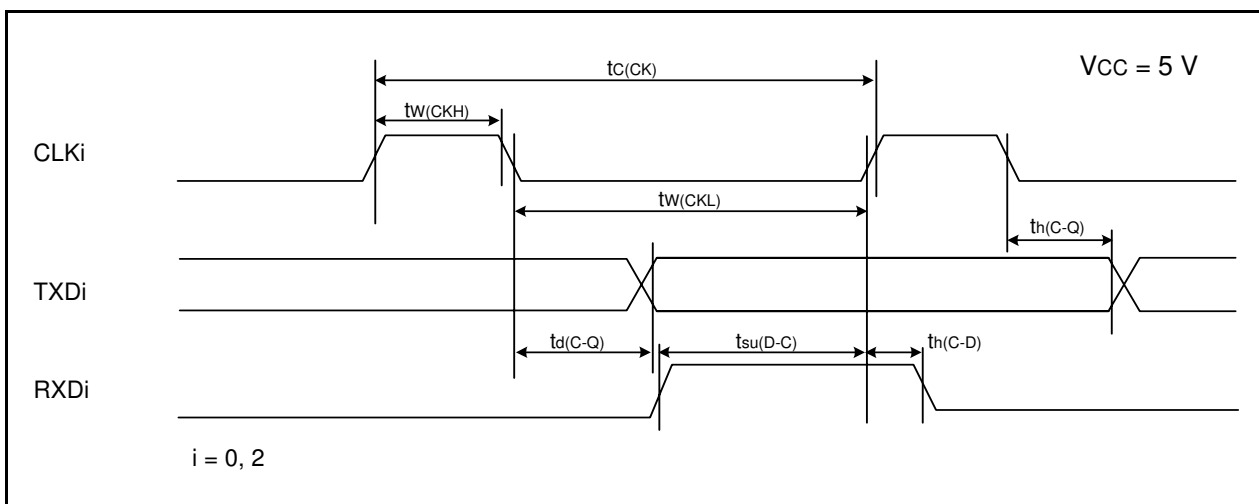
| Symbol          | Parameter              | Standard |      | Unit |
|-----------------|------------------------|----------|------|------|
|                 |                        | Min.     | Max. |      |
| $t_{c(TRAIO)}$  | TRAIO input cycle time | 100      | –    | ns   |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width  | 40       | –    | ns   |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width  | 40       | –    | ns   |

**Figure 26.5 TRAI0 Input Timing Diagram when  $V_{CC} = 5\text{ V}$**

**Table 26.17 Serial Interface**

| Symbol        | Parameter              | Standard |      | Unit |
|---------------|------------------------|----------|------|------|
|               |                        | Min.     | Max. |      |
| $t_{c(CK)}$   | CLKi input cycle time  | 200      | –    | ns   |
| $t_{w(CKH)}$  | CLKi input “H” width   | 100      | –    | ns   |
| $t_{w(CKL)}$  | CLKi input “L” width   | 100      | –    | ns   |
| $t_{d(C-Q)}$  | TXDi output delay time | –        | 50   | ns   |
| $t_{h(C-Q)}$  | TXDi hold time         | 0        | –    | ns   |
| $t_{su(D-C)}$ | RXDi input setup time  | 50       | –    | ns   |
| $t_{h(C-D)}$  | RXDi input hold time   | 90       | –    | ns   |

$i = 0, 2$



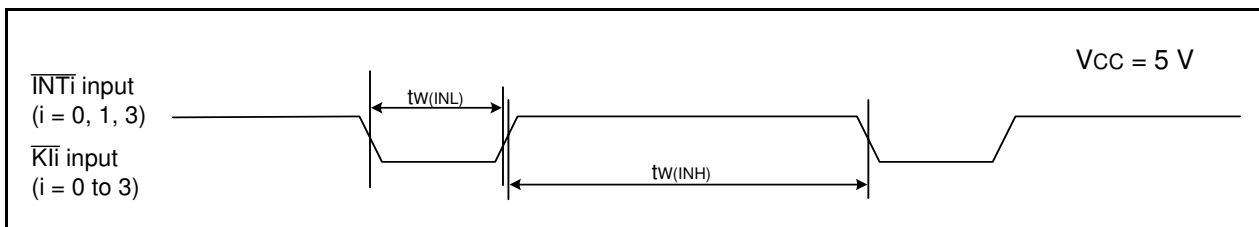
**Figure 26.6 Serial Interface Timing Diagram when Vcc = 5 V**

**Table 26.18 External Interrupt  $\overline{INTi}$  ( $i = 0, 1, 3$ ) Input, Key Input Interrupt  $\overline{Kli}$  ( $i = 0$  to 3)**

| Symbol       | Parameter   | Standard           |      | Unit |
|--------------|---|--------------------|------|------|
|              |   | Min.               | Max. |      |
| $t_{w(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{Kli}$ input “H” width | 250 <sup>(1)</sup> | –    | ns   |
| $t_{w(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{Kli}$ input “L” width | 250 <sup>(2)</sup> | –    | ns   |

Notes:

1. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



**Figure 26.7 Input Timing for External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{Kli}$  when Vcc = 5 V**

**Table 26.19 Electrical Characteristics (3) [ $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$ ]**

| Symbol                           | Parameter           |  | Condition                                     |                           | Standard              |      |                 | Unit |
|----------------------------------|---------------------|--|---|---------------------------|-----------------------|------|-----------------|------|
|                                  |                     |  |   |                           | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  | Other than XOUT  | Drive capacity High                           | I <sub>OH</sub> = -5 mA   | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     |  | Drive capacity Low                            | I <sub>OH</sub> = -1 mA   | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     | XOUT   |   | I <sub>OH</sub> = -200 μA | 1.0                   | -    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  | Other than XOUT  | Drive capacity High                           | I <sub>OL</sub> = 5 mA    | -                     | -    | 0.5             | V    |
|                                  |                     |  | Drive capacity Low                            | I <sub>OL</sub> = 1 mA    | -                     | -    | 0.5             | V    |
|                                  |                     | XOUT   |   | I <sub>OL</sub> = 200 μA  | -                     | -    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | INT0, INT1, INT3,<br>K10, K11, K12, K13,<br>TRAIO, TRBO,<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, RXD2,<br>CLK0, CLK2 | V <sub>CC</sub> = 3.0 V                       |                           | 0.1                   | 0.4  | -               | V    |
|                                  |                     | RESET  | V <sub>CC</sub> = 3.0 V                       |                           | 0.1                   | 0.5  | -               | V    |
| I <sub>IH</sub>                  | Input "H" current   |  | V <sub>I</sub> = 3 V, V <sub>CC</sub> = 3.0 V |                           | -                     | -    | 4.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |  | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3.0 V |                           | -                     | -    | -4.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |  | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 3.0 V |                           | 42                    | 84   | 168             | kΩ   |
| R <sub>IXIN</sub>                | Feedback resistance | XIN  |   |                           | -                     | 0.3  | -               | MΩ   |
| R <sub>IXCIN</sub>               | Feedback resistance | XCIN   |   |                           | -                     | 8    | -               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |  | During stop mode                              |                           | 1.8                   | -    | -               | V    |

Note:

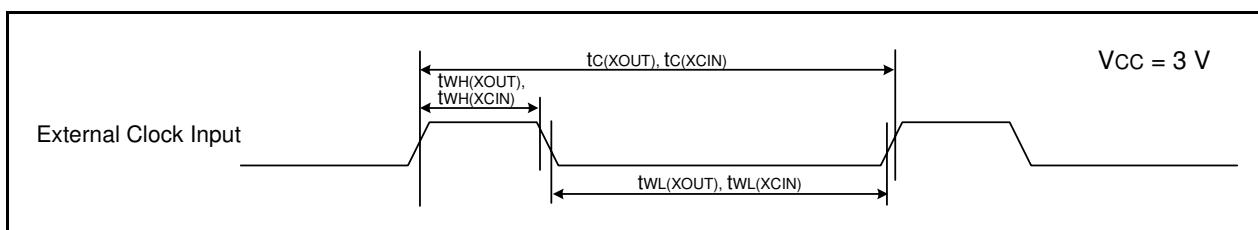
1.  $2.7\text{ V} \leq V_{CC} < 4.2\text{ V}$  at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 26.20 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]**  
**(T<sub>opr</sub> = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

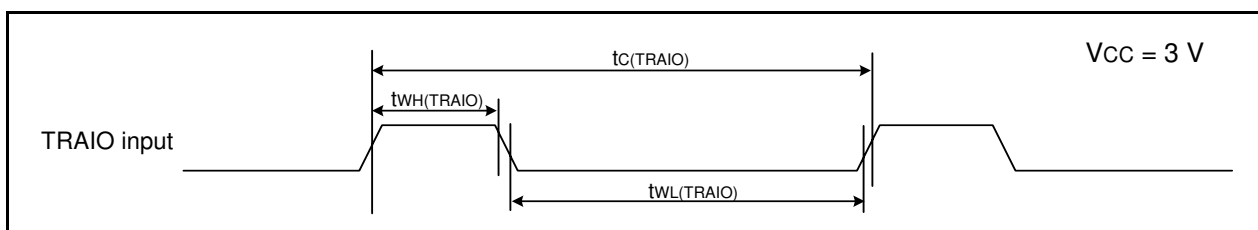
| Symbol          | Parameter   | Condition                          | Standard   |   |      | Unit |     |    |
|-----------------|---|------------------------------------|--|---|------|------|-----|----|
|                 |   |                                    | Min.   | Typ.  | Max. |      |     |    |
| I <sub>cc</sub> | Power supply current (V <sub>cc</sub> = 2.7 to 3.3 V)<br>Single-chip mode, output pins are open, other pins are V <sub>ss</sub> | High-speed clock mode              | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –   | 3.5  | 10   | mA  |    |
|                 |   |                                    | XIN = 10 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –   | 1.5  | 7.5  | mA  |    |
|                 |   | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –   | 7.0  | 15   | mA  |    |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 20 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –   | 3.0  | –    | mA  |    |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division  | –   | 4.0  | –    | mA  |    |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 10 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8  | –   | 1.5  | –    | mA  |    |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator on f <sub>OCO-F</sub> = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTTRC = 1  | –   | 1    | –    | mA  |    |
|                 |   |                                    | Low-speed on-chip oscillator mode  | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0  | –    | 90   | 390 | μA |
|                 |   | Low-speed clock mode               | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0   | –   | 80   | 400  | μA  |    |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0 | –   | 40   | –    | μA  |    |
|                 |   |                                    | Wait mode  | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | –    | 15   | 90  | μA |
|                 |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1          | –   | 4    | 80   | μA  |    |
|                 |   | Stop mode                          | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0  | –   | 3.5  | –    | μA  |    |
|                 |   |                                    | XIN clock off, T <sub>opr</sub> = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0                                 | –   | 2.0  | 5.0  | μA  |    |
|                 |   |                                    | XIN clock off, T <sub>opr</sub> = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0                                 | –   | 5.0  | –    | μA  |    |

**Timing Requirements (Unless Otherwise Specified:  $V_{CC} = 3\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = 25^\circ\text{C}$ )**
**Table 26.21 External clock input (XOUT, XCIN)**

| Symbol         | Parameter             | Standard |      | Unit          |
|----------------|-----------------------|----------|------|---------------|
|                |                       | Min.     | Max. |               |
| $t_{c(XOUT)}$  | XOUT input cycle time | 50       | –    | ns            |
| $t_{WH(XOUT)}$ | XOUT input "H" width  | 24       | –    | ns            |
| $t_{WL(XOUT)}$ | XOUT input "L" width  | 24       | –    | ns            |
| $t_{c(XCIN)}$  | XCIN input cycle time | 14       | –    | $\mu\text{s}$ |
| $t_{WH(XCIN)}$ | XCIN input "H" width  | 7        | –    | $\mu\text{s}$ |
| $t_{WL(XCIN)}$ | XCIN input "L" width  | 7        | –    | $\mu\text{s}$ |


**Figure 26.8 External Clock Input Timing Diagram when  $V_{CC} = 3\text{ V}$** 
**Table 26.22 TRAI0 Input**

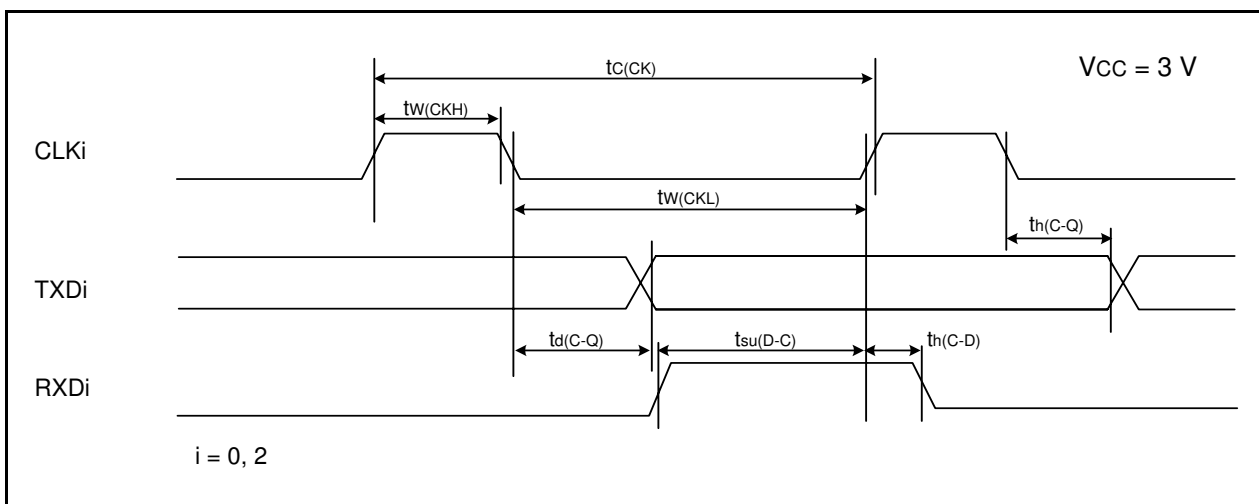
| Symbol          | Parameter              | Standard |      | Unit |
|-----------------|------------------------|----------|------|------|
|                 |                        | Min.     | Max. |      |
| $t_{c(TRAIO)}$  | TRAIO input cycle time | 300      | –    | ns   |
| $t_{WH(TRAIO)}$ | TRAIO input "H" width  | 120      | –    | ns   |
| $t_{WL(TRAIO)}$ | TRAIO input "L" width  | 120      | –    | ns   |


**Figure 26.9 TRAI0 Input Timing Diagram when  $V_{CC} = 3\text{ V}$**

**Table 26.23 Serial Interface**

| Symbol        | Parameter              | Standard |      | Unit |
|---------------|------------------------|----------|------|------|
|               |                        | Min.     | Max. |      |
| $t_{c(CK)}$   | CLKi input cycle time  | 300      | –    | ns   |
| $t_{w(CKH)}$  | CLKi input “H” width   | 150      | –    | ns   |
| $t_{w(CKL)}$  | CLKi Input “L” width   | 150      | –    | ns   |
| $t_{d(C-Q)}$  | TXDi output delay time | –        | 80   | ns   |
| $t_{h(C-Q)}$  | TXDi hold time         | 0        | –    | ns   |
| $t_{su(D-C)}$ | RXDi input setup time  | 70       | –    | ns   |
| $t_{h(C-D)}$  | RXDi input hold time   | 90       | –    | ns   |

$i = 0, 2$



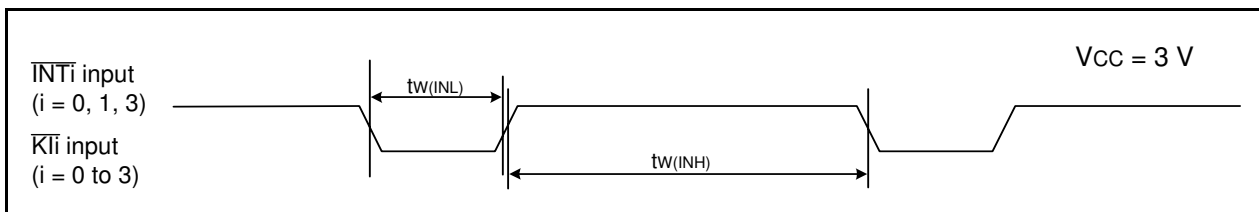
**Figure 26.10 Serial Interface Timing Diagram when  $V_{CC} = 3V$**

**Table 26.24 External Interrupt  $\overline{INT}_i$  ( $i = 0, 1, 3$ ) Input, Key Input Interrupt  $\overline{K}_i$  ( $i = 0$  to 3)**

| Symbol       | Parameter  | Standard |      | Unit |
|--------------|--|----------|------|------|
|              |  | Min.     | Max. |      |
| $t_{w(INH)}$ | $\overline{INT}_i$ input “H” width, $\overline{K}_i$ input “H” width | 380 (1)  | –    | ns   |
| $t_{w(INL)}$ | $\overline{INT}_i$ input “L” width, $\overline{K}_i$ input “L” width | 380 (2)  | –    | ns   |

Notes:

1. When selecting the digital filter by the  $\overline{INT}_i$  input filter select bit, use an  $\overline{INT}_i$  input HIGH width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the  $\overline{INT}_i$  input filter select bit, use an  $\overline{INT}_i$  input LOW width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.



**Figure 26.11 Input Timing for External Interrupt  $\overline{INT}_i$  and Key Input Interrupt  $\overline{K}_i$  when  $V_{CC} = 3V$**

**Table 26.25 Electrical Characteristics (5) [ $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$ ]**

| Symbol                           | Parameter           |  | Condition                                       |                           | Standard              |      |                 | Unit |
|----------------------------------|---------------------|--|---|---------------------------|-----------------------|------|-----------------|------|
|                                  |                     |  |   |                           | Min.                  | Typ. | Max.            |      |
| V <sub>OH</sub>                  | Output "H" voltage  | Other than XOUT  | Drive capacity High                             | I <sub>OH</sub> = -2 mA   | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     |  | Drive capacity Low                              | I <sub>OH</sub> = -1 mA   | V <sub>CC</sub> - 0.5 | -    | V <sub>CC</sub> | V    |
|                                  |                     | XOUT   |   | I <sub>OH</sub> = -200 μA | 1.0                   | -    | V <sub>CC</sub> | V    |
| V <sub>OL</sub>                  | Output "L" voltage  | Other than XOUT  | Drive capacity High                             | I <sub>OL</sub> = 2 mA    | -                     | -    | 0.5             | V    |
|                                  |                     |  | Drive capacity Low                              | I <sub>OL</sub> = 1 mA    | -                     | -    | 0.5             | V    |
|                                  |                     | XOUT   |   | I <sub>OL</sub> = 200 μA  | -                     | -    | 0.5             | V    |
| V <sub>T+</sub> -V <sub>T-</sub> | Hysteresis          | INT0, INT1, INT3,<br>KI0, KI1, KI2, KI3,<br>TRAIO, TRBO,<br>TRCIOA, TRCIOB,<br>TRCIOC, TRCIOD,<br>TRCTRG, TRCCLK,<br>ADTRG,<br>RXD0, RXD2,<br>CLK0, CLK2 |   |                           | 0.05                  | 0.2  | -               | V    |
|                                  |                     | RESET  |   |                           | 0.05                  | 0.20 | -               | V    |
| I <sub>IH</sub>                  | Input "H" current   |  | V <sub>I</sub> = 2.2 V, V <sub>CC</sub> = 2.2 V |                           | -                     | -    | 4.0             | μA   |
| I <sub>IL</sub>                  | Input "L" current   |  | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 2.2 V   |                           | -                     | -    | -4.0            | μA   |
| R <sub>PULLUP</sub>              | Pull-up resistance  |  | V <sub>I</sub> = 0 V, V <sub>CC</sub> = 2.2 V   |                           | 70                    | 140  | 300             | kΩ   |
| R <sub>I<sub>XIN</sub></sub>     | Feedback resistance | XIN  |   |                           | -                     | 0.3  | -               | MΩ   |
| R <sub>I<sub>XCIN</sub></sub>    | Feedback resistance | XCIN   |   |                           | -                     | 8    | -               | MΩ   |
| V <sub>RAM</sub>                 | RAM hold voltage    |  | During stop mode                                |                           | 1.8                   | -    | -               | V    |

Note:

1.  $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$  at T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

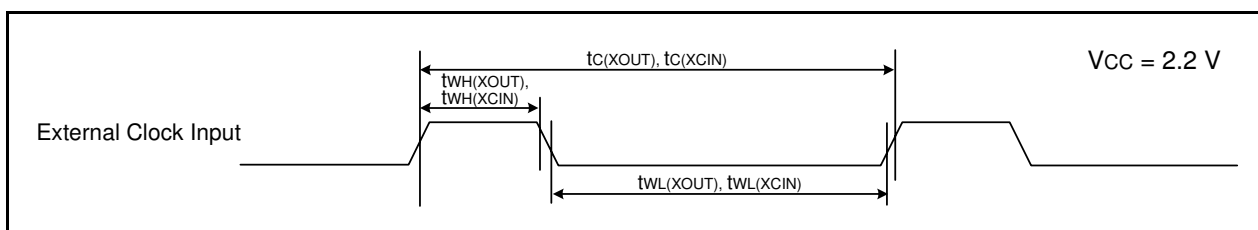


**Table 26.26 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]**  
**(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

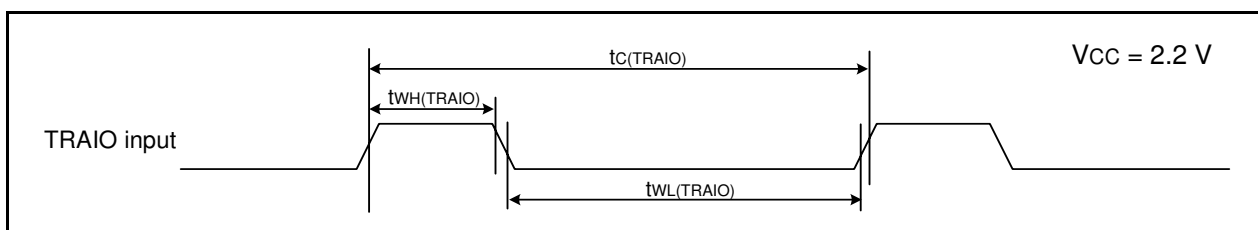
| Symbol | Parameter   | Condition                          | Standard   |      |      | Unit |    |
|--------|---|------------------------------------|--|------|------|------|----|
|        |   |                                    | Min.   | Typ. | Max. |      |    |
| Icc    | Power supply current (Vcc = 1.8 to 2.7 V)<br>Single-chip mode,<br>output pins are open,<br>other pins are Vss | High-speed clock mode              | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>No division   | –    | 2.2  | –    | mA |
|        |   |                                    | XIN = 5 MHz (square wave)<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8   | –    | 0.8  | –    | mA |
|        |   | High-speed on-chip oscillator mode | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>No division   | –    | 2.5  | 10   | mA |
|        |   |                                    | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 5 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8   | –    | 1.7  | –    | mA |
|        |   |                                    | XIN clock off<br>High-speed on-chip oscillator on fOCO-F = 4 MHz<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-16<br>MSTTRC = 1  | –    | 1    | –    | mA |
|        |   | Low-speed on-chip oscillator mode  | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>Divide-by-8, FMR27 = 1, VCA20 = 0   | –    | 90   | 300  | μA |
|        |   | Low-speed clock mode               | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>FMR27 = 1, VCA20 = 0   | –    | 80   | 350  | μA |
|        |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz<br>No division<br>Program operation on RAM<br>Flash memory off, FMSTP = 1, VCA20 = 0                   | –    | 40   | –    | μA |
|        |   | Wait mode                          | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock operation<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1                      | –    | 15   | 90   | μA |
|        |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator on = 125 kHz<br>While a WAIT instruction is executed<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1                            | –    | 4    | 80   | μA |
|        |   |                                    | XIN clock off<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>XCIN clock oscillator on = 32 kHz (peripheral clock off)<br>While a WAIT instruction is executed<br>VCA27 = VCA26 = VCA25 = 0, VCA20 = 1 | –    | 3.5  | –    | μA |
|        |   | Stop mode                          | XIN clock off, Topr = 25°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0   | –    | 2.0  | 5    | μA |
|        |   |                                    | XIN clock off, Topr = 85°C<br>High-speed on-chip oscillator off<br>Low-speed on-chip oscillator off<br>CM10 = 1<br>Peripheral clock off<br>VCA27 = VCA26 = VCA25 = 0   | –    | 5.0  | –    | μA |

**Timing Requirements (Unless Otherwise Specified:  $V_{CC} = 2.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$  at  $T_{opr} = 25^\circ\text{C}$ )****Table 26.27 External clock input (XOUT, XCIN)**

| Symbol         | Parameter             | Standard |      | Unit          |
|----------------|-----------------------|----------|------|---------------|
|                |                       | Min.     | Max. |               |
| $t_{c(XOUT)}$  | XOUT input cycle time | 200      | –    | ns            |
| $t_{WH(XOUT)}$ | XOUT input “H” width  | 90       | –    | ns            |
| $t_{WL(XOUT)}$ | XOUT input “L” width  | 90       | –    | ns            |
| $t_{c(XCIN)}$  | XCIN input cycle time | 14       | –    | $\mu\text{s}$ |
| $t_{WH(XCIN)}$ | XCIN input “H” width  | 7        | –    | $\mu\text{s}$ |
| $t_{WL(XCIN)}$ | XCIN input “L” width  | 7        | –    | $\mu\text{s}$ |

**Figure 26.12 External Clock Input Timing Diagram when  $V_{CC} = 2.2\text{ V}$** **Table 26.28 TRAI0 Input**

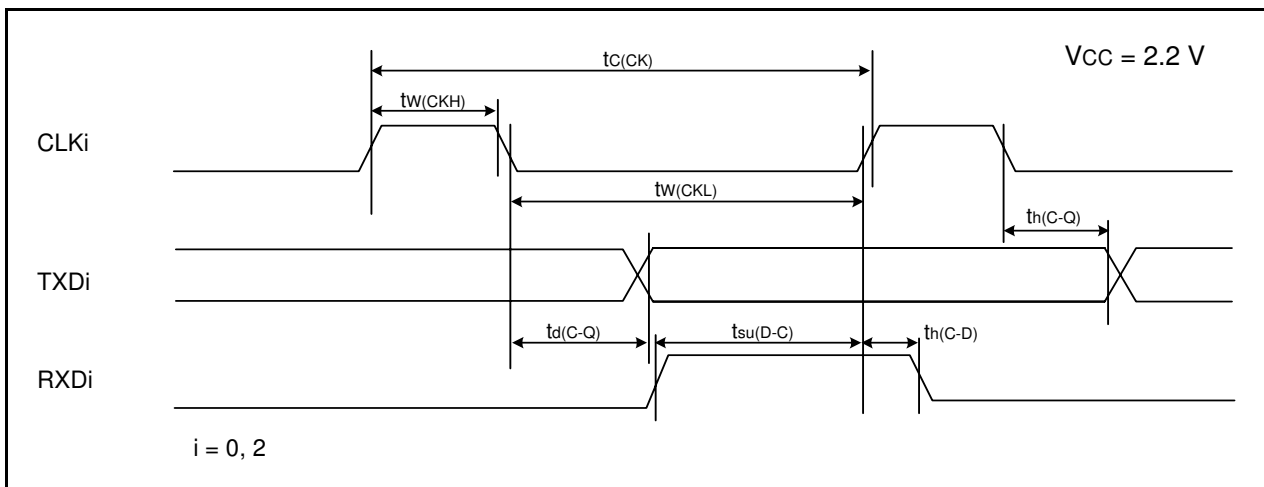
| Symbol          | Parameter              | Standard |      | Unit |
|-----------------|------------------------|----------|------|------|
|                 |                        | Min.     | Max. |      |
| $t_{c(TRAIO)}$  | TRAIO input cycle time | 500      | –    | ns   |
| $t_{WH(TRAIO)}$ | TRAIO input “H” width  | 200      | –    | ns   |
| $t_{WL(TRAIO)}$ | TRAIO input “L” width  | 200      | –    | ns   |

**Figure 26.13 TRAI0 Input Timing Diagram when  $V_{CC} = 2.2\text{ V}$**

**Table 26.29 Serial Interface**

| Symbol        | Parameter              | Standard |      | Unit |
|---------------|------------------------|----------|------|------|
|               |                        | Min.     | Max. |      |
| $t_{c(CK)}$   | CLKi input cycle time  | 800      | –    | ns   |
| $t_{w(CKH)}$  | CLKi input “H” width   | 400      | –    | ns   |
| $t_{w(CKL)}$  | CLKi input “L” width   | 400      | –    | ns   |
| $t_{d(C-Q)}$  | TXDi output delay time | –        | 200  | ns   |
| $t_{h(C-Q)}$  | TXDi hold time         | 0        | –    | ns   |
| $t_{su(D-C)}$ | RXDi input setup time  | 150      | –    | ns   |
| $t_{h(C-D)}$  | RXDi input hold time   | 90       | –    | ns   |

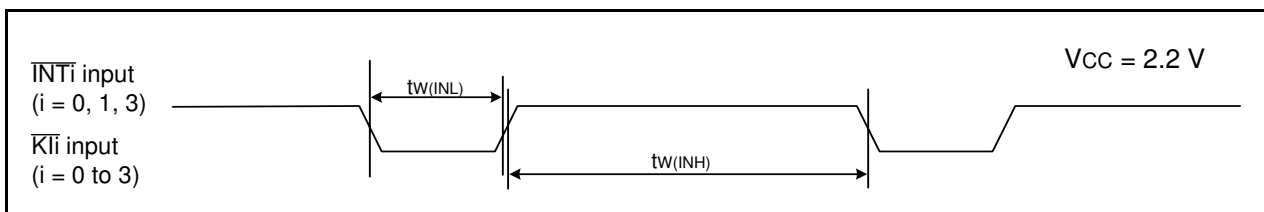
i = 0, 2

**Figure 26.14 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 26.30 External Interrupt  $\overline{INTi}$  (i = 0, 1, 3) Input, Key Input Interrupt  $\overline{Kli}$  (i = 0 to 3)**

| Symbol       | Parameter   | Standard |      | Unit |
|--------------|---|----------|------|------|
|              |   | Min.     | Max. |      |
| $t_{w(INH)}$ | $\overline{INTi}$ input “H” width, $\overline{Kli}$ input “H” width | 1000 (1) | –    | ns   |
| $t_{w(INL)}$ | $\overline{INTi}$ input “L” width, $\overline{Kli}$ input “L” width | 1000 (2) | –    | ns   |

Notes:

- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input HIGH width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{INTi}$  input filter select bit, use an  $\overline{INTi}$  input LOW width of either (1/digital filter clock frequency  $\times$  3) or the minimum value of standard, whichever is greater.

**Figure 26.15 Input Timing for External Interrupt  $\overline{INTi}$  and Key Input Interrupt  $\overline{Kli}$  when Vcc = 2.2 V**

## 27. Usage Notes

### 27.1 Notes on Clock Generation Circuit

#### 27.1.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.

Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```

        BCLR    1, FMR0    ; CPU rewrite mode disabled
        BCLR    7, FMR2    ; Low-current-consumption read mode disabled
        BSET    0, PRCR    ; Writing to CM1 register enabled
        FSET    I          ; Enable interrupt
        BSET    0, CM1     ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP

```

#### 27.1.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.

To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```

        BCLR    1, FMR0    ; CPU rewrite mode disabled
        BCLR    7, FMR2    ; Low-current-consumption read mode disabled
        FSET    I          ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP

```

- Program example to execute the instruction to set the CM30 bit to 1

```

        BCLR    1, FMR0    ; CPU rewrite mode disabled
        BCLR    7, FMR2    ; Low-current-consumption read mode disabled
        BSET    0, PRCR    ; Writing to CM3 register enabled
        FCLR    I          ; Interrupt disabled
        BSET    0, CM3     ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR    ; Writing to CM3 register disabled
        FSET    I          ; Enable interrupt

```

### 27.1.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

### 27.1.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system. To use the MCU with supply voltage below  $VCC = 2.7$  V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled) and connect the feedback resistor to the chip externally.

## 27.2 Notes on Interrupts

### 27.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.

If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

### 27.2.2 SP Setting

Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

### 27.2.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins  $\overline{\text{INT0}}$ ,  $\overline{\text{INT1}}$ ,  $\overline{\text{INT3}}$  and pins  $\overline{\text{KI0}}$  to  $\overline{\text{KI3}}$ , regardless of the CPU clock.

For details, refer to **Table 26.18** (VCC = 5V), **Table 26.24** (VCC = 3V), **Table 26.30** (VCC = 2.2V) **External Interrupt  $\overline{\text{INTi}}$  (i = 0, 1, 3) Input, Key Input Interrupt  $\overline{\text{KIi}}$  (i = 0 to 3).**

### 27.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources. Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts. Figure 27.1 shows a Procedure Example for Changing Interrupt Sources.

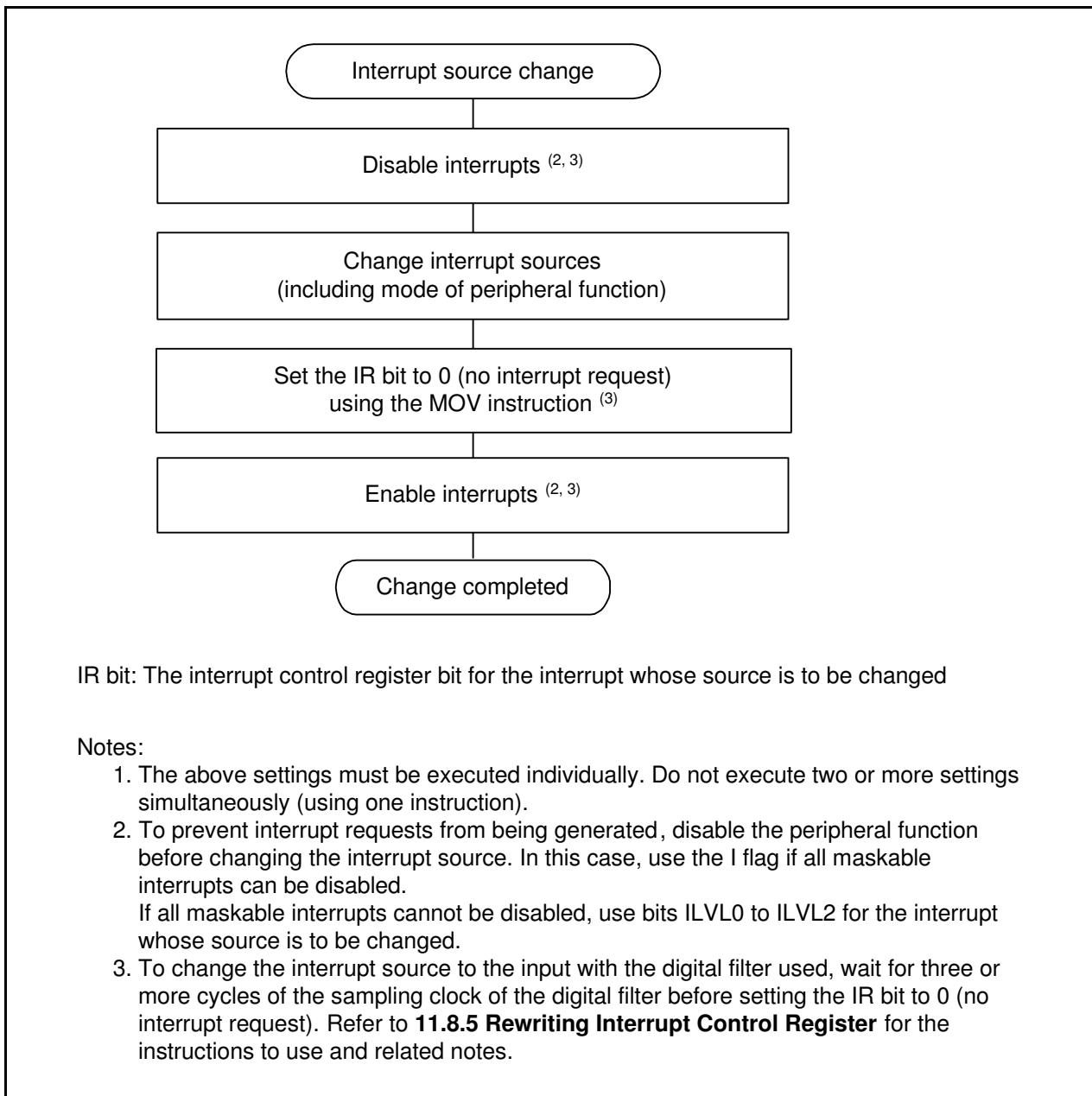


Figure 27.1 Procedure Example for Changing Interrupt Sources

### 27.2.5 Rewriting Interrupt Control Register

- (a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.
- (b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.

#### Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

#### Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

- (c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

#### Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  NOP                    ;
  NOP                    ;
  FSET   I           ; Enable interrupts
```

#### Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  MOV.W  MEM,R0      ; Dummy read
  FSET   I           ; Enable interrupts
```

#### Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC  FLG
  FCLR   I           ; Disable interrupts
  AND.B  #00H,0056H ; Set the TRAIC register to 00h
  POPC   FLG        ; Enable interrupts
```



## 27.3 Notes on ID Code Areas

### 27.3.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h) ; UND
.lword dummy | (55000000h) ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h) ; ADDRESS MATCH
.lword dummy | (55000000h) ; SET SINGLE STEP
.lword dummy | (55000000h) ; WDT
.lword dummy | (55000000h) ; ADDRESS BREAK
.lword dummy | (55000000h) ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

## 27.4 Notes on Option Function Select Area

### 27.4.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF00000h) ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

## 27.5 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

During this time, do not access registers associated with timer RA <sup>(1)</sup> other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

During this time, do not access registers associated with timer RA <sup>(1)</sup> other than the TCSTF bit.

Note:

1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

## 27.6 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

During this time, do not access registers associated with timer RB <sup>(1)</sup> other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.

During this time, do not access registers associated with timer RB <sup>(1)</sup> other than the TCSTF bit.

Note:

1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRES, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

### 27.6.1 Timer Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

### 27.6.2 Programmable Waveform Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

### 27.6.3 Programmable One-shot Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

### 27.6.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRES and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRES register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

## 27.7 Notes on Timer RC

### 27.7.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).

When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.

If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.W      #XXXXh, TRC          ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:         MOV.W      TRC,DATA        ;Read

```

### 27.7.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.B      #XXh, TRCSR        ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:         MOV.B      TRCSR,DATA   ;Read

```

### 27.7.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

### 27.7.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- Wait for a minimum of two cycles of f1.
- Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

- (1) Set the TSTART bit in the TRCMR register to 0 (count stops).
- (2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- (3) Wait for a minimum of two cycles of fOCO-F.
- (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

- (1) Set the TSTART bit in the TRCMR register to 0 (count stops).
- (2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- (3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
- (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

### 27.7.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  - [When the digital filter is not used]  
Three or more cycles of the timer RC operation clock (refer to **Table 18.1 Timer RC Operation Clock**)
  - [When the digital filter is used]  
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 18.5 Digital Filter Block Diagram**).
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

### 27.7.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

### 27.7.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

## 27.8 Notes on Timer RE

### 27.8.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TREC1 register.

Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE <sup>(1)</sup> other than the TCSTF bit.

Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:

1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TREC1, TREC2, and TRECSR.

### 27.8.2 Register Setting

Write to the following registers or bits when timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TREC2
- Bits H12\_H24, PM, and INT in TREC1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TREC1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TREC2 register.

Figure 27.2 shows a Setting Example in Real-Time Clock Mode.

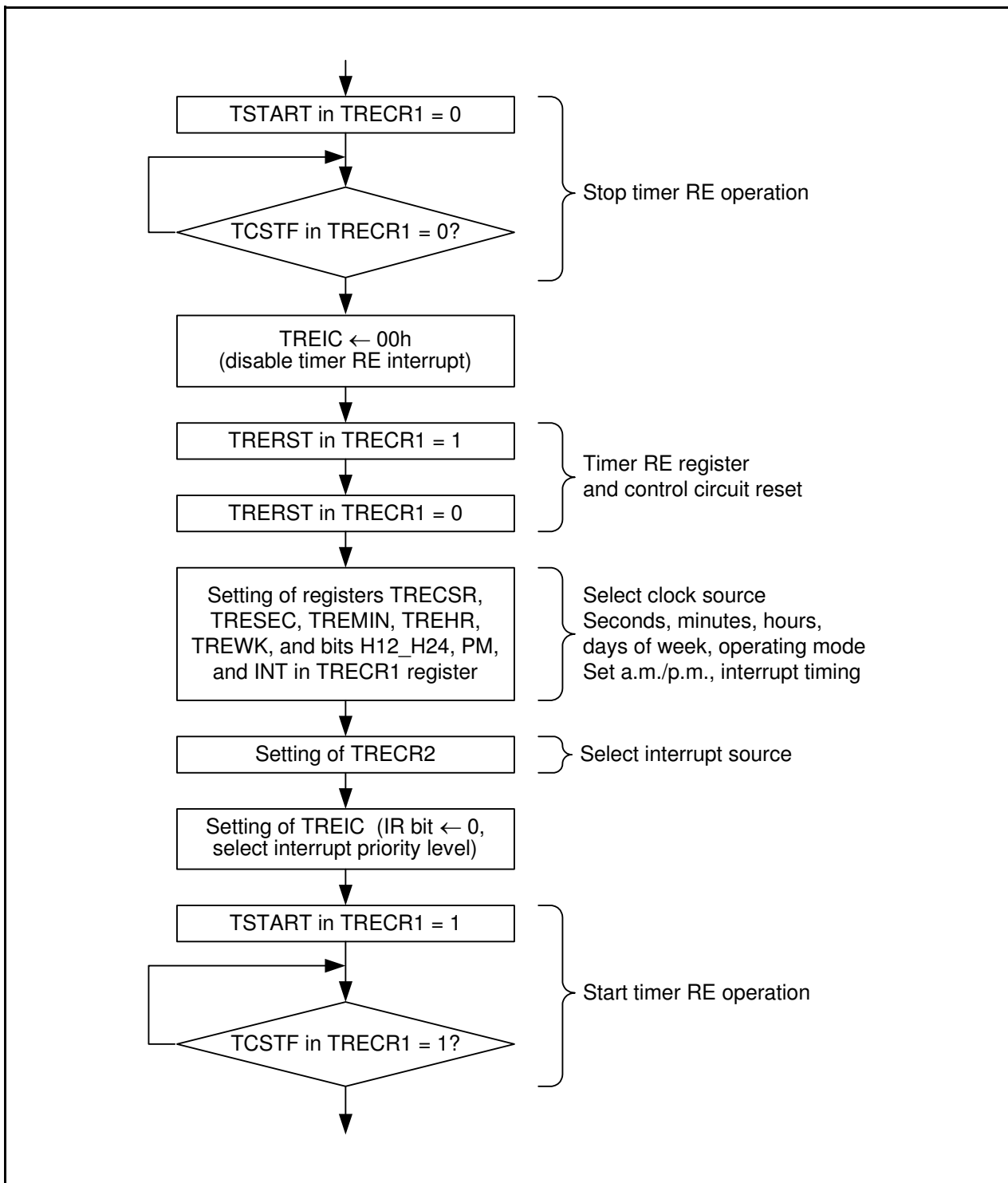


Figure 27.2 Setting Example in Real-Time Clock Mode



### 27.8.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECRI register when the BSY bit is set to 0 (not while data is updated).

Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt

Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register in the timer RE interrupt routine.

- Monitoring with a program 1

Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.

(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).

(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECRI register.

(2) Read the same register as (1) and compare the contents.

(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

## 27.9 Notes on Serial Interface (UART0)

- When reading data from the UORB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.  
When the high-order byte of the UORB register is read, bits PER and FER in the UORB register and the RI bit in the UOC1 register are set to 0.  
To check receive errors, read the UORB register and then use the read data.

Program example to read the receive buffer register:

```
MOV.W    00A6H,R0    ; Read the UORB register
```

- When writing data to the UOTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

Program example to write to the transmit buffer register:

```
MOV.B    #XXH,00A3H  ; Write to the high-order byte of the UOTB register  
MOV.B    #XXH,00A2H  ; Write to the low-order byte of the UOTB register
```

## 27.10 Notes on Serial Interface (UART2)

### 27.10.1 Clock Synchronous Serial I/O Mode

#### 27.10.1.1 Transmission/Reception

When the  $\overline{\text{RTS}}$  function is used with an external clock, the  $\overline{\text{RTS2}}$  pin outputs “L,” which informs the transmitting side that the MCU is ready for a receive operation. The  $\overline{\text{RTS2}}$  pin outputs “H” when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the  $\overline{\text{RTS2}}$  pin to the  $\overline{\text{CTS2}}$  pin of the transmitting side. The  $\overline{\text{RTS}}$  function is disabled when an internal clock is selected.

#### 27.10.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the  $\overline{\text{CTS}}$  function is selected, input on the  $\overline{\text{CTS2}}$  pin = “L”

#### 27.10.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

### 27.10.2 Special Mode 1 (I<sup>2</sup>C Mode)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

### 27.11 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock  $\phi_{AD}$  or more for the CPU clock during A/D conversion.  
Do not select fOCO-F as  $\phi_{AD}$ .
- Connect 0.1  $\mu$ F capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined. If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

## 27.12 Notes on Flash Memory

### 27.12.1 CPU Rewrite Mode

#### 27.12.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

#### 27.12.1.2 Interrupts

Tables 27.1 and 27.2 show CPU Rewrite Mode Interrupts, respectively.

**Table 27.1 CPU Rewrite Mode Interrupts (1)**

| Mode | Erase/<br>Write<br>Target | Status  | Maskable Interrupt  |
|------|---------------------------|---|---|
| EW0  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | Usable by allocating a vector in RAM.   |
|      |                           | During auto-erasure<br>(suspend disabled)                 |   |
|      |                           | During<br>auto-programming                                |   |
| EW1  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | Auto-erasure suspends after $t_d(SR-SUS)$ and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. |
|      |                           | During auto-erasure<br>(suspend disabled<br>or FMR22 = 0) | Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.   |
|      |                           | During<br>auto-programming                                |   |

FMR21, FMR22: Bits in FMR2 register

**Table 27.2 CPU Rewrite Mode Interrupts (2)**

| Mode | Erase/<br>Write<br>Target | Status  | <ul style="list-style-type: none"> <li>• Watchdog Timer</li> <li>• Oscillation Stop Detection</li> <li>• Voltage Monitor 2</li> <li>• Voltage Monitor 1</li> <li>• NMI</li> </ul> <p style="text-align: right;">(Note 1)</p>  | <ul style="list-style-type: none"> <li>• Undefined Instruction</li> <li>• INTO Instruction</li> <li>• BRK Instruction</li> <li>• Single Step</li> <li>• Address Match</li> <li>• Address Break</li> </ul> <p style="text-align: right;">(Note 1)</p> |
|------|---------------------------|---|---|--|
| EW0  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | <p>When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period.</p> <p>Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally.</p> <p>The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.</p> | Not usable during auto-erasure or auto-programming.  |
|      |                           | During auto-erasure<br>(suspend disabled)                 |   |  |
|      |                           | During<br>auto-programming                                |   |  |
| EW1  | Program<br>ROM            | During auto-erasure<br>(suspend enabled)                  | <p>When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period.</p> <p>Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally.</p> <p>The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.</p> | Not usable during auto-erasure or auto-programming.  |
|      |                           | During auto-erasure<br>(suspend disabled<br>or FMR22 = 0) |   |  |
|      |                           | During<br>auto-programming                                |   |  |

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

### 27.12.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Do not generate an interrupt between writing 0 and writing 1.

- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Do not generate an interrupt between writing 1 and writing 0.

- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

### 27.12.1.4 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

### 27.12.1.5 Programming

Do not write additions to the already programmed address.

### 27.12.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

If the FST7 in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.

Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

### 27.12.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$  as the supply voltage. Do not perform programming and erasure at less than  $2.7\text{ V}$ .

### 27.12.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

### 27.12.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

To reduce the power consumption, refer to **25. Reducing Power Consumption**.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).



## 27.13 Notes on Noise

### 27.13.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (at least 0.1  $\mu\text{F}$ ) using the shortest and thickest wire possible.

### 27.13.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

## 28. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/3GD Group, take note of the following:

- (1) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.  
Refer to the on-chip debugger manual for which areas are used.
- (2) Do not set the address match interrupt (registers AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.
- (3) Do not use the BRK instruction in a user system.
- (4) Debugging is available under the condition of supply voltage  $VCC = 1.8\text{ V}$  to  $5.5\text{ V}$ . Set the supply voltage to  $2.7\text{ V}$  or above for rewriting the flash memory.

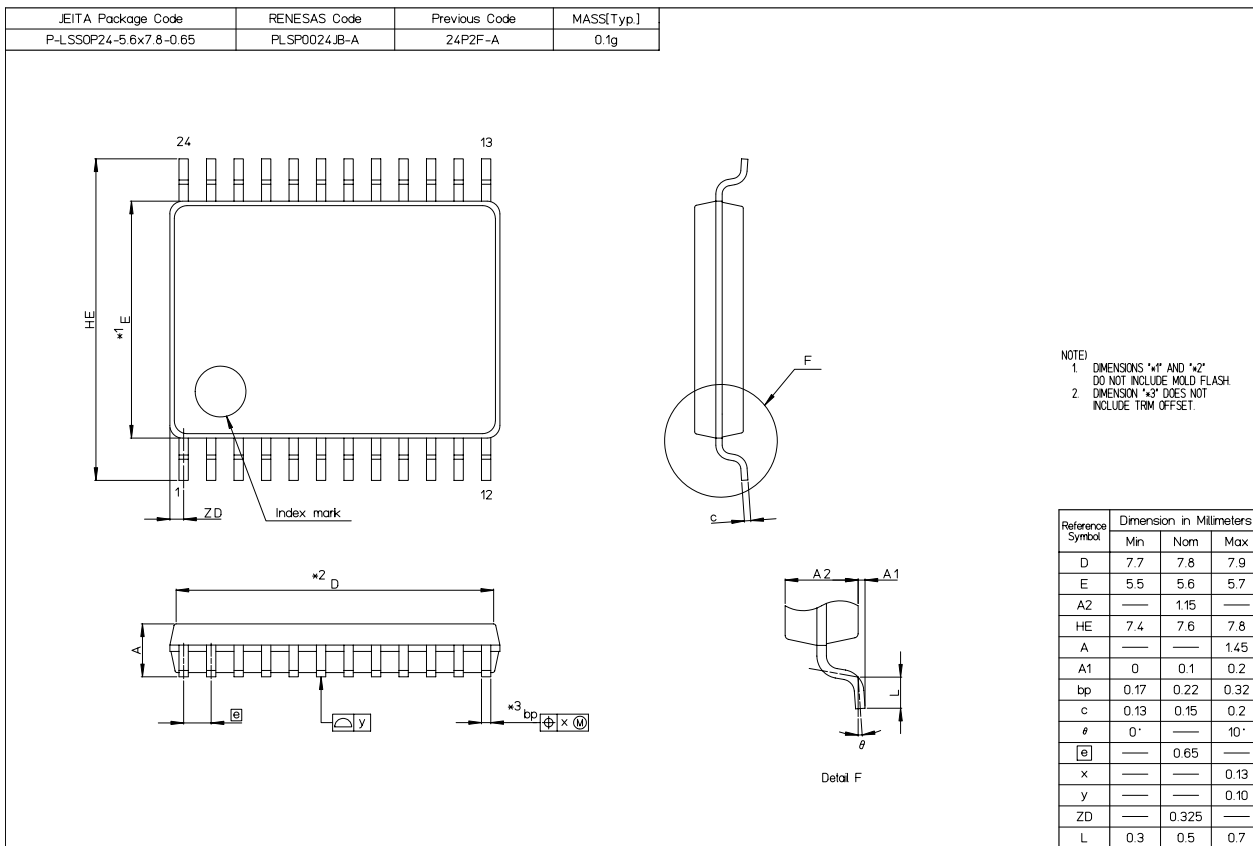
Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

## 29. Notes on Emulator Debugger

Connecting and using the emulator debugger has some special restrictions. Refer to the emulator debugger manual for details.

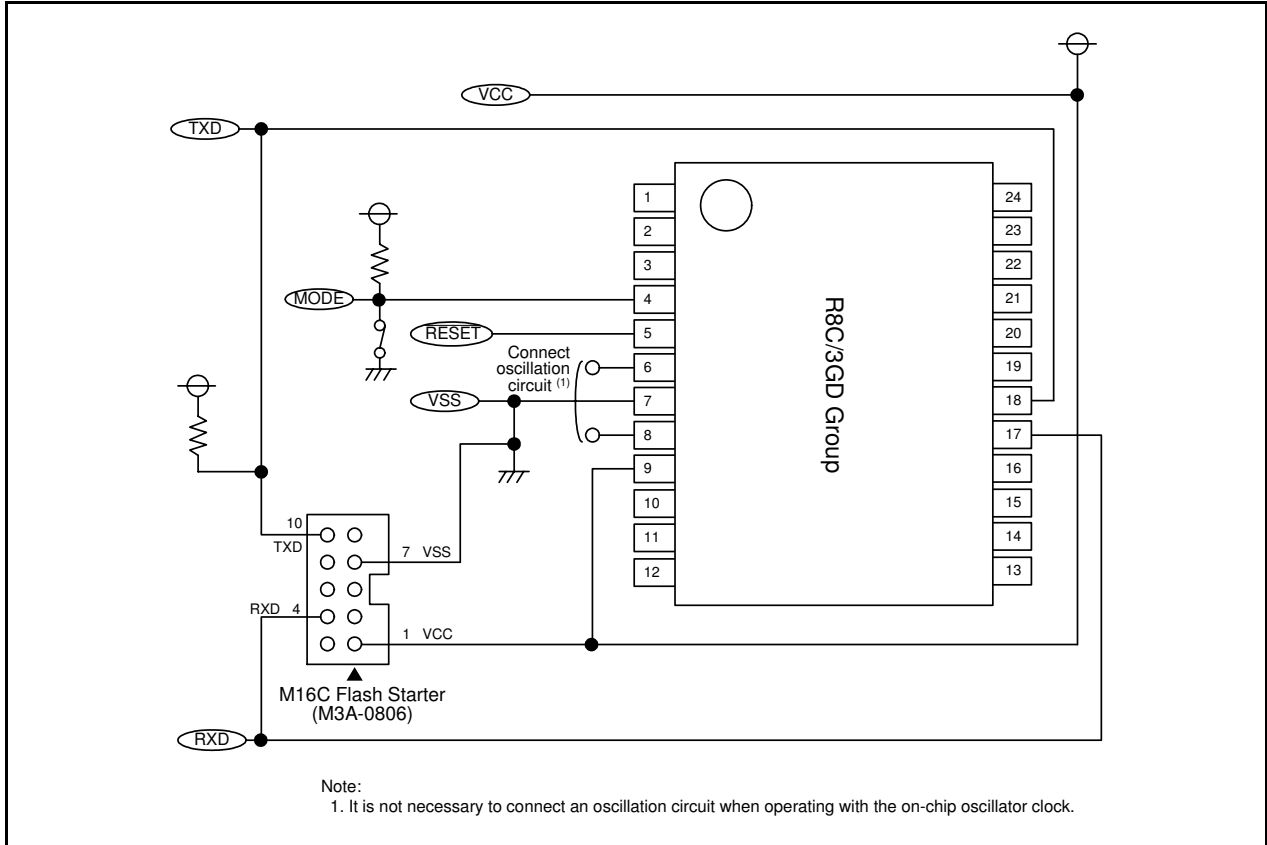
## Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

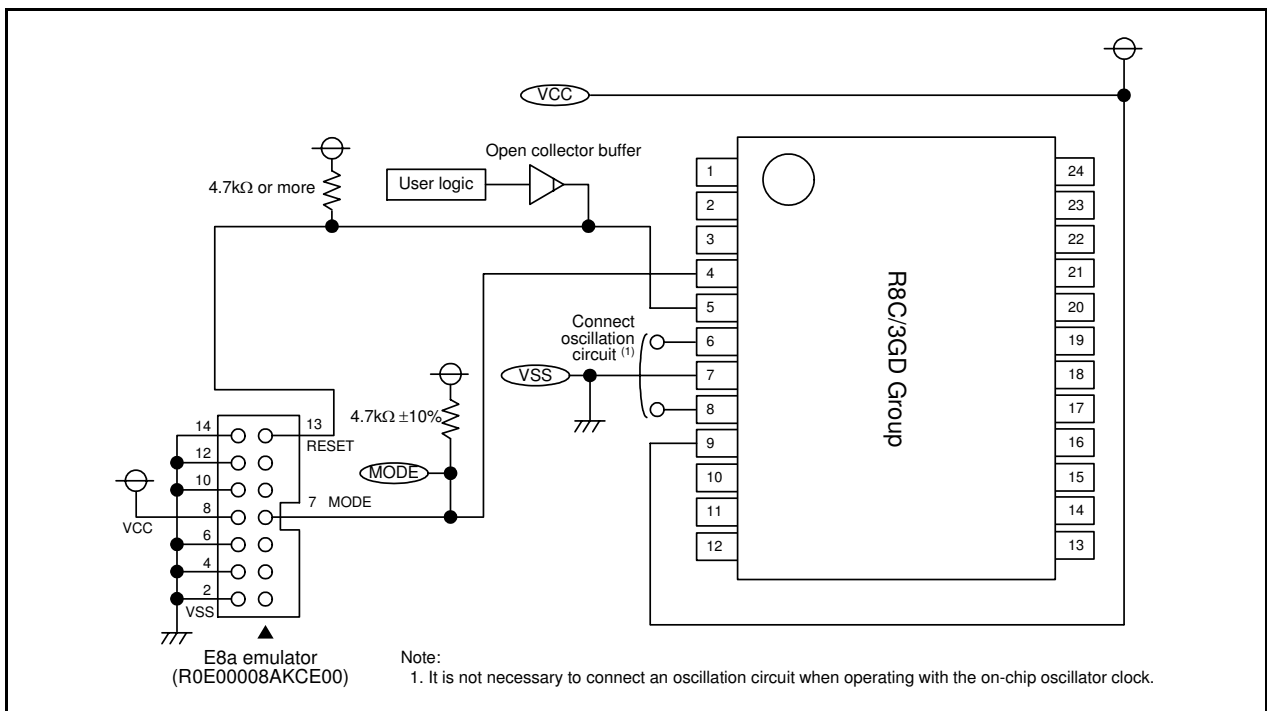


## Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with M16C Flash Starter (M3A-0806) and Appendix Figure 2.2 shows a Connection Example with E8a Emulator (R0E00008AKCE00).



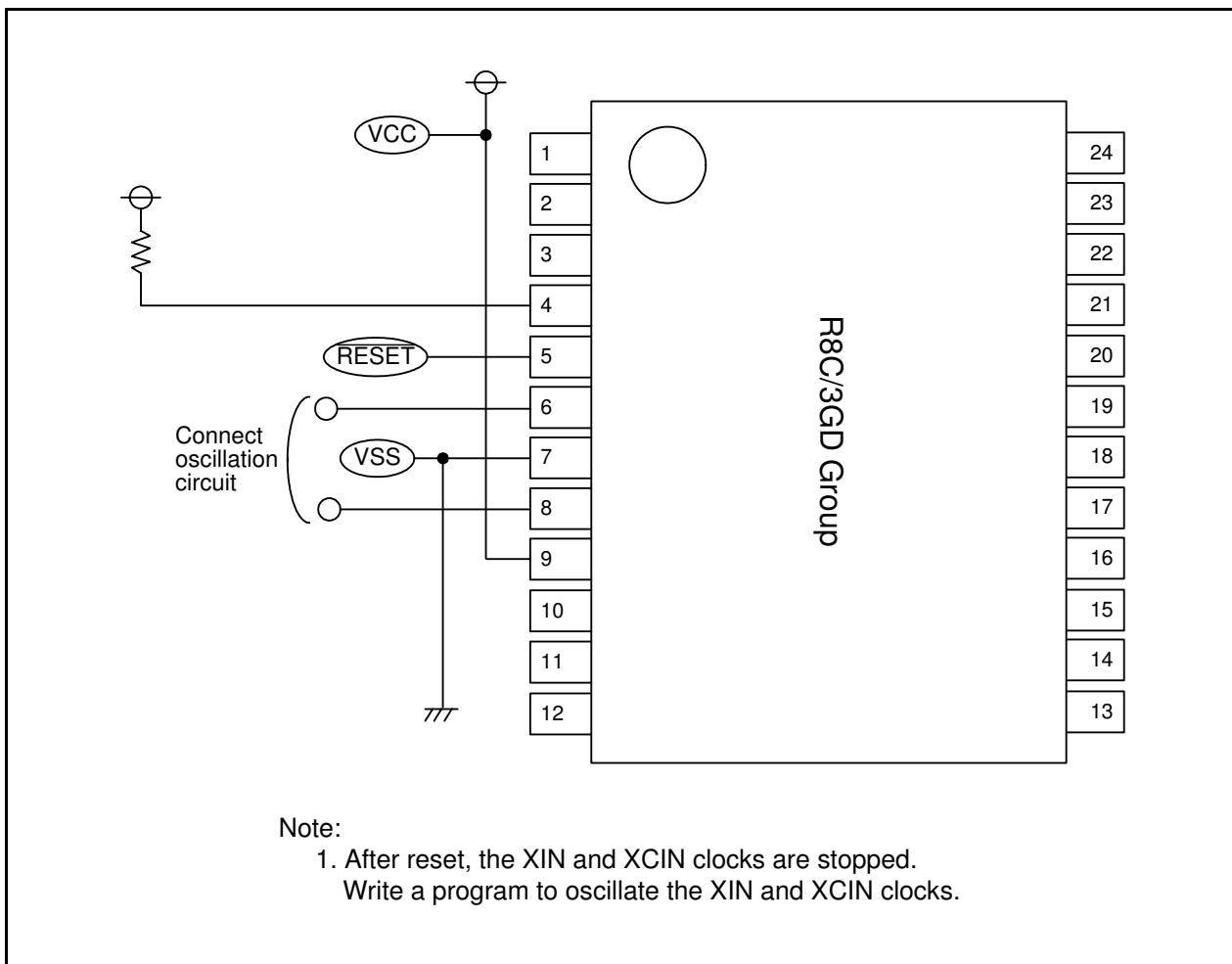
Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)



Appendix Figure 2.2 Connection Example with E8a Emulator (R0E00008AKCE00)

### Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



**Appendix Figure 3.1 Example of Oscillation Evaluation Circuit**

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|      |              | 44          | 6.3.2 and 6.3.3 revised                                       |
|      |              | 46, 48      | Tables 6.2 and 6.3, Notes 1 to 3 revised                      |
|      |              | 49          | Figure 6.7 "VCC or LVCCMP2" → "VCC"                           |
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|      |              | 75 to 78    | Tables 7.9 to 7.12, Tables 7.15                               |
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|      |              | 101         | Figure 9.5 Note 1 revised                                     |
|      |              | 102         | 9.6.5 "VCC = 3.0 to 5.5 V" → "VCC = 2.7 to 5.5 V"             |
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|      |  | 174         | Table 16.4 Function selection: "INT0" → "TRAIO"              |
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|      |  | 183         | Figure 17.1 "TCSTF bit" → "Write 1 to TSTOP bit"             |
|      |  | 185         | 17.2.4 Note 3 added  |
|      |  | 196         | Figure 17.4 revised  |
|      |  | 197         | 17.5.3 "0 (enabled)" → "1 (enabled)", "INT pin" → "INT0 pin" |
|      |  | 201         | 17.7 added   |
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|      |  | 245         | Table 18.14 "(1)" added                                      |
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| 314  | Figure 21.14 revised   |             |  |
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|      |  | 364, 365             | 24.4.1 RDYSTI bit, BSYAEI bit and FST7 bit revised   |
|      |  | 367                  | FMSTP bit, CMDRST bit and CMDERIE bit revised        |
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|      |  | 416                  | Table 26.27, Figure 26.12 revised                    |
|      |  | 418                  | 27.1.1 and 27.1.2 revised                            |
|      |  | 421                  | Figure 27.1: Note 3 revised                          |
| 423  | 27.3.1 and 27.4.1 revised                |                      |  |
| 425  | 27.6 added                               |                      |  |
| 428  | 27.7.5 revised                           |                      |  |
| 434  | 27.10.2, 27.10.2.1 and 27.10.2.2 deleted |                      |  |

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| 1.00 | Feb 22, 2010 | 435         | 27.11 revised                          |
|      |              | 436         | Table 27.1 revised                     |
|      |              | 438         | 27.12.1.3 revised, 27.12.1.9 added     |
|      |              | 439         | 27.13.1 revised                        |
|      |              | 441         | "29. Notes on Emulator Debugger" added |
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